

FAIRCHILD
SEMICONDUCTOR™

January 1992
Revised November 1999

74ABT2952 Octal Registered Transceiver

General Description

The ABT2952 is an octal registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-STATE output enable signals are provided for each register. The output pins are guaranteed to source 32 mA and to sink 64 mA.

Features

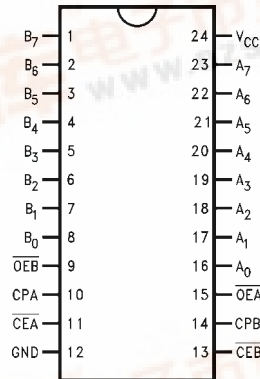
- Separate clock, clock enable and 3-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code:

Order Number	Package Number	Package Description
74ABT2952CSC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT2952CMSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT2952CMTCT	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
A ₀ -A ₇	A-Register Inputs/B-Register 3-STATE Outputs
B ₀ -B ₇	B-Register Inputs/A-Register 3-STATE Outputs
\overline{OEA}	Output Enable A-Register
CPA	A-Register Clock
\overline{CEA}	A-Register Clock Enable
\overline{OEB}	Output Enable B-Register
CPB	B-Register Clock
\overline{CEB}	B-Register Clock Enable

74ABT2952 Octal Registered Transceiver



Truth Table

Output Control

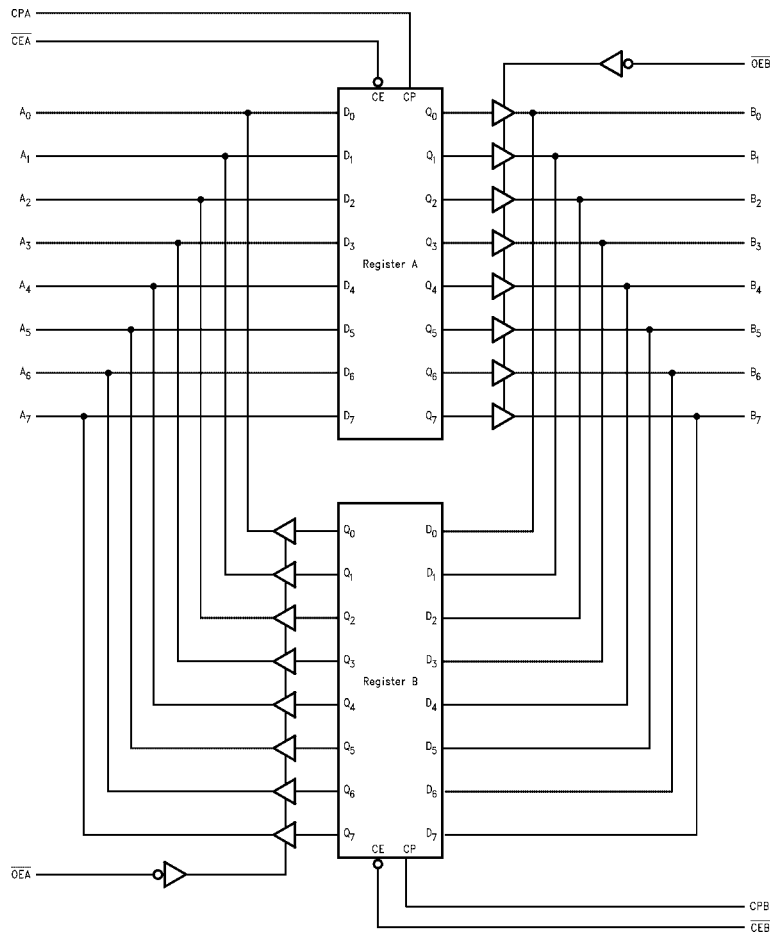
\overline{OE}	Internal Q	Output	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

Register Function Table (Applies to A or B Register)

Inputs			Internal	Function
D	CP	\overline{CE}	Q	
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↗	L	H	

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance
 ↗ = LOW-to-HIGH Transition
 NC = No Change

Block Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	-0.5V to +5.5V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage	2.5					I _{OH} = -3 mA (A _n , B _n) I _{OH} = -32 mA (A _n , B _n)
V _{OL}	Output LOW Voltage			0.55	V	Min	I _{OL} = 64 mA (A _n , B _n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μ A (Non-I/O Pins) All Other Pins Grounded
I _{IH}	Input HIGH Current			1	μ A	Max	V _{IN} = 2.7V (Non-I/O Pins) (Note 3) V _{IN} = V _{CC} (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			7	μ A	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μ A	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current			-1	μ A	Max	V _{IN} = 0.5V (Non-I/O Pins) (Note 3) V _{IN} = 0.0V (Non-I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			10	μ A	0V-5.5V	V _{OUT} = 2.7V (A _n , B _n); OE _A or OE _B = 2.0V
I _{IL} + I _{OZL}	Output Leakage Current			-10	μ A	0V-5.5V	V _{OUT} = 0.5V (A _n , B _n); OE _A or OE _B = 2.0V
I _{OS}	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current			50	μ A	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test			100	μ A	0.0V	V _{OUT} = 5.5V (A _n , B _n); All Others GND
I _{CCH}	Power Supply Current			250	μ A	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			50	μ A	Max	Outputs 3-STATE; All Others GND
I _{CCT}	Additional I _{CC} /Input			2.5	mA	Max	V _I = V _{CC} - 2.1V; All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 4)	No Load		0.18	mA/MHz	Max	Outputs Open OE _A or OE _B = GND, Non-I/O = GND or V _{CC} One Bit toggling, 50% duty cycle (Note 4)

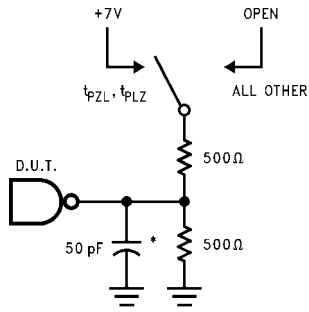
Note 3: Guaranteed, but not tested.

Note 4: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

DC Electrical Characteristics							
(SOIC Package)							
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		0.6	0.8	V	5.0	T _A = 25°C (Note 5)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-1.2	-1.0		V	5.0	T _A = 25°C (Note 5)
V _{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T _A = 25°C (Note 6)
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.7		V	5.0	T _A = 25°C (Note 7)
V _{ILD}	Maximum LOW Level Dynamic Input Voltage		1.2	0.8	V	5.0	T _A = 25°C (Note 7)
<p>Note 5: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.</p> <p>Note 6: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.</p> <p>Note 7: Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.</p>							
AC Electrical Characteristics							
(SOIC and SSOP Package)							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	200			200		MHz
t _{PLH} t _{PHL}	Propagation Delay CPA or CPB to A _n or B _n	1.5	3.4	5.3	1.5	5.3	ns
t _{PZH} t _{PZL}	Output Enable Time OE \bar{A} or OE \bar{B} to A _n or B _n	1.5	3.2	5.5	1.5	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE \bar{A} or OE \bar{B} to A _n or B _n	1.5	3.6	6.0	1.5	6.0	ns
AC Operating Requirements							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF		T _A = -40°C to +85°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		Units	
		Min	Max	Min	Max		
t _S (H) t _S (L)	Setup Time, HIGH or LOW A _n or B _n to CPA or CPB	2.5		2.5		ns	
t _H (H) t _H (L)	Hold Time, HIGH or LOW A _n or B _n to CPA or CPB	1.5		1.5		ns	
t _S (H) t _S (L)	Setup Time, HIGH or LOW \overline{CEA} or \overline{CEB} to CPA or CPB	2.5		2.5		ns	
t _H (H) t _H (L)	Hold Time, HIGH or LOW \overline{CEA} or \overline{CEB} to CPA or CPB	1.5		1.5		ns	
t _W (H) t _W (L)	Pulse Width, HIGH or LOW CPA or CPB	3.0		3.0		ns	

Extended AC Electrical Characteristics								
(SOIC Package)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 8)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 250\text{ pF}$ (Note 9)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 10)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay CPA or CPB to A_n or B_n	1.5	6.0	2.0	8.0	2.5	10.5	ns
t_{PHL}		1.5	6.0	2.0	8.0	2.5	10.5	
t_{PZH}	Output Enable Time	1.5	6.0	2.0	8.0	2.5	11.5	ns
t_{PZL}	$\overline{OE}A$ or $\overline{OE}B$ to A_n or B_n	1.5	6.0	2.0	8.0	2.5	11.5	
t_{PHZ}	Output Disable Time	1.5	6.0	(Note 11)		(Note 11)		ns
t_{PZL}	$\overline{OE}A$ or $\overline{OE}B$ to A_n or B_n	1.5	6.0	(Note 11)		(Note 11)		
<p>Note 8: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p>Note 9: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.</p> <p>Note 10: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p>Note 11: The 3-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.</p>								
Skew								
(SOIC Package)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 12)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 13)		Units		
		Max		Max				
t_{OSHL} (Note 14)	Pin to Pin Skew HL Transitions	1.0		1.5		ns		
t_{OSLH} (Note 14)	Pin to Pin Skew LH Transitions	1.0		2.0		ns		
t_{PS} (Note 15)	Duty Cycle LH-HL Skew	2.0		4.5		ns		
t_{OST} (Note 14)	Pin to Pin Skew LH/HL Transitions	2.1		4.5		ns		
t_{PV} (Note 16)	Device to Device Skew LH/HL Transitions	2.5		5.0		ns		
<p>Note 12: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p>Note 13: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p>Note 14: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). This specification is guaranteed but not tested.</p> <p>Note 15: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.</p> <p>Note 16: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.</p>								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$				
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$ (Non I/O Pins)				
$C_{I/O}$ (Note 17)	Output Capacitance	11	pF	$V_{CC} = 5.0\text{V}$ (A_n, B_n)				
<p>Note 17: $C_{I/O}$ is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883, Method 3012.</p>								

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

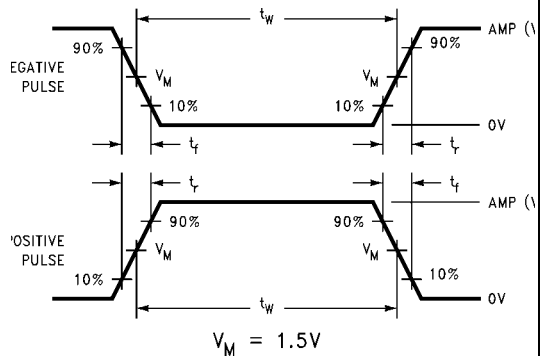


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Input Signal Requirements

AC Waveforms

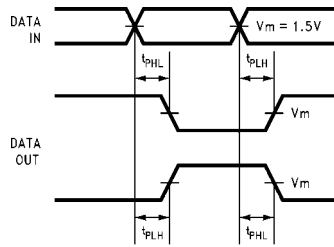


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

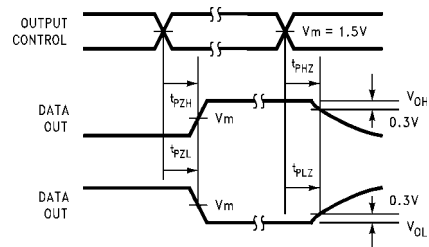


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

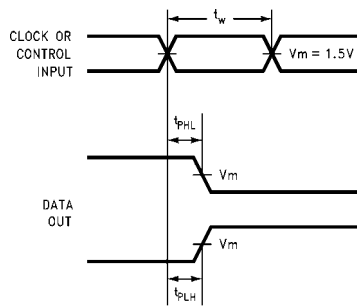


FIGURE 5. Propagation Delay, Pulse Width Waveforms

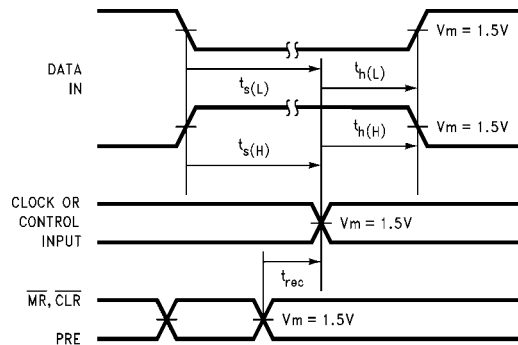
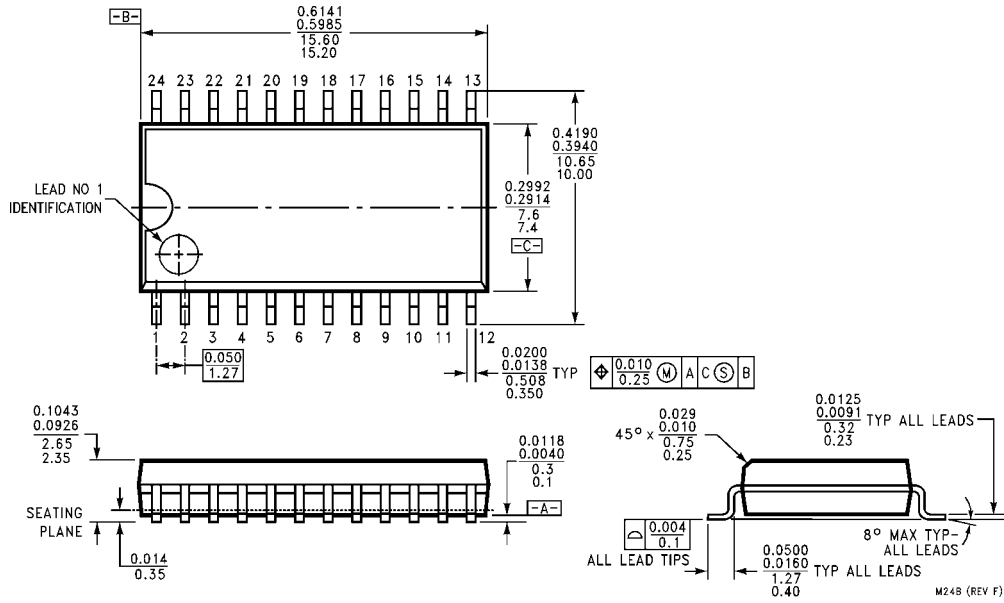
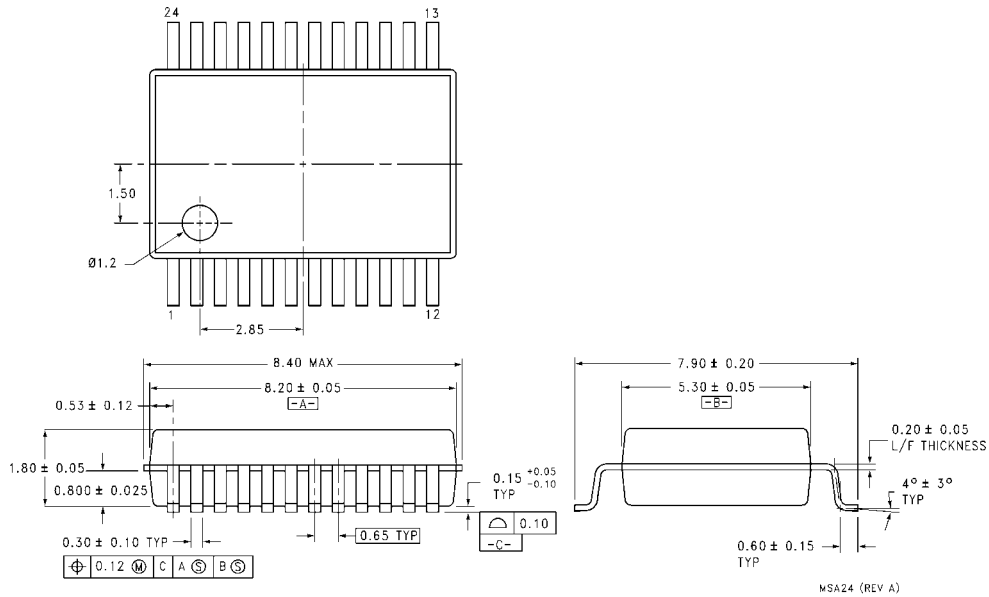


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

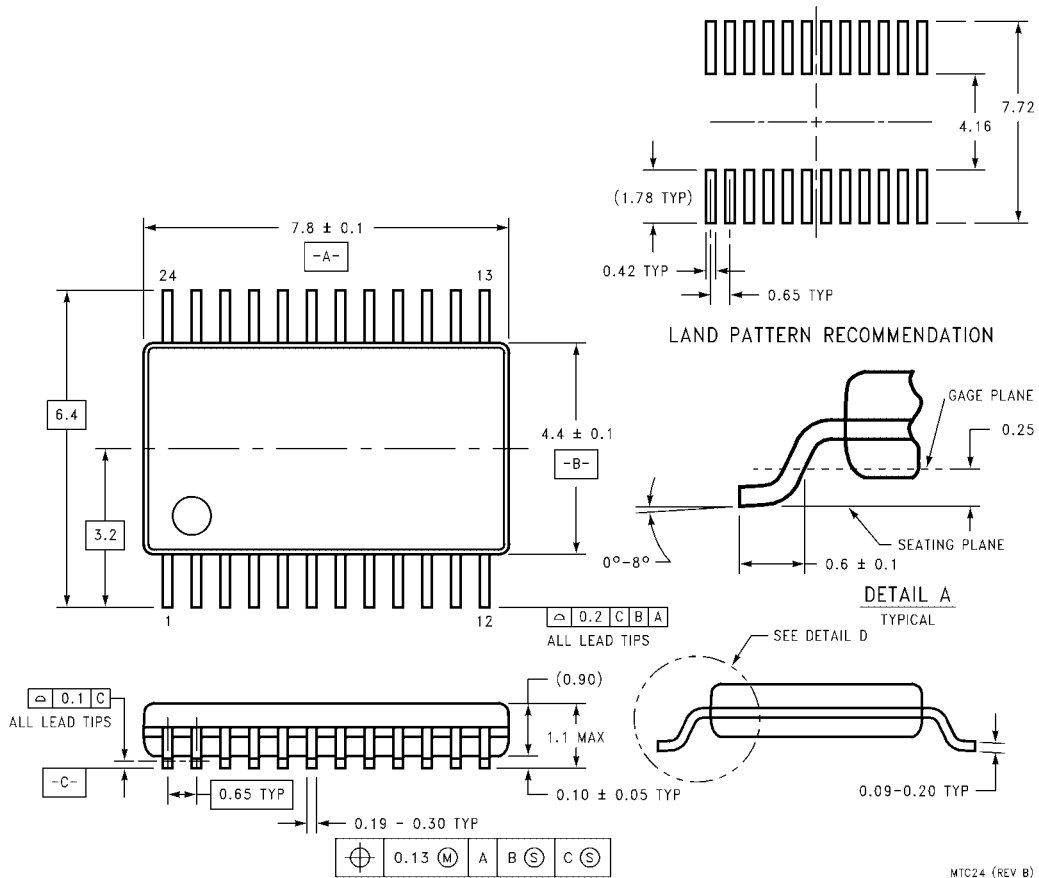


**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M24B**



**24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA24**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24**

MTC24 (REV B)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com