

NCP4672

Dual Linear Voltage Regulators with V_{in} and V_{out} Voltage Detector

The NCP4672 is a dual linear voltage regulator with input voltage and output voltage detectors. This part is useful in systems where multiple voltages are required such as for core and I/O. The NCP4672 is very accurate at 2% over full input voltage and full load current. The NCP4672 eliminates the need for external voltage supervision due to the two built in voltage detectors. The voltage detector on the input is set to 7.0 V. The output voltage detector is for channel 1 and is set to 2.9 V. An external capacitor is used to set the duration of this reset signal. Other features include short circuit protection and thermal shutdown protection. The NCP4672 has been designed to work with a 4.7 μF output capacitor having an ESR between 0.1 Ω and 5.0 Ω .

Features

- Accuracy: 2% at Full Voltage and Load
- Excellent Ripple Rejection: 70 dB @ 1 kHz
- Voltage Detector for Input Voltage
- Voltage Detector for Output Voltage
- Programmable Delay of Reset Signal
- Thermal Short Circuit Protection
- This is a Pb-Free Device

Typical Application

- Small Core and I/O Power
- Consumer Equipment
- Measurement Equipment
- Industrial Equipment

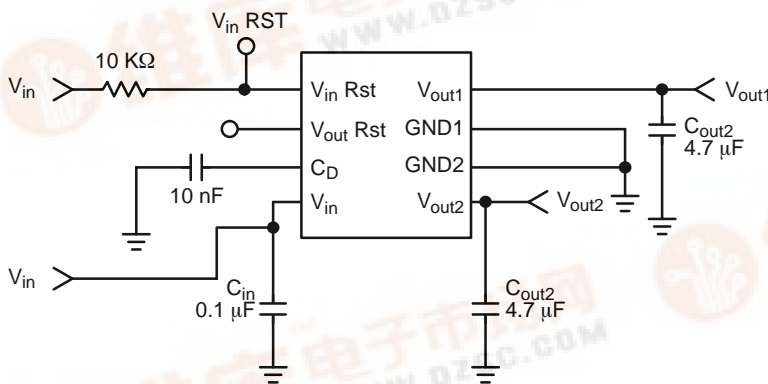


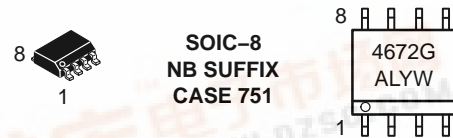
Figure 1. Typical Application Circuit



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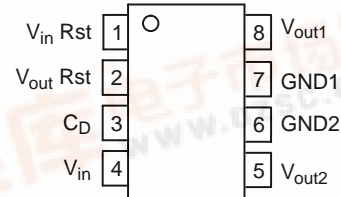
MARKING DIAGRAM



SOIC-8
NB SUFFIX
CASE 751

4672G = Specific Device Code
A = Assembly Location
L = Wafer Lot
YW = Date Code

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------|------------------|------------------|
| NCP4672DR2G | SOIC-8 (Pb-Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|--|-------------------------------|
| Input Voltage | V_{inmax} | -0.3 ~ 18 | V |
| Output Voltage | V_{out} | -0.3 to $V_{in} + 0.3$ | V |
| Output Current 1 Output Current 2 | $I_{out1max}$ $I_{out2max}$ | 30 80 | mA mA |
| Output Short Circuit Duration | – | Infinite | – |
| Power Dissipation and Thermal Characteristics – SOIC–8 Power Dissipation Thermal Resistance, Junction–to–Ambient Minimum Pad Size 200 mm ² Pad Size (Note 1) Thermal Resistance, Junction–to–Case | P_D $R_{\theta JA}$ $R_{\theta JC}$ | Internally Limited 190 160 25 | W °C/W °C/W °C/W |
| Operating Junction Temperature Range | T_{stg} | -40 to 125 | °C |
| Storage Temperature Range | T_{solder} | -55 to 150 | °C |

1. Refer to Figure 4 for more information.

PIN DESCRIPTION

| Pin Number | Symbol | Description |
|------------|--------------|---|
| 1 | $V_{in RST}$ | Open–collector, active–low output of the input voltage detector with hysteresis. Threshold levels are typical 7.0 V/ 7.35 V at V_{CC} pin. |
| 2 | $V_{o RST}$ | Active–low output of the reset generator. Reset generator is based on sensing of the V_{out1} voltage. Sensing is with hysteresis – threshold levels are typically 2.9 V/ 2.95 V at V_{out1} . Reset is generated at rising edge of the V_{out1} and it's duration is set by external capacitor connected to C_D pin. |
| 3 | C_D | Programmable delay of the reset generator. Delay is adjusted by inserting a capacitor between C_D and GND (typically 10 ms for 10 nF capacitor). |
| 4 | V_{CC} | Supply Voltage |
| 5 | V_{out2} | 1.8 V/ 80 mA LDO Regulator Output |
| 6 | GND2 | Ground for V_{out2} (internally connected with GND1) |
| 7 | GND1 | Ground for V_{out1} (internally connected with GND2) |
| 8 | V_{out1} | 3.5 V/30 mA LDO Regulator Output |

Recommended Conditions ($T_A = 25^\circ\text{C}$, $C_{in} = 0.1 \mu\text{F}$ Ceramic, $C_{out} = 4.7 \mu\text{F}$)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|--|--------------------------|--------|--------|----------|------|
| Input Voltage | V_{in} | 3.8 | 12 | 16 | V |
| Output Current (where V_{out} remains within accuracy) | I_{out1} I_{out2} | 0 0 | – – | 20 70 | mA |

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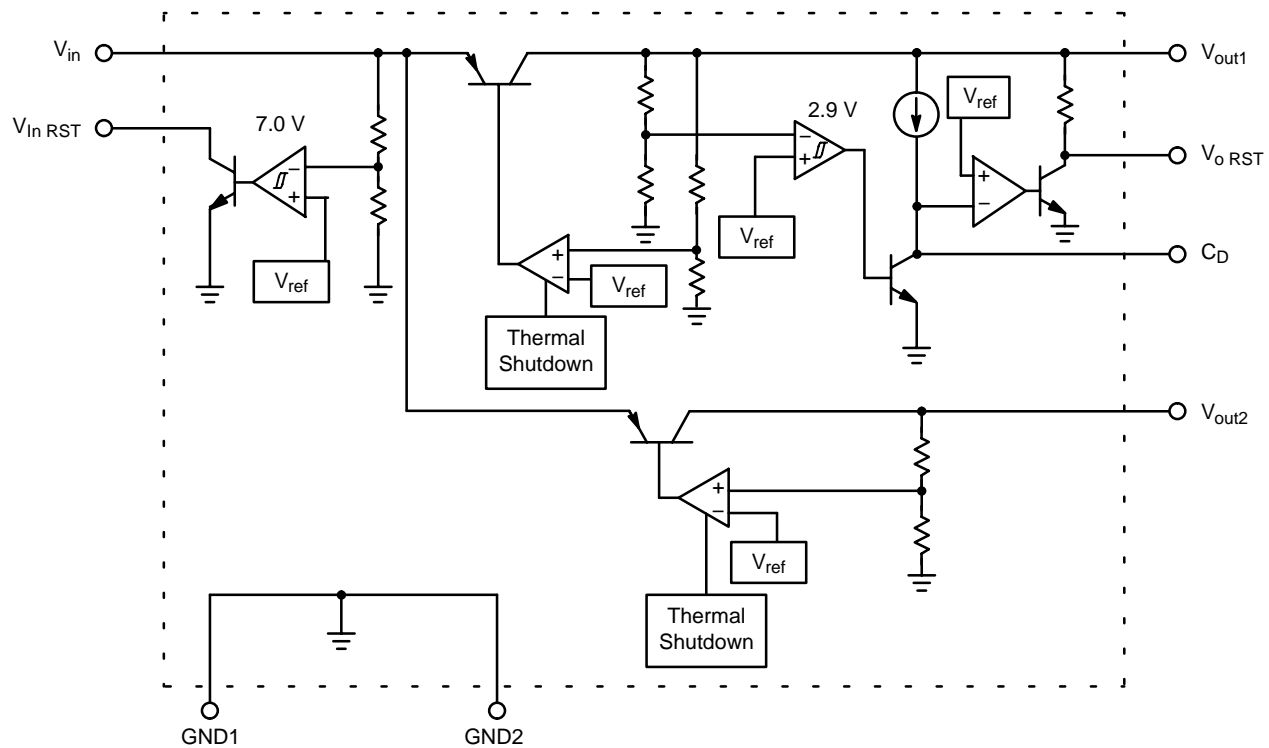


Figure 1.

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ELECTRICAL CHARACTERISTICS (C_{in} = 0.1 μF Ceramic, C_{out} = 4.7 μF with ESR = 0.1 – 5.0 Ω, V_{in} = 12 V, T_A = 25°C)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|-------------------------------------|---------------|------------|---------------|-------------------|
| Output Voltage V _{out1} (V _{in} = 4.5 V, I _{out1} = 20 mA) V _{out2} (V _{in} = 4.5 V, I _{out2} = 40 mA) | V _{adj} | 3.43 1.764 | 3.5 1.8 | 3.57 1.836 | V |
| Line Regulation V _{out1} (V _{in} = 4.5 V, I _{out1} = 20 mA) V _{out2} (V _{in} = 4.5 V to 10 V, I _{out2} = 40 mA) | Reg _{line} | – – | 3.0 3.0 | 30 30 | mV |
| Load Regulation V _{out1} (V _{in} = 4.5 V, I _{out1} = 0.1 mA to 20 mA) V _{out2} (V _{in} = 4.5 V, I _{out2} = 0.1 mA to 70 mA) | Reg _{load} | – – | 3.0 2.0 | 40 40 | mV |
| Dropout Voltage V _{out1} (V _{in} = 3.3 V, I _{out1} = 20 mA) | V _{in} – V _{out1} | – | 150 | 300 | mV |
| Ground Pin Current (V _{in} = 8.0 V, I _{out1} = I _{out2} = 0 mA) (V _{in} = 2.7 V, I _{out1} = I _{out2} = 0 mA, R _{pu} = infinite) | I _{GND} | – – | 1.0 3.0 | 2.0 – | mA |
| Short Current Limit V _{out1} V _{out2} | I _{SC} | 30 80 | 60 150 | – – | mA |
| Thermal Shutdown | | – | 165 | – | °C |
| Temperature Coefficient V _{out1} (T _J = –30 to 85°C, V _{in} = 4.5 V, I _{out1} = 20 mA) V _{out2} (T _J = –30 to 85°C, V _{in} = 4.5 V, I _{out2} = 40 mA) | T _C | – – | 100 100 | – – | ppm/°C |
| Ripple Rejection (Note 6) V _{out1} (V _{in} = 4.5 V, V _{ripple} = 1.0 V, I _{out1} = 20 mA, 120 Hz) V _{out2} (V _{in} = 4.5 V, V _{ripple} = 1.0 V, I _{out2} = 40 mA, 120 Hz) | R _R | – – | 65 70 | – – | dB |
| Output Noise Voltage V _{out1} (V _{in} = 4.5 V, f = 20 Hz – 80 kHz, I _{out1} = 20 mA) V _{out2} (V _{in} = 4.5 V, f = 20 Hz – 80 kHz, I _{out2} = 40 mA) | V _n | – – | 80 50 | – – | μV _{rms} |

V_{in} Detect

| | | | | | |
|---|----------------------------------|------|------|------|--------|
| Detecting Voltage L (V _{in} = H to L) | V _{SLin} | 6.72 | 7.0 | 7.28 | V |
| Detecting Voltage H (V _{in} = L to H) | V _{SHin} | – | 7.35 | – | V |
| Hysteresis Voltage (V _{in} = H to L to H) | Δ V _{Sin} | 140 | 350 | 560 | mV |
| V _{SLin} Temperature Coefficient (T _J = –30°C to +85°C) | V _{SLin} T _C | – | 100 | – | ppm/°C |
| Low-Level Output Voltage (V _{in} = 6.0 V, V _{t1} = 5.0 V, R _{t1} = 10 kΩ) (Note 5) | V _{OLin1} | – | 100 | 200 | mV |
| Threshold Operating Voltage (V _{OPLin} = V _{t1} = 1.0 V) | V _{OLin2} | – | – | 0.4 | V |

V_{out} Detect

| | | | | | |
|---|----------------------------------|------|------|-------|--------|
| Detecting Voltage L (V _{in} = H to L) | V _{SLout} | 2.78 | 2.9 | 3.020 | V |
| Detecting Voltage H (V _{in} = L to H) | V _{SHout} | – | 2.95 | – | V |
| Hysteresis Voltage (V _{in} = H to L to H) | Δ V _{Sout} | 25 | 50 | 100 | mV |
| V _{SLin} Temperature Coefficient (T _J = –30°C to +85°C) | V _{SLin} T _C | – | 100 | – | ppm/°C |
| Low-Level Output Voltage (V _{out1} = 2.6 V) | V _{OLout1} | – | 100 | 200 | mV |
| Threshold Operating Voltage (V _{OPLout} = 0.85 V) | V _{OLout2} | – | – | 0.4 | V |
| Reset Delay Time (C _D = 10 nF) | t _{PLH} | 5 | 10 | 15 | ms |
| “L” Transmission Delay Time (C _D = 10 nF) | t _{PHL} | – | 30 | 90 | μs |

2. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V.

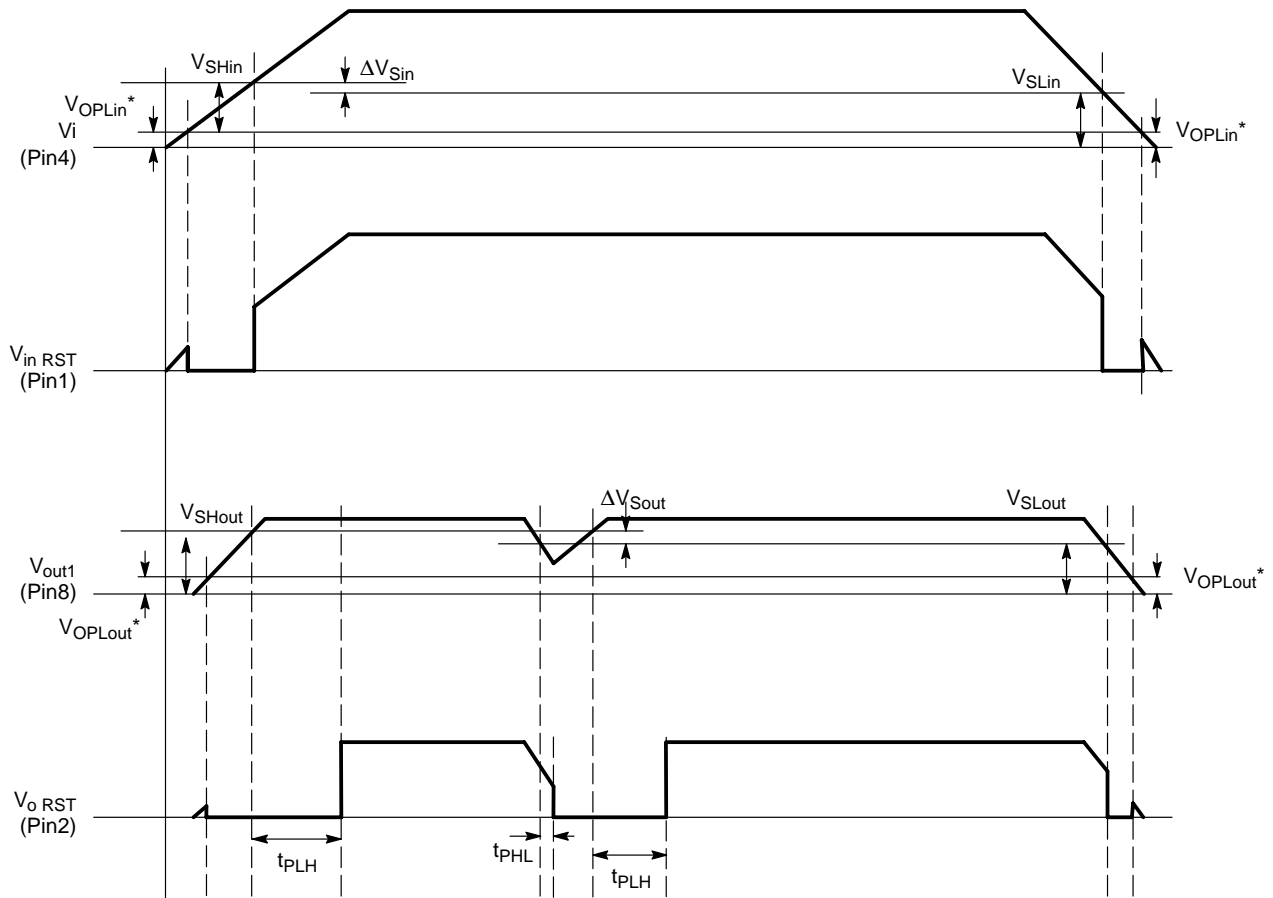
3. The maximum package power dissipation is: $P_D = \frac{T_J(\max) - T_A}{R_{\theta JA}}$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

5. Refer to Figure 3.

6. Guaranteed by design.

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*; V_{OPLin} shows theoretical on this chart.

V_{OPLin} spec. must be specified on Pin 1 voltage (0.4 V)

*; V_{OPLout} shows theoretical on this chart.

V_{OPLout} spec. must be specified on Pin 2 voltage (0.4 V)

Figure 2. Dual Regulator Timing

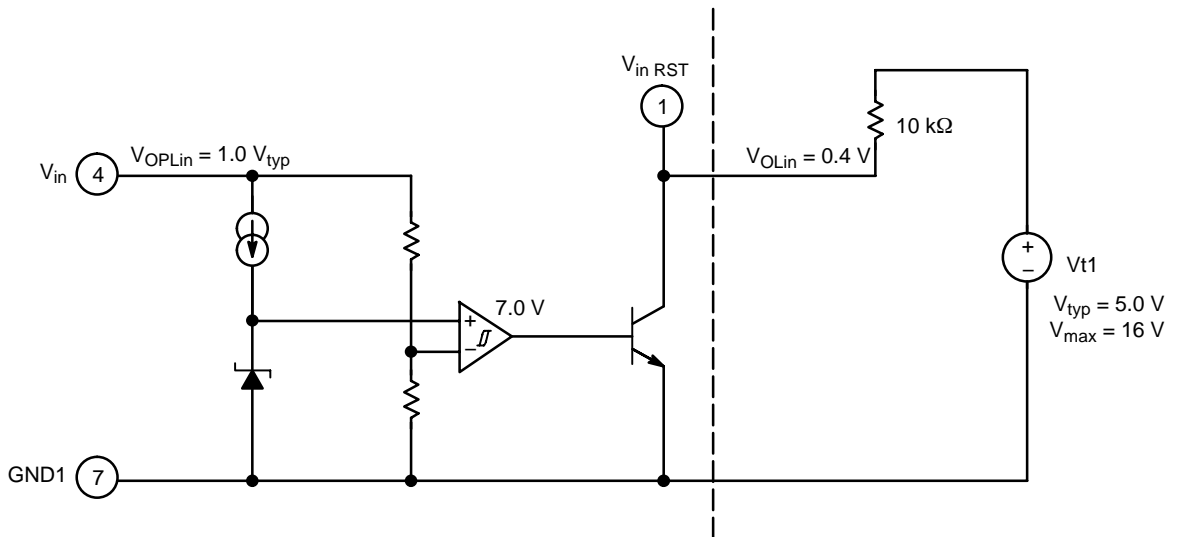


Figure 3. Threshold Operating Voltage V_{OPLin} Under Condition $V_{OLin} = 0.4$ V

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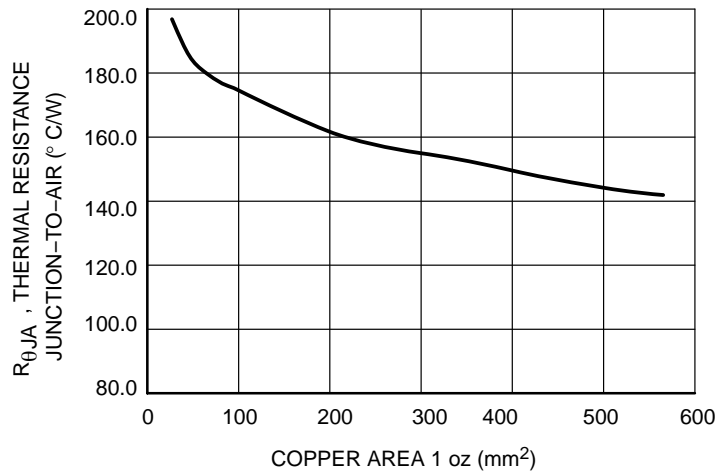


Figure 4. SOP-8 Thermal Resistance versus P.C.B. Copper Area

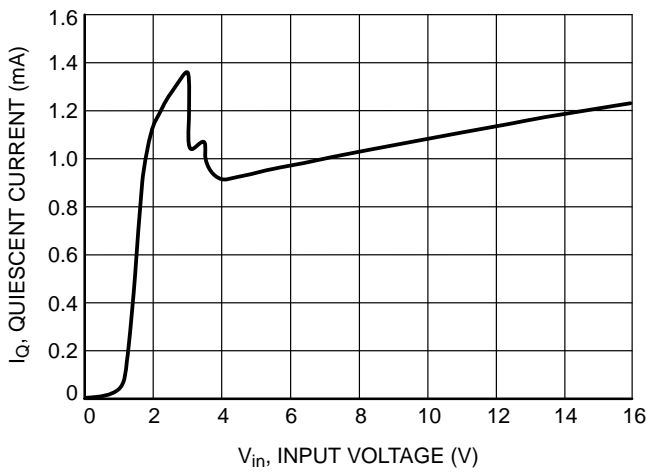


Figure 5. Quiescent Current versus Input Voltage

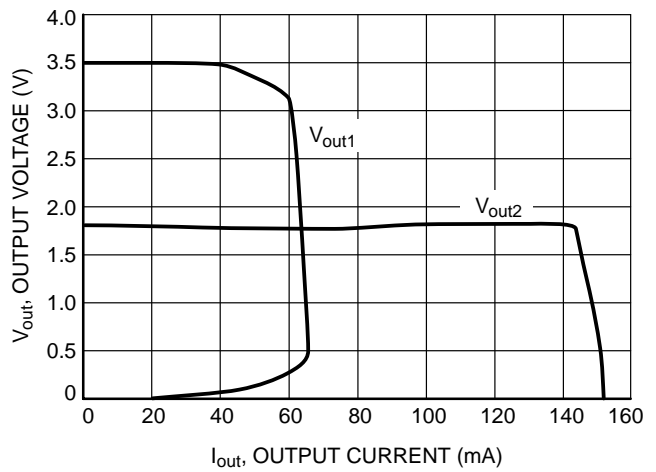


Figure 6. Peak Current Limit

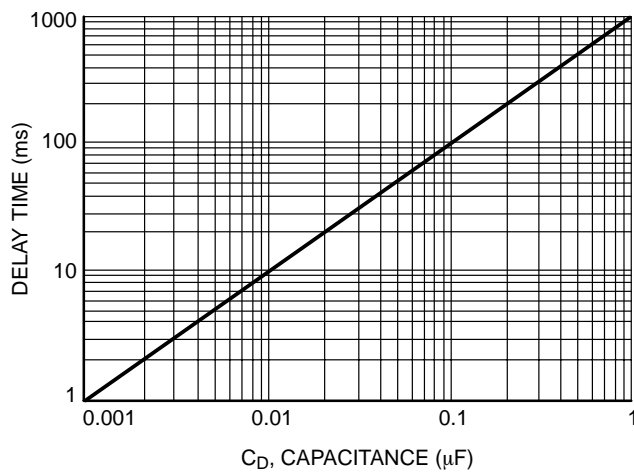


Figure 7. Delay Time versus Capacitance

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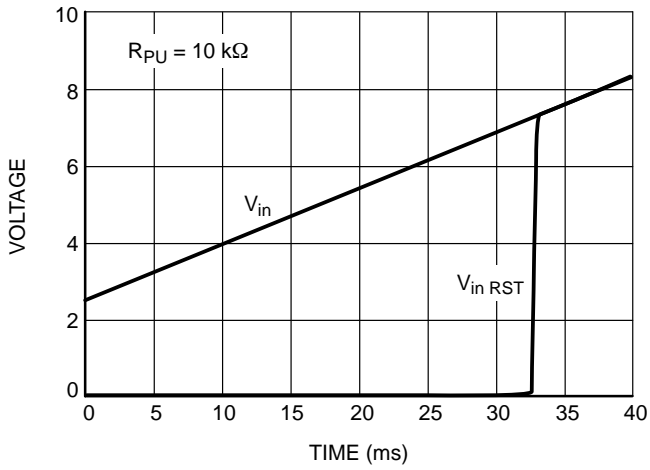


Figure 8. V_{in} and $V_{in\ RST}$ versus Time

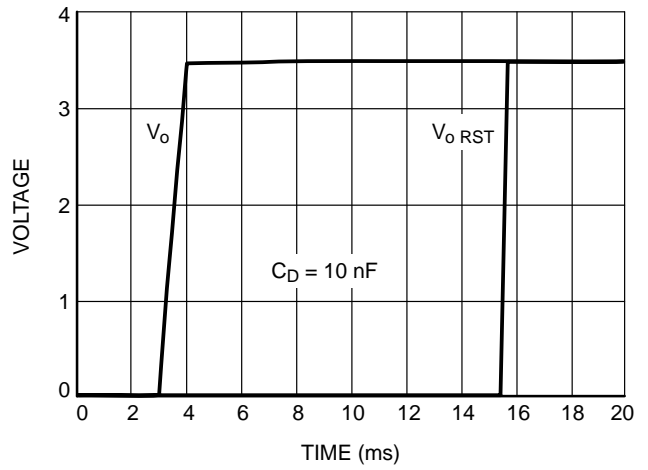


Figure 9. V_o and $V_o\ RST$ versus Time

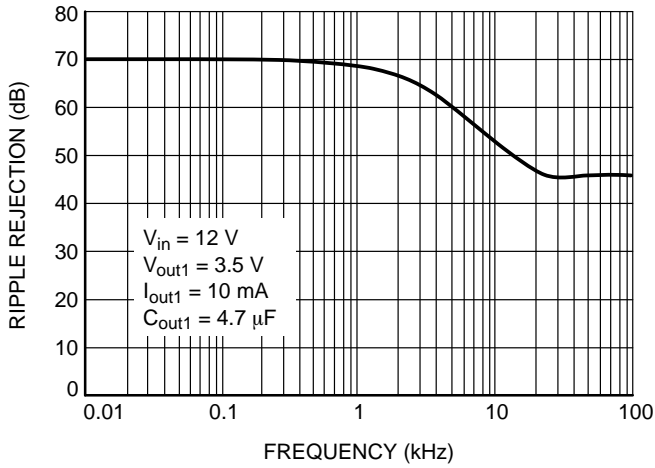


Figure 10. V_{out1} Ripple Rejection

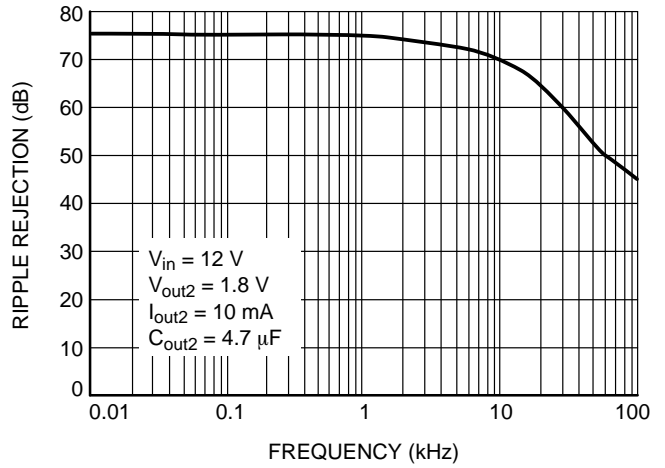
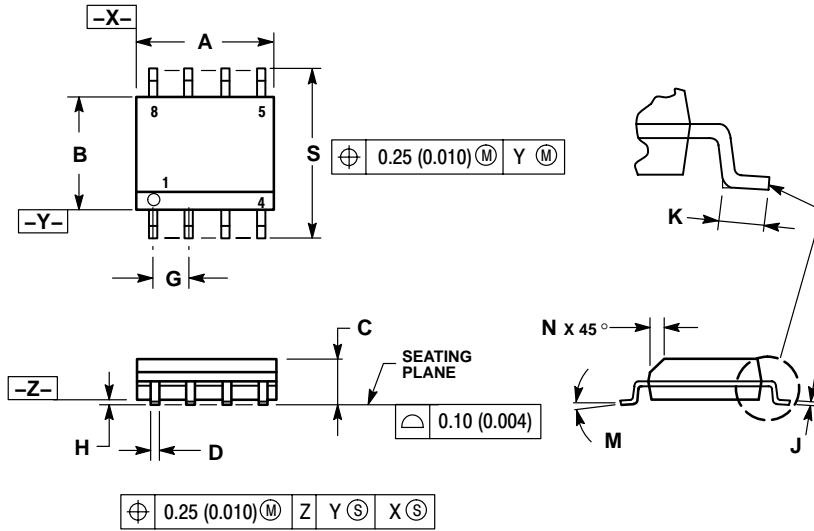


Figure 11. V_{out2} Ripple Rejection

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PACKAGE DIMENSIONS

SOIC-8
NB SUFFIX
 CASE 751-07
 ISSUE AB

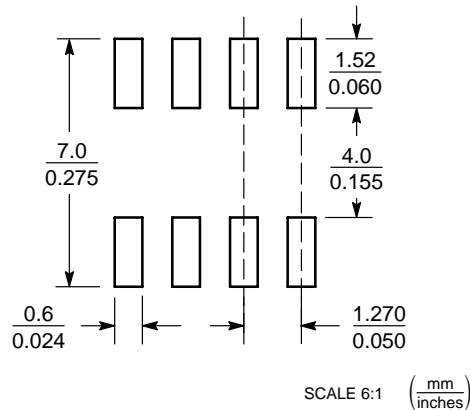


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



SOIC-8

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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