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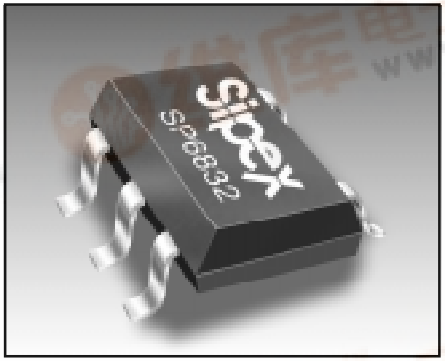
Sipex

SP6832

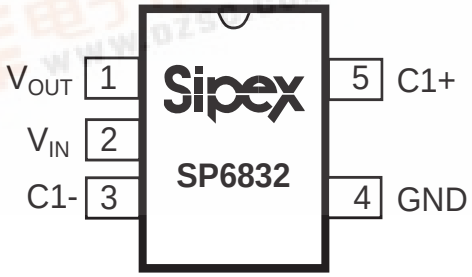
High Speed, High Efficiency Voltage Inverter

- 99.9% Voltage Conversion Efficiency
- +1.15V to +5.3V Input Voltage Range
- +1.15 V_{IN} Guaranteed Start-up
- Inverts Input Supply Voltage
- 700µA Quiescent Current
- 25mA Output Current
- 500kHz Operating Frequency
- Ideal for +3.6V Lithium Ion Battery Applications
- Reverse Battery Protection
- 5-pin SOT23 Package
- 19Ω Output Resistance
- 0.1 or 0.33 µF Capacitors



DESCRIPTION

The SP6832 device is a CMOS Charge Pump Voltage Inverter that can be implemented in designs requiring a negative voltage from a positive source as low as 1.15V. The SP6832 device is ideal for both battery-powered and board level voltage conversion applications with a typical operating current of 700mA at a 5V supply. The SP6832 can output 25mA with a voltage drop of 500mV. These devices combine a low quiescent current with high efficiency of 85-90% over most of its load range. Applications include cell phones, PDAs, medical instruments and other portable equipment. The SP6832 is available in a space-saving 5-pin SOT23 Package.



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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{IN}.....-0.3V to +5.6V
V_{OUT}.....-5.6V to +0.3V
V_{OUT} Short Circuit to GND.....Indefinite
I_{OUT}.....50mA
Storage Temperature.....-65˚C to +150˚C
Power Dissipation per Package
5-pin SOT (derate 4.35mW/°C above +70°C).....400mW
Lead Temperature (Soldering).....300°C
ESD Rating.....2kV Human Body Model

CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS FOR THE SP6832

V_{IN} = +5.0V, C1 = C2 = C3 = 0.33µF and T_{AMB} = 25°C unless otherwise noted. The circuit found in ***Figure 14*** was used to obtain the following typical performance characteristics (unless otherwise noted).

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Minimum Voltage Supply Voltage	 1.4	0.86	1.15 5.3	V	R_L=10kΩ, T_{AMB}=+25° C, Note 1 R_L=10kΩ, T_{AMB}=-40° C to +85° C
Supply Currrent		0.7	1.4	mA	T_{AMB} = -40°C to +85°C, RL = ∞
Output Resistance		19	45	Ω	I_{OUT} = 5mA to 25mA, Note 2
Oscillator Frequency	300	500	750	kHz	
Voltage Conversion Efficiency	95	99.9		%	R_L = ∞
Power Efficiency (Ideal)		97		%	I_{OUT} = 5mA, Note 3
Power Efficiency (Actual)		87		%	I_{OUT} = 5mA, Note 4

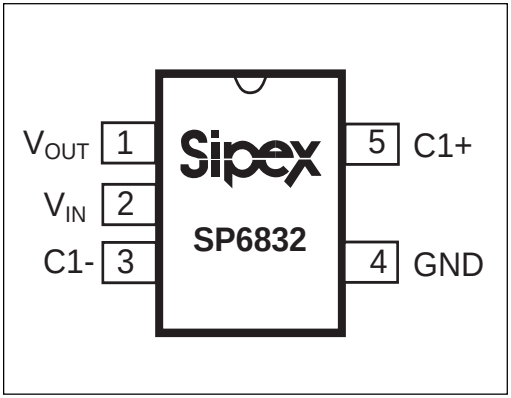
NOTE 1: $V_{OUT} = -V_{IN} + 200mV$

NOTE 2: Capacitors are approximately 20% of the output impedance where $ESR = \frac{1}{f_{OSC} \times C}$

NOTE 3: Power Efficiency (Ideal) = $\frac{V_{OUT} \times I_{OUT}}{-V_{IN} \times (-V_{IN}/R_L)}$

NOTE 4: Power Efficiency (Actual) = $\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$

PINOUT



PIN ASSIGNMENTS

Pin 1— V_{OUT} — Inverting charge pump output.

Pin 2 — V_{IN} — Input to the positive power supply.

Pin 3 — C1- — Negative terminal to the charge pump capacitor.

Pin 4 — GND — Ground reference.

Pin 5 — C1+ — Positive terminal to the charge pump capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +5.0V, C1 = C2 = C3 = 0.33µF and T_{AMB} = 25°C unless otherwise noted. The circuit found in ***Figure 14*** was used to obtain the following typical performance characteristics (unless otherwise noted).

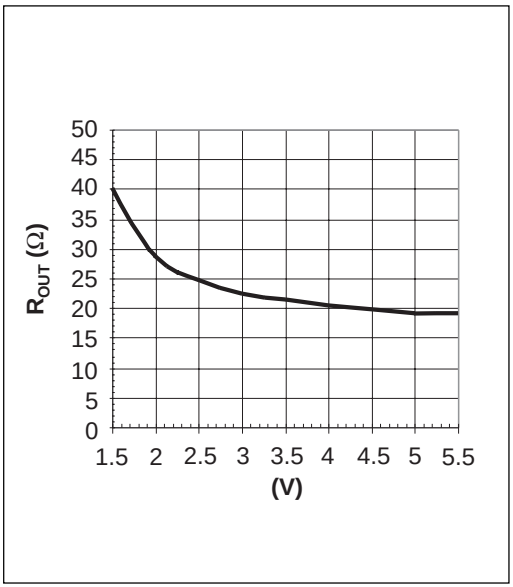


Figure 1. Output Resistance vs. Supply Voltage with a 5mA load

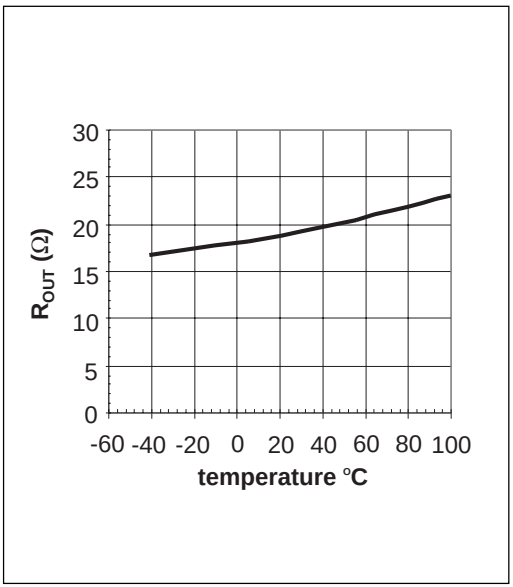


Figure 2. Output Resistance vs. Temperature with a 25mA load

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +5.0V, C1 = C2 = C3 = 0.33µF and T_{AMB} = 25°C unless otherwise noted. The circuit found in ***Figure 14*** was used to obtain the following typical performance characteristics (unless otherwise noted).

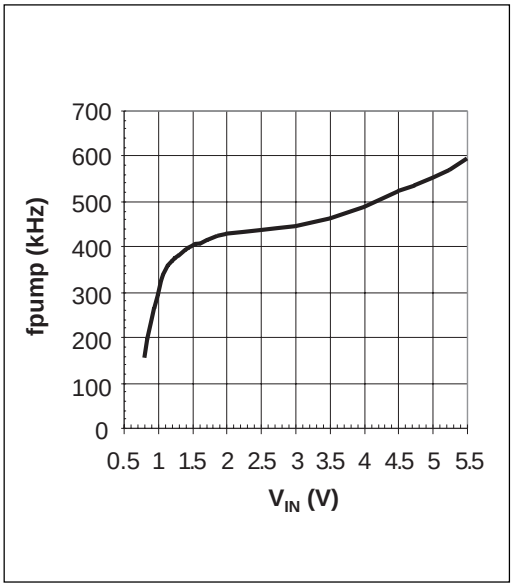


Figure 3. Charge Pump Frequency vs. Supply Voltage

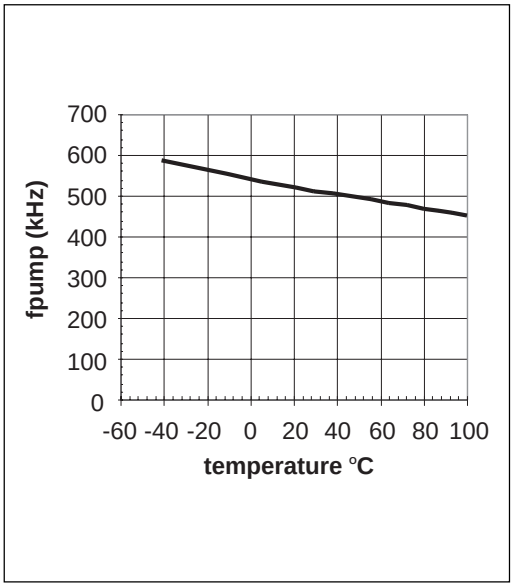


Figure 4. Charge Pump Frequency vs. Temperature

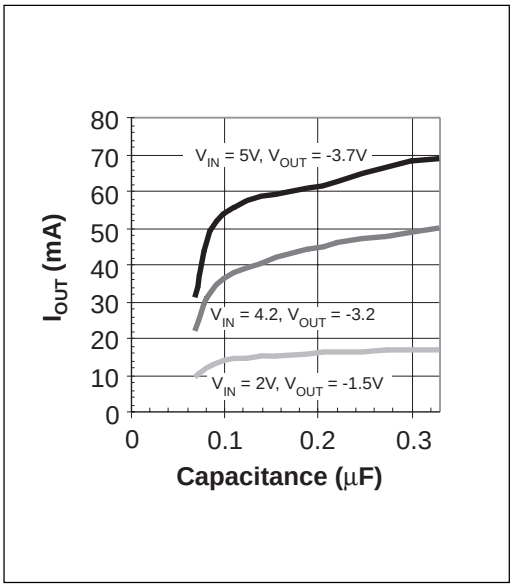


Figure 5. Output Current vs. Capacitance

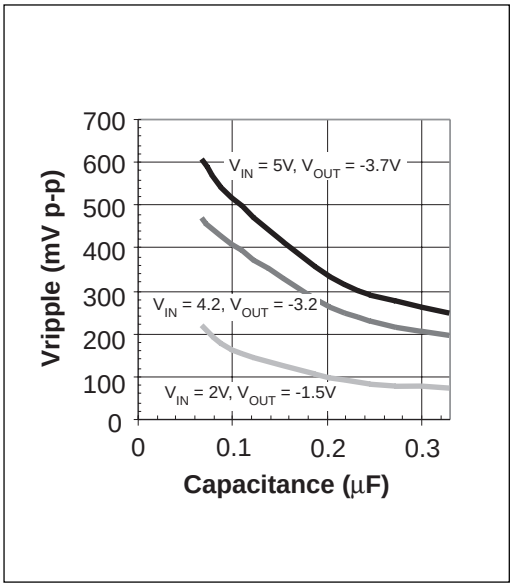


Figure 6. Output Voltage Ripple vs. Capacitance

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +5.0V, C1 = C2 = C3 = 0.33µF and T_{AMB} = 25°C unless otherwise noted. The circuit found in ***Figure 14*** was used to obtain the following typical performance characteristics (unless otherwise noted).

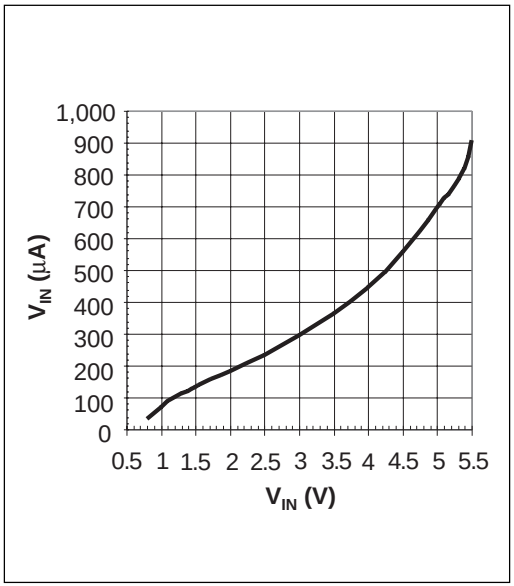


Figure 7. Supply Current vs. Supply Voltage

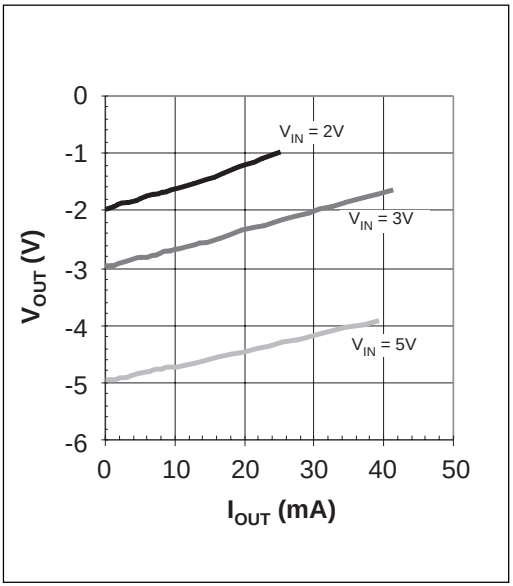


Figure 8. Output Voltage vs. Output Current with 0.1µF Capacitors

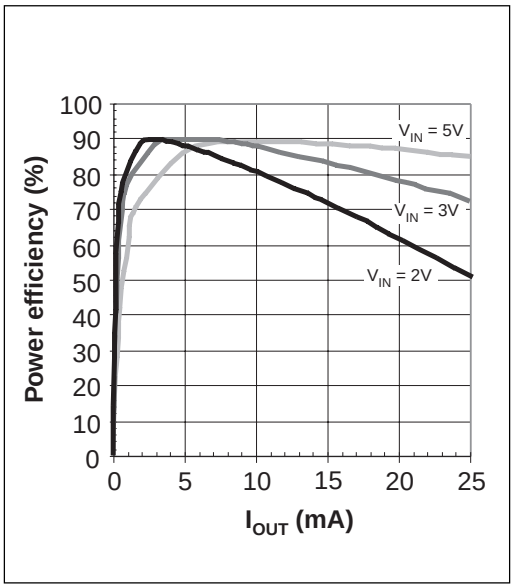


Figure 9. Power Efficiency vs. Output Current with 0.1µF Capacitors

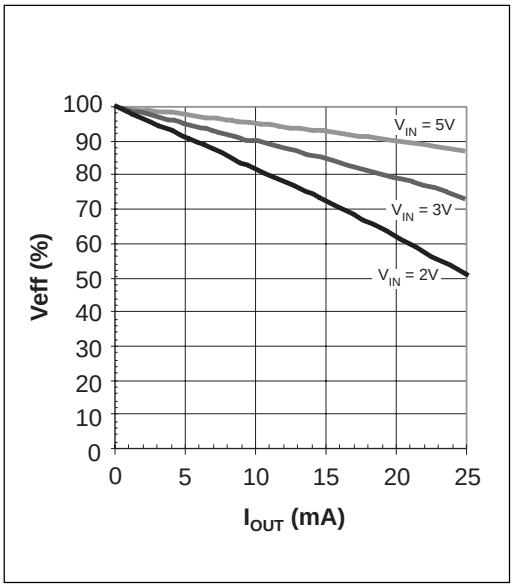


Figure 10. Voltage Efficiency vs. Output Current with 0.1µF Capacitors

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +5.0V, C1 = C2 = C3 = 0.33µF and T_{AMB} = 25°C unless otherwise noted. The circuit found in ***Figure 14*** was used to obtain the following typical performance characteristics (unless otherwise noted).

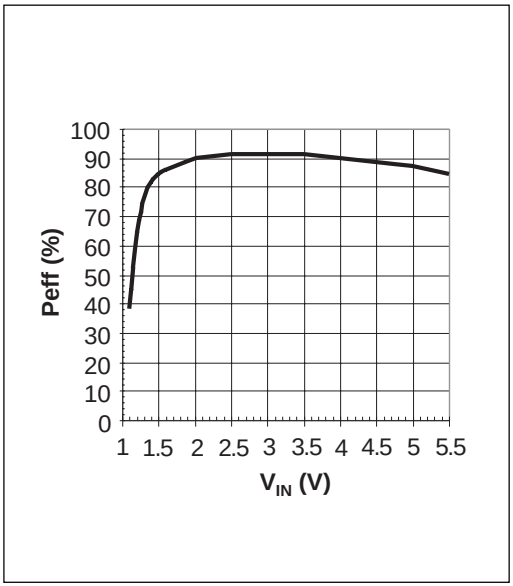


Figure 11. Power Efficiency vs. Supply Voltage with a 5mA load

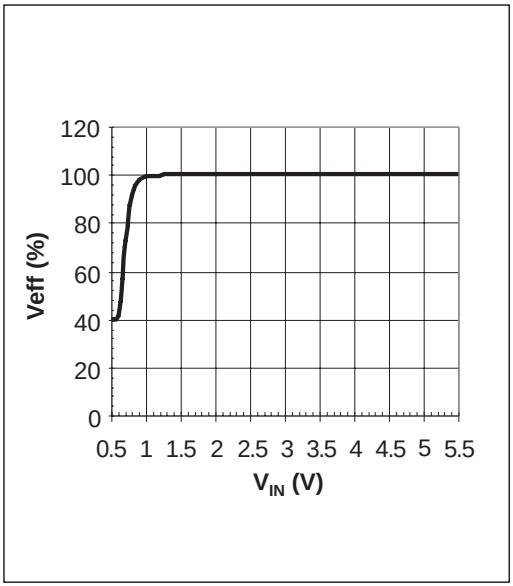


Figure 12. Voltage efficiency vs. Supply Voltage without a Load with 0.1µF Capacitors

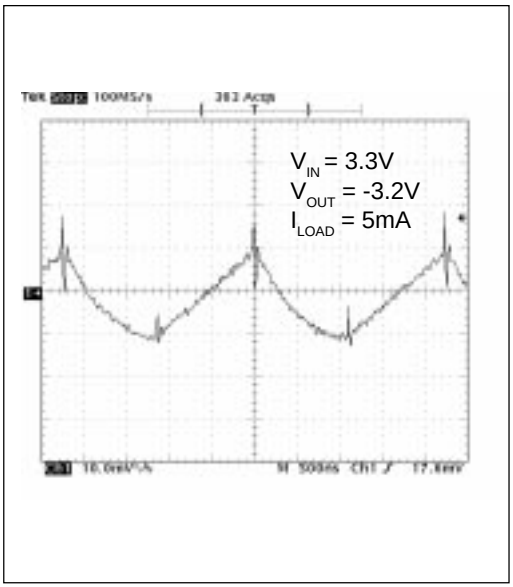


Figure 13. Output Noise and Ripple

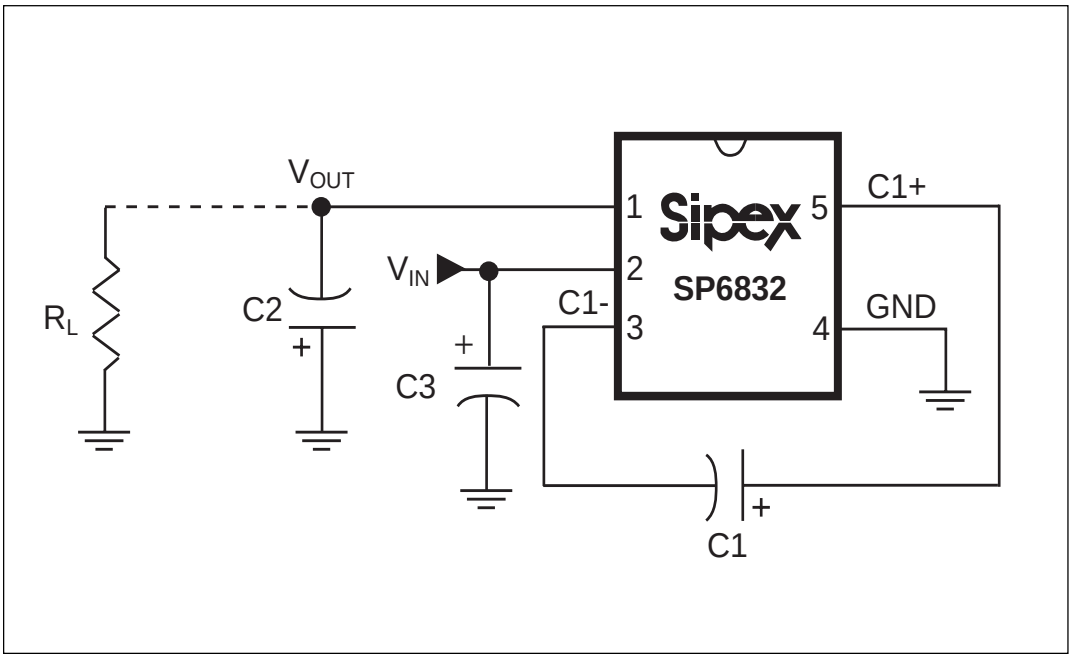


Figure 14. SP6832 in its Typical Operating Circuit as a Negative Voltage Converter; this Circuit Was Used to Obtain the Typical Performance Characteristics Found in Figures 1 Through 13 (unless otherwise noted)

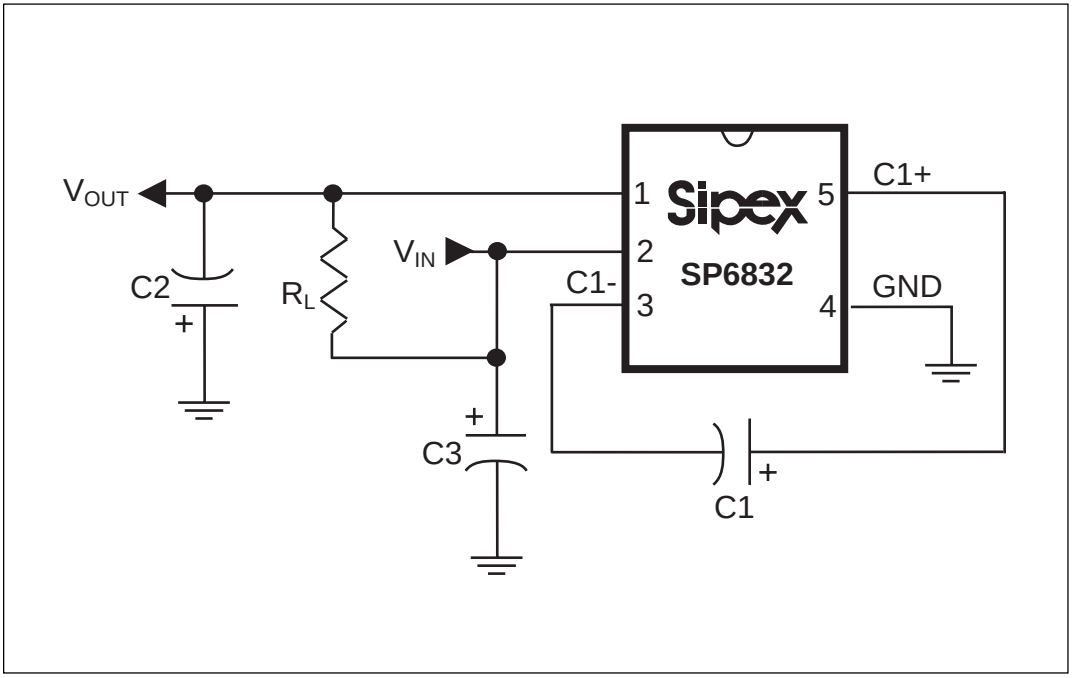


Figure 15. SP6832 Connected as a Voltage Inverter with the load from V_{OUT} to V_{IN}

DESCRIPTION

The **SP6832** is a CMOS Charge Pump Voltage Converter that can be used to invert a +1.15V to +5.3V input voltage. These devices are ideal for designs involving battery-powered and/or board level voltage conversion applications.

The typical operating frequency of the **SP6832** is 500kHz. The **SP6832** has a typical operating current of 800µA. The device can output 25mA with a voltage drop of 500mV. The devices are ideal for designs using +3.3V or +3.6V lithium ion batteries such as cell phones, PDAs, medical instruments, and other portable equipment. The **SP6832** combines a high efficiency with a low quiescent current.

THEORY OF OPERATION

The **SP6832** should theoretically produce an inverted input voltage. In real world applications, there are small voltage drops at the output that reduce efficiency. The circuit of an ideal voltage inverter can be found in ***Figure 16***. The voltage inverters require two external capacitors to store the charge. A description of the two phases follows:

Phase 1

In the first phase of the clock cycle, switches S1 and S3 are opened and S2 and S4 are closed. This connects the flying capacitor, C1, from V_{IN} to ground. C1 charges up to the input voltage applied at V_{IN}.

Phase 2

In the second phase of the clock cycle, switches S1 and S3 are opened and S2 and S4 are closed. This connects the flying capacitor, C1, in parallel with the output capacitor, C2. The charge stored in C1 is now transferred to C2. Simultaneously, the negative side of C2 is connected to V_{OUT} and the positive side is connected to ground. With the voltage across C2 smaller than the voltage across C1, the charge flows from C1 to C2 until the voltage at the V_{OUT} equals $-V_{IN}$.

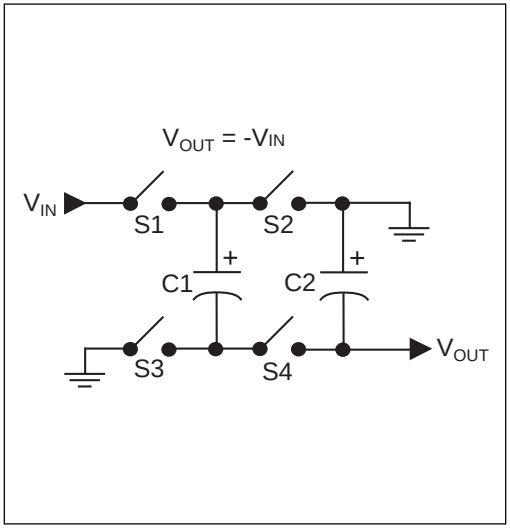


Figure 16. Circuit for an Ideal Voltage Inverter

Charge-Pump Output

The output of the **SP6832** is not regulated and therefore is dependent on the output resistance and the amount of load current. As the load current increases, losses may slightly increase at the output and the voltage may become slightly more positive. The loss at the negative output, V_{LOSS}, equals the current draw, I_{OUT}, from V_{OUT} times the negative converter's source resistance, R_S:

$$\mathbf{V_{LOSS} = I_{OUT} \times R_S.}$$

The actual inverted output voltage at V_{OUT} will equal the inverted voltage difference of V_{IN} and V_{LOSS}:

$$\mathbf{V_{OUT} = -(V_{IN} - V_{LOSS}).}$$

Efficiency

Theoretically, the total power loss of a switched capacitor voltage converter can be summed up as follows:

$$\mathbf{\sum P_{LOSS} = P_{INT} + P_{CAP} + P_{CONV},}$$

where P_{LOSS} is the total power loss, P_{INT} is the total internal loss in the IC including any losses in the MOSFET switches, P_{CAP} is the resistive loss of

the charge pump capacitors, and P_{CONV} is the total conversion loss during charge transfer between the flying and output capacitors. These are the three theoretical factors that may effect the power efficiency of the **SP6832** in designs.

Internal losses come from the power dissipated in the IC's internal circuitry.

Losses in the charge pump capacitors will be induced by the capacitors' ESR. The effects of the ESR losses and the output resistance can be found in the following equation:

$$I_{OUT}^2 \times R_{OUT} = P_{CAP} + P_{CONV}$$

and

$$R_{OUT} \approx 4 \times (2 \times R_{SWITCHES} + ESR_{C1}) + ESR_{C2} + \frac{1}{f_{OSC} \times C1},$$

where I_{OUT} is the output current, R_{OUT} is the circuit's output resistance, $R_{SWITCHES}$ is the internal resistance of the MOSFET switches, ESR_{C1} and ESR_{C2} are the ESR of their respective capacitors, and f_{OSC} is the oscillator frequency. This term with f_{OSC} is derived from an ideal switched-capacitor circuit as seen in ***Figure 17***.

Conversion losses will happen during the charge transfer between the flying capacitor, C1, and the output capacitor, C2, when there is a voltage difference between them. P_{CONV} can be determined by the following equation:

$$P_{CONV} = f_{OSC} \times [\, {}^1/_2 \times C1 \times (V_{IN}^2 - V_{OUT}^2) + {}^1/_2 \times C2 \times (V_{RIPPLE}^2 - 2 \times V_{OUT} \times V_{RIPPLE}) \,].$$

Actual Efficiency

To determine the actual efficiency of the **SP6832** device operation, a designer can use the following equation:

$$\text{Efficiency (ACTUAL)} = \frac{P_{OUT}}{P_{IN}} \times 100\%,$$

where

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

and

$$P_{IN} = V_{IN} \times I_{IN}$$

where P_{OUT} is the power output, V_{OUT} is the output voltage, I_{OUT} is the output current, P_{IN} is the power from the supply driving the **SP6832**, V_{IN} is the supply input voltage, and I_{IN} is the supply input current.

Ideal Efficiency

The ideal efficiency is not the true power efficiency because it is not calculated relative to the input power which includes the input current losses in the charge pump. The ideal efficiency can be determined with the following equation:

$$\text{Efficiency (IDEAL)} = \frac{P_{OUT}}{P_{OUT\,(IDEAL)}} \times 100\%,$$

where

$$P_{OUT\,(IDEAL)} = -V_{IN} \times \frac{-V_{IN}}{R_L},$$

and P_{OUT} is the measured power output. Both efficiencies are provided to designers for comparison.

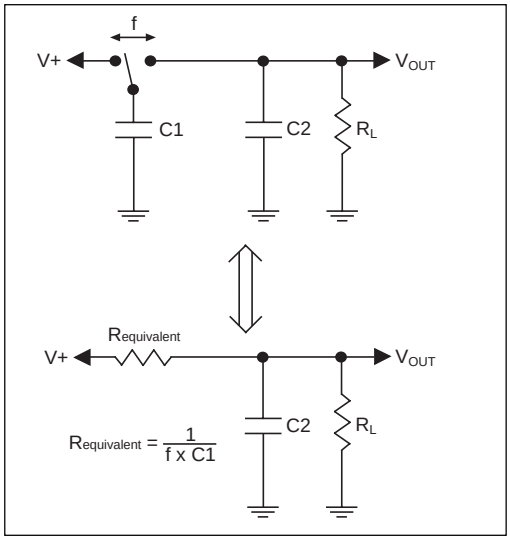


Figure 17. Equivalent Circuit for an Ideal Switched Capacitor

APPLICATION INFORMATION

For the following applications, C1 = C2 = 0.1µF

Capacitor Selection

Low ESR capacitors are needed to obtain low output resistance. Refer to ***Table 1*** for some suggested low ESR capacitors. The output resistance of the **SP6832** is a function of the ESR of C1 and C2. This output resistance can be determined by the equation previously provided in the **Efficiency** section:

$$R_{OUT} \approx 4 \times (2 \times R_{SWITCHES} + ESR_{C1}) + ESR_{C2} + \frac{1}{f_{OSC} \times C1},$$

where R_{OUT} is the circuit output resistance, $R_{SWITCHES}$ is the internal resistance of the MOSFET switches, ESR_{C1} and ESR_{C2} are the ESR of their respective capacitors, and f_{OSC} is the oscillator frequency. This term with f_{OSC} is derived from an ideal switched-capacitor circuit as seen in ***Figure 21***.

Minimizing the ESR of C1 and C2 will minimize the total output resistance and will improve the efficiency.

Flying Capacitor

Decreasing flying capacitor, C1, values will increase the output resistance of the **SP6832** while increasing C1 will reduce the output resistance. There is a point where increasing C1 will have a negligible effect on the output resistance due to the domination of the output resistance by the internal MOSFET switch resistance and the total capacitor ESR.

Output Capacitor

Increasing output capacitor, C2, values will decrease the output ripple voltage. Reducing the ESR of C2 will reduce both output ripple voltage and output resistance. If higher output ripple can be tolerated in designs, smaller capacitance values for C2 should be used with light loads. The following equation can be used to calculate the peak-to-peak ripple voltage:

$$V_{RIPPLE} = 2 \times I_{OUT} \times ESR_{C2} + \frac{I_{OUT}}{f_{OSC} \times C2}.$$

Input Bypass Capacitor

The bypass capacitor at the input pin will reduce AC impedance and the impact of any of the **SP6832** devices' switching noise. It is recommended that for heavy loads a bypass capacitor approximately equal to the flying capacitor, C1, be used. For light loads, the value of the bypass capacitor can be reduced.

When loading the **SP6832** devices from IN to OUT, the input current remains constant (disregarding any spikes due to internal switching). Implementing a 0.1µF bypass capacitor should be sufficient.

When loading the **SP6832** devices from OUT to GND, the current from the supply will flow into the input for half of the cycle and will be zero for the other half of the cycle. Designers should implement a large bypass capacitor if the supply has a high AC impedance.

Negative Voltage Converter

The typical operating circuit for the **SP6832** devices is a negative voltage converter. Refer to ***Figure 14***. This circuit is used to obtain the Typical Performance Characteristics found in ***Figures 1*** to ***13*** (unless otherwise noted).

Voltage Inverter with the Load from V_{OUT} to V_{IN}

A designer can find the most common application for the **SP6832** devices in ***Figure 15*** as a voltage inverter. The only external components needed are 3 capacitors: the flying capacitor, C1, the output capacitor, C2, and the bypass capacitor, C3 (if necessary).

Driving Excessive Loads

The output should never be pulled above ground. A designer should implement a Schottky diode (1N5817) from OUT to GND when driving heavy loads where a higher supply is sourcing current into OUT. Refer to ***Figure 18*** for this circuit connection.

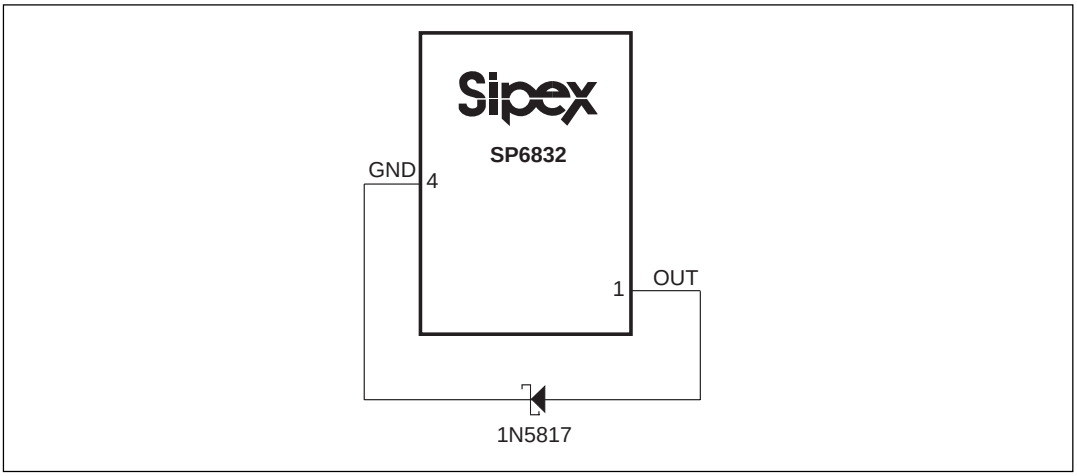


Figure 18. Protection for Heavy Loads

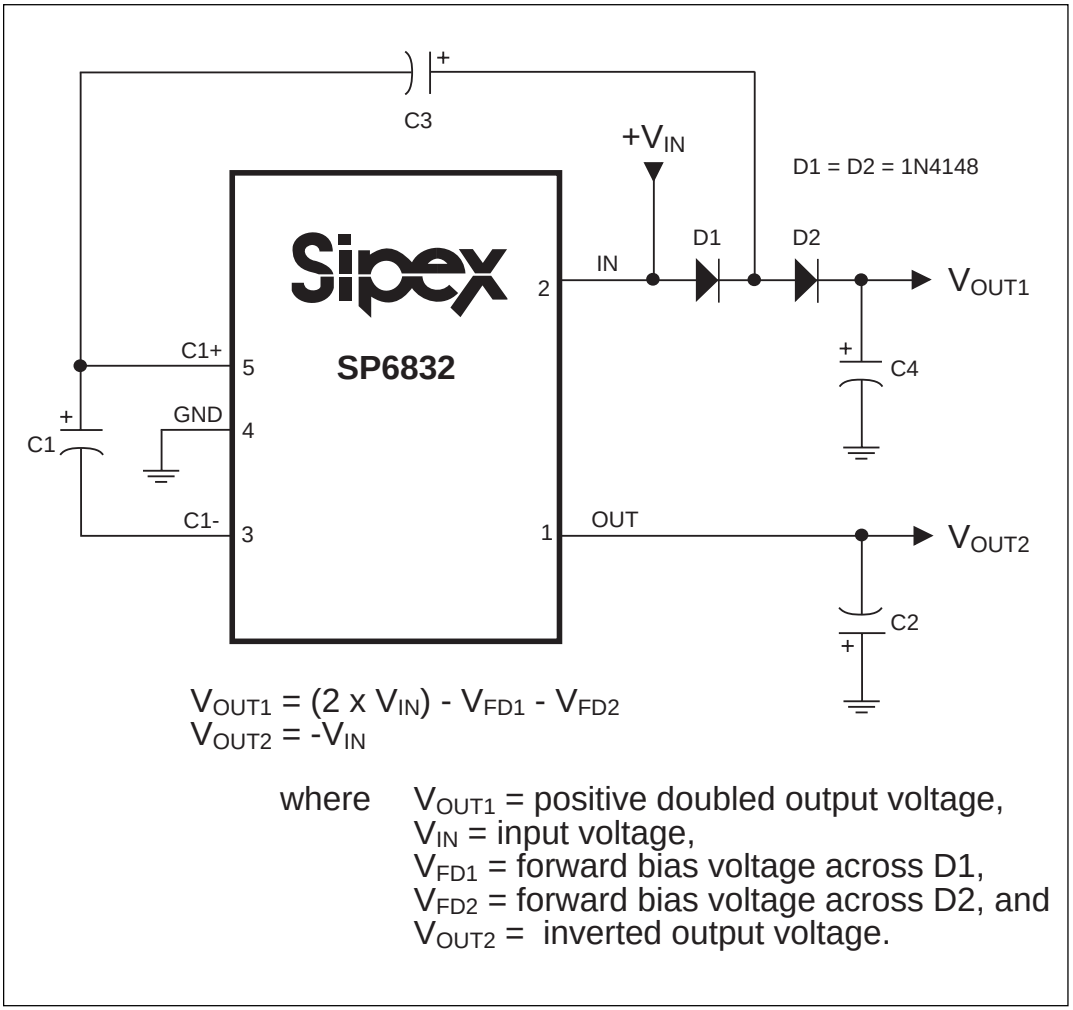


Figure 19. SP6832 Device Connected in a Doubler/Inverter Combination Circuit

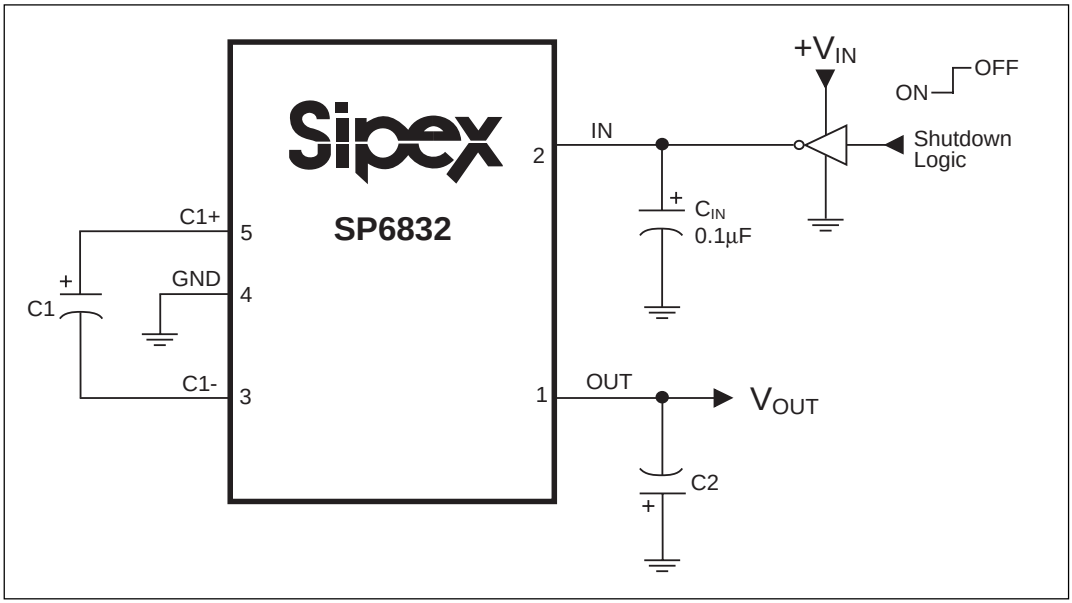


Figure 20. SP6832 Device with Shutdown Control

Combining a Doubler and Inverter Circuit

A designer can connect a **SP6832** device in a combination doubler/inverter circuit as seen in ***Figure 19***. The doubler uses capacitors C3 and C4 while the inverter uses C1 and C2. Loading either output decreases both output voltages to GND because both the doubler and the inverter circuits use the charge pump. Designers should not allow the total current output from the doubler and the inverter to exceed 40mA.

Implementing Shutdown

If shutdown control of the **SP6832** devices is necessary, the circuit found in ***Figure 20*** can be implemented. The 0.1µF capacitor at IN absorbs transient input currents. The output resistance of the devices can be determined by the following equation:

$$\mathbf{R_{OUT} = 20 + 2 \times R_{BUFFER}},$$

where R_{OUT} is the output resistance and R_{BUFFER} is the output resistance of the buffer driving IN. R_{BUFFER} can be reduced by connecting multiple buffers in parallel at IN. The polarity of the SHUTDOWN signal can be changed by using a noninverting buffer to drive IN.

Connecting in Parallel

A designer can parallel a number of **SP6832** devices to reduce the output resistance for specific designs. All devices will need their own flying capacitor, C1, but a single output capacitor will serve all of the devices connected in parallel by increasing the capacitance of C2 by a factor of n where n equals the total number of devices connected. This connection can be found in ***Figure 21***.

Cascading Devices

A designer can cascade **SP6832** devices to produce a larger inverted voltage output. Refer to ***Figure 22*** for this circuit connection. With two cascaded devices, the unloaded output voltage is decreased by the output resistance of the first device multiplied by the quiescent current of the second device connected. The total output resistance is greatly increased when more than two devices are cascaded.

Layout and Grounding

Designers should make an effort to minimize noise by paying special attention to the circuit layout with the **SP6832** devices. External components should be connected in close proximity to the device and a ground plane should be implemented. This will keep electrical traces short minimizing parasitic inductance and capacitance.

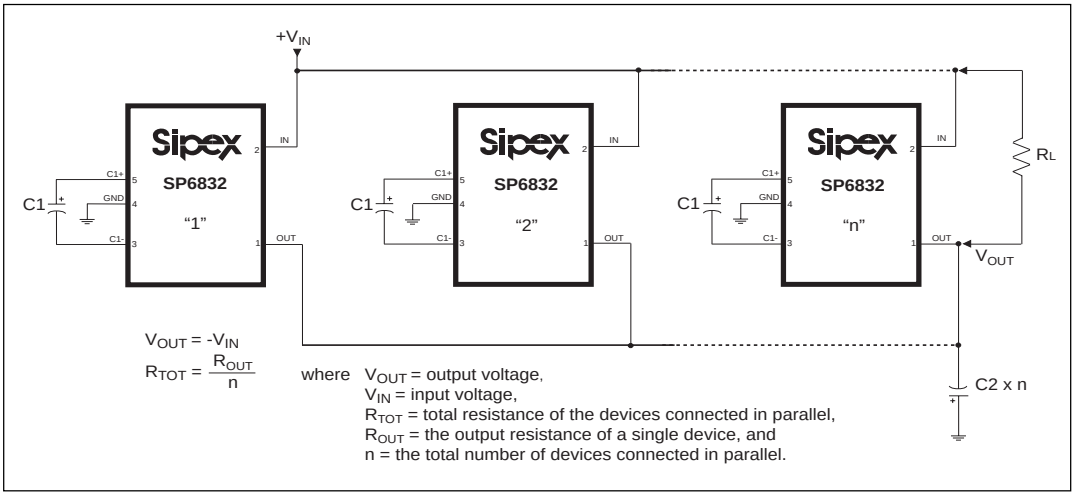


Figure 21. SP6832 Devices Connected in Parallel to Reduce Total Output Resistance

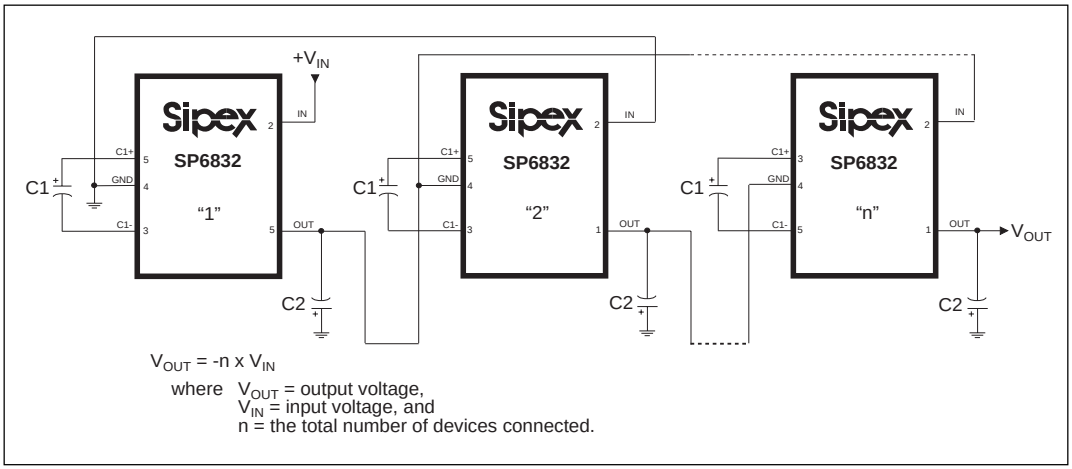
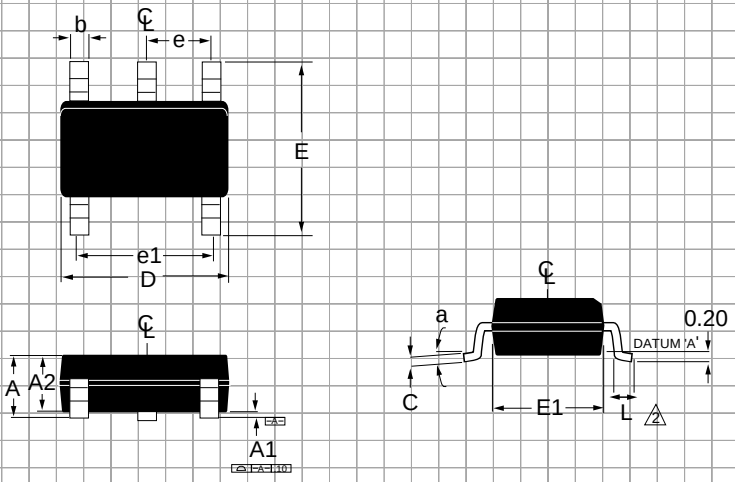


Figure 22. SP6832 Devices Cascaded to Increase Output Voltage

MANUFACTURER/ TELEPHONE #	PART NUMBER	CAPACITANCE / VOLTAGE	ESR @ 500kHz	CAPACITOR SIZE/TYPE
TDK/ 847-803-6100	C1005X5R0J104K	0.1µF / 6.3V	0.08Ω	0402/X5R
TDK/ 847-803-6100	C1608X5R0J334K	0.33µF / 6.3V	0.04Ω	0603/X5R
TAIYO/YUDEN 847-925-0888	LMK105BJ104KV	0.1µF / 10V	0.1Ω	0402/X5R
TAIYO/YUDEN 847-925-0888	LMK107BJ334KA	0.33µF / 10V	0.05Ω	0603/X7R

Table 1. Suggested Low ESR SM Ceramic Capacitors

PACKAGE: SOT23-5



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.25	0.50
C	0.09	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95ref	
e1	1.90ref	
a	0°	10°

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6832EK	-40˚C to +85˚C	SOT23-5
SP6832EK/TR	-40˚C to +85˚C	SOT23-5

Please consult the factory for pricing and availability on a Tape-On-Reel option.

SIGNAL PROCESSING EXCELLENCE

Sipex Corporation

Headquarters and
Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com

Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

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