SP3222H/3232H

3.3V, 460 Kbps RS-232 Transceivers

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with RS-232 down to +2.7V power source
- 1μA Low-Power Shutdown with Receivers Active (**SP3222H**)
- Enhanced ESD Specifications: ±2kV Human Body Model
- 460Kbps Minimum Transmission Rate
- Ideal for Handheld, Battery Operated Applications

DESCRIPTION

The **SP3222H** and the **3232H** are 2 driver/2 receiver RS-232 transceiver solutions intended for portable or hand-held applications such as notebook or palmtop computers. Their data transmission rate of 460Kbps meeting the demands of high speed RS-232 applications. Both ICS have a high-efficiency, charge-pump power supply that requires only 0.1μF capacitors for 3.3V operation. The charge pump allows the **SP3222H** and the **3232H** series to deliver true RS-232 performance from a single power supply ranging from +3.3V to +5.0V.

The **SP3222H** device has a low-power shutdown mode where the devices' driver outputs and charge pumps are disabled. During shutdown, the supply current is less than 1μA.

SELECTION TABLE

MODEL	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Shutdown	TTL 3-State	No. of Pins
SP3222H	+3.0V to +5.5V	2	2	4	Yes	Yes	18, 20
SP3232H	+3.0V to +5.5V	2	2	4	No	No	16

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V+ (NOTE 1).....-0.3V to +7.0V
V- (NOTE 1).....+0.3V to -7.0V
V+ + |V-| (NOTE 1).....+13V

I_{CC} (DC V_{CC} or GND current).....±100mA

Electrostatic Discharge
HBM 15kV
IEC1000-4-2-AirDischarge.....15kV
IEC1000-4-2 Direct Contact.....8kV

Input Voltages
TxIN, EN .....-0.3V to +6.0V
RxIN.....±25V

Output Voltages
TxOUT.....±13.2V
RxOUT.....-0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration
TxOUT.....Continuous

Storage Temperature.....-65°C to +150°C

Power Dissipation Per Package
20-pin SSOP (derate 9.25mW/°C above +70°C).....750mW
18-pin PDIP (derate 15.2mW/°C above +70°C).....1220mW
18-pin SOIC (derate 15.7mW/°C above +70°C).....1260mW
20-pin TSSOP (derate 11.1mW/°C above +70°C).....890mW
16-pin SSOP (derate 9.69mW/°C above +70°C).....775mW
16-pin PDIP (derate 14.3mW/°C above +70°C).....1150mW
16-pin Wide SOIC (derate 11.2mW/°C above +70°C)....900mW
16-pin TSSOP (derate 10.5mW/°C above +70°C).....850mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

SPECIFICATIONS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.0V with T_{AMB} = T_{MIN} to T_{MAX}

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current		0.3	1.0	mA	no load, T_{AMB} = +25°C, V_{CC} = +3.3V, TxIN = V_{CC} or GND
Shutdown Supply Current		1.0	10	µA	$\overline{SHDN}$=GND, T_{AMB} = +25°C, V_{CC}=+3.3V, TxIN=V_{CC} or GND
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW			0.8	V	TxIN, $\overline{EN}$, $\overline{SHDN}$, Note 2
Input Logic Threshold HIGH	2.0 2.4			V	V_{CC}=3.3V, Note 2 V_{CC}=5.0V, Note 2
Input Leakage Current		±0.01	±1.0	µA	TxIN, $\overline{EN}$, $\overline{SHDN}$, T_{AMB} = +25°C
Output Leakage Current		±0.05	±10	µA	receivers disabled
Output Voltage LOW			0.4	V	I_{OUT}=1.6mA
Output Voltage HIGH	V_{CC}-0.6	V_{CC}-0.1		V	I_{OUT}=-1.0mA
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	3kΩ load to ground at all driver outputs, T_{AMB}=+25°C
Output Resistance	300			Ω	V_{CC}= V+ = V- = 0V, T_{OUT} = ±2V
Output Short-Circuit Current		±35	±60	mA	V_{OUT} = 0V
Output Leakage Current			±25	µA	V_{OUT} = ±12V, V_{CC} = 0V or 3.0V+5.5V, drivers disabled

SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.0V with $T_{AMB} = T_{MIN}$ to T_{MAX} .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER INPUTS					
Input Voltage Range	-15		+15	V	
Input Threshold LOW	0.6 0.8	1.2 1.5		V	V_{CC}=3.3V V_{CC}=5.0V
Input Threshold HIGH		1.5 1.8	2.4 2.4	V	V_{CC}=3.3V V_{CC}=5.0V
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	
TIMING CHARACTERISTICS					
Maximum Data Rate	460			Kbps	R_L=3kΩ, C_L=1000pF, one driver switching
Driver Propagation Delay		1.0 1.0		µs µs	t_{PHL}, R_L = 3KΩ, C_L = 1000pF t_{PLH}, R_L = 3KΩ, C_L = 1000pF
Receiver Propagation Delay		0.3 0.3		µs	t_{PHL}, RxIN to RxOUT, C_L=150pF t_{PLH}, RxIN to RxOUT, C_L=150pF
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Driver Skew		100	500	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Receiver Skew		200	1000	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Transition-Region Slew Rate		60		V/µs	V_{CC} = 3.3V, R_L = 3KΩ, T_{AMB} = 25°C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 460Kbps data rates, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

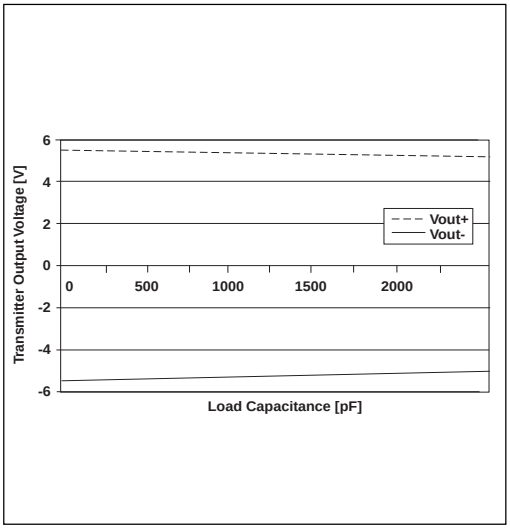


Figure 1. Transmitter Output Voltage VS. Load Capacitance for the SP3222H and the SP3232H

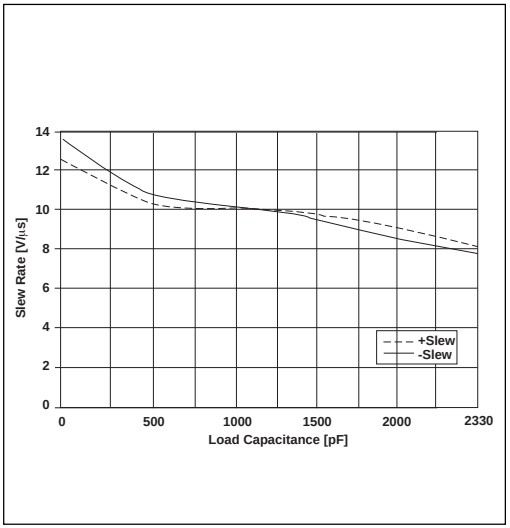


Figure 2. Slew Rate VS. Load Capacitance for the SP3222H and the SP3232H

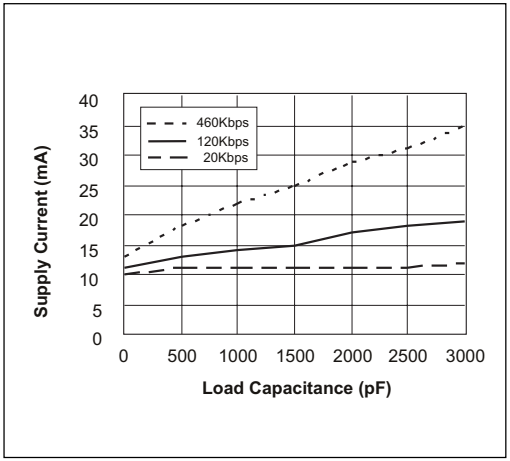


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data for the SP3222H and the SP3232H

NAME	FUNCTION	PIN NUMBER		
		SP3222H		SP3232H
		DIP/SO	SSOP/ TSSOP	
$\overline{EN}$	Receiver Enable. Apply logic LOW for normal operation. Apply Logic HIGH to disable the receiver outputs (high-Z state).	1	1	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2	2	1
V+	+5.5V generated by the charge pump.	3	3	2
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4	4	3
C2+	Positive terminal of the inverting charge-pump capacitor.	5	5	4
C2-	Negative terminal of the inverting charge-pump capacitor.	6	6	5
V-	-5.5V generated by the charge pump.	7	7	6
T1OUT	RS-232 driver output.	15	17	14
T2OUT	RS-232 driver output.	8	8	7
R1IN	RS-232 receiver input.	14	16	13
R2IN	RS-232 receiver input.	9	9	8
R1OUT	TTL/CMOS receiver output.	13	15	12
R2OUT	TTL/CMOS receiver output.	10	10	9
T1IN	TTL/CMOS driver input.	12	13	11
T2IN	TTL/CMOS driver input.	11	12	10
GND	Ground.	16	18	15
V_{CC}	+3.0V to +5.5V supply voltage	17	19	16
$\overline{SHDN}$	Shutdown Control Input. Drive HIGH for normal device operation. Drive LOW to shutdown the drivers (high-Z output) and the on-board power supply.	18	20	-
NC	No Connect.	-	11, 14	-

Table 1. Device Pin Description

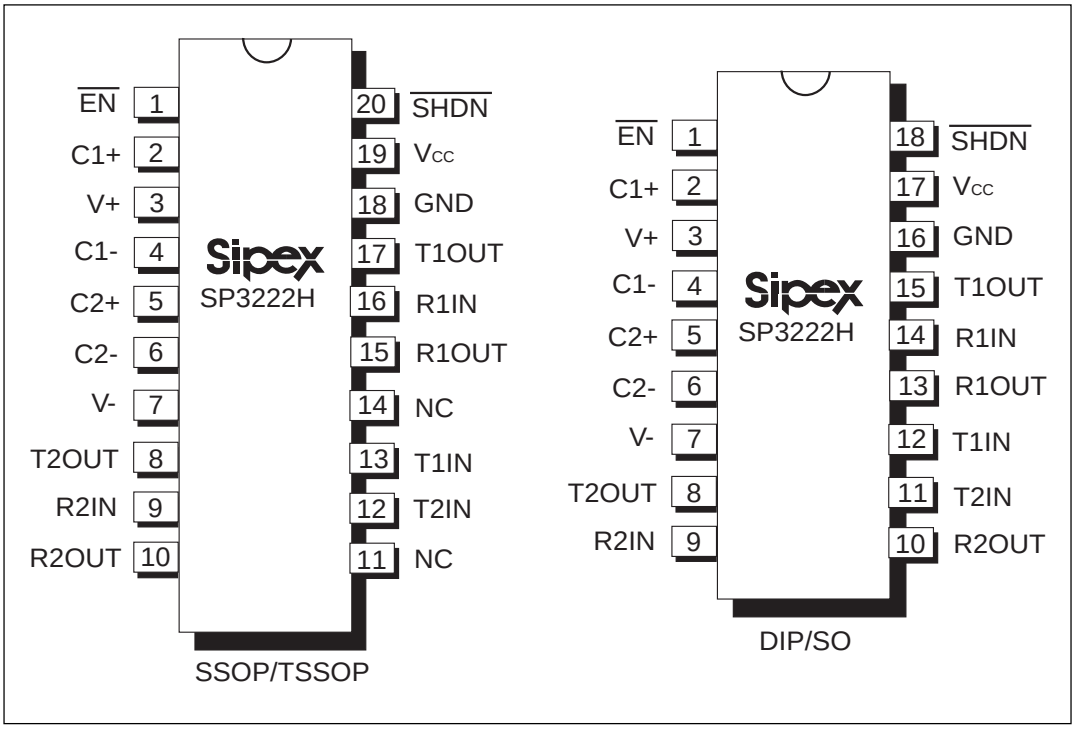


Figure 4. Pinout Configurations for the SP3222H

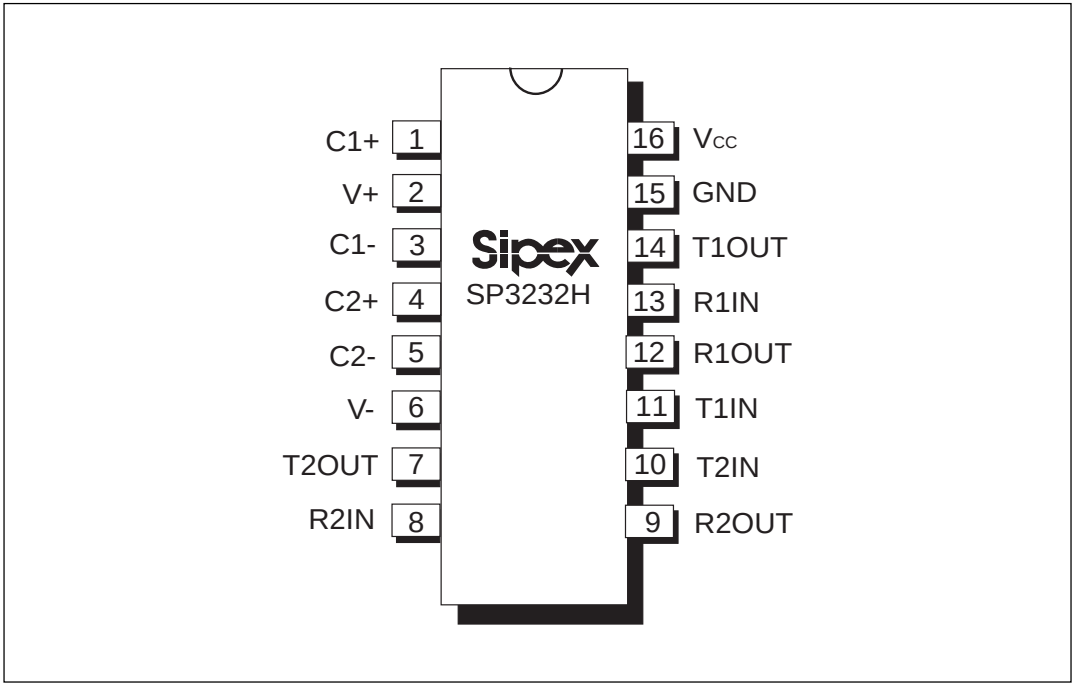


Figure 5. Pinout Configuration for the SP3232H

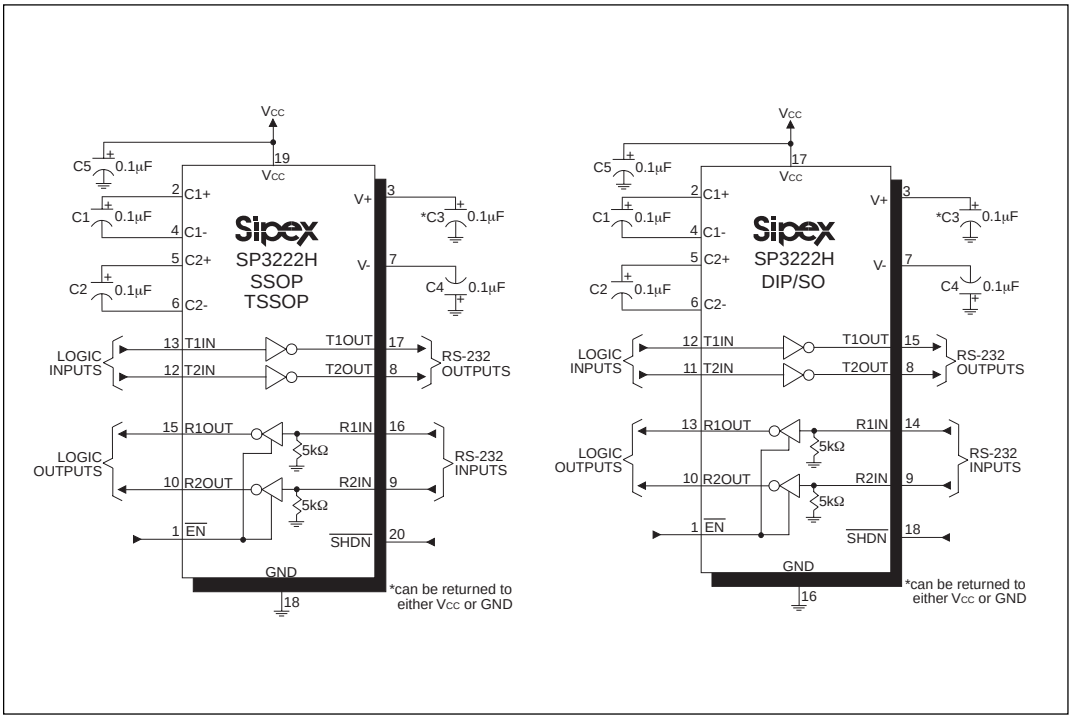


Figure 6. SP3222H Typical Operating Circuits

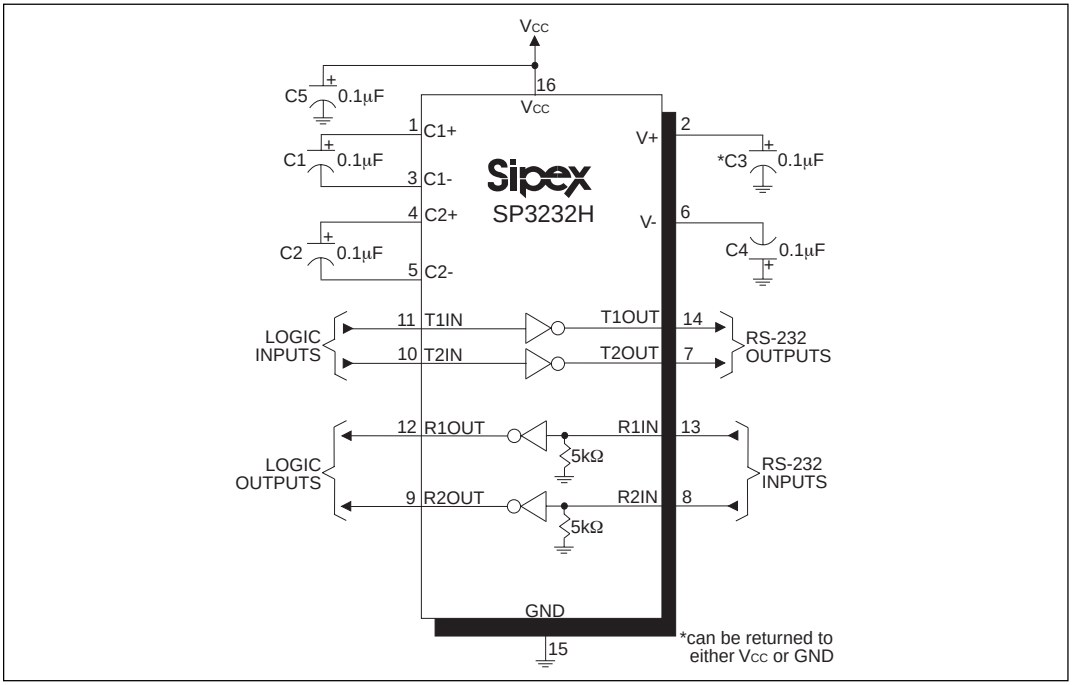


Figure 7. SP3232H Typical Operating Circuit

DESCRIPTION

The **SP3222H** and **SP3232H** are 2-driver/ 2-receiver devices ideal for portable or hand-held applications. The **SP3222H** features a 1μA shut-down mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only 1μA supply current.

The **SP3222H/3232H** transceivers meet the EIA/ TIA-232 and V.28/V.24 communication protocols. They feature **Sipex's** proprietary on-board charge pump circuitry that generates 2 x V_{CC} for RS-232 voltage levels from a single +3.0V to +5.5V power supply. The **SP3222H/ 3232H** drivers operate at a minimum data rate of 460Kbps.

THEORY OF OPERATION

The **SP3222H/3232H** are made up of three basic circuit blocks: 1. Drivers, 2. Receivers, and 3. the Sipex proprietary charge pump.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to ±5.0V EIA/TIA-232 levels inverted relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.5V with no load and at least ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of ±3.7V with supply voltages as low as 2.7V.

The drivers have a minimum data rate of 460Kbps fully loaded with 3KΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of 30V/μs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

Figure 8 shows a loopback circuit used to test the RS-232 drivers. *Figure 9* shows the test results of the loopback circuit with all drivers active at 120Kbps and RS-232 loads in parallel with 1000pF capacitors. *Figure 10* shows the test results where one driver is active at 460Kbps and all drivers are loaded with an RS-232 receiver in parallel with a 1000pF capacitor.

The **SP3222H** driver's output stages are tri-stated in shutdown mode. When the power is off, the **SP3222H** device permits the outputs to be driven up to ±12V. Because the driver's inputs do not have pull-up resistors, unused inputs should be connected to V_{CC} or GND.

In the shutdown mode, the supply current is less than 1μA, where $\overline{SHDN}$ = LOW. When the **SP3222H** device is shut down, the device's driver outputs are disabled (tri-stated) and the charge pumps are turned off with V+ pulled down to V_{CC} and V- pulled to GND. The time required to exit shutdown is typically 100μs. $\overline{SHDN}$ is connected to V_{CC} if the shutdown mode is not used. $\overline{SHDN}$ has no effect on RxOUT or RxOUTB. As they become active, the two driver outputs go to opposite RS-232 levels: one driver input is HIGH and the other LOW. Note that the drivers are enabled only when the magnitude of V- exceeds approximately 3V.

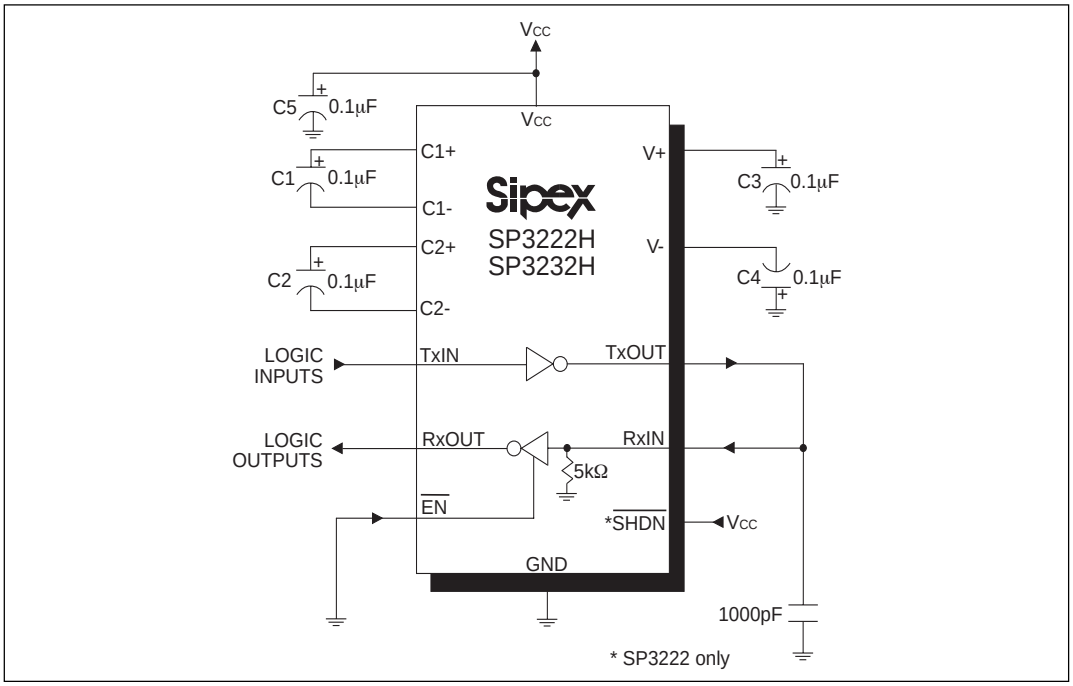


Figure 8. SP3222H/3232H Driver Loopback Test Circuit

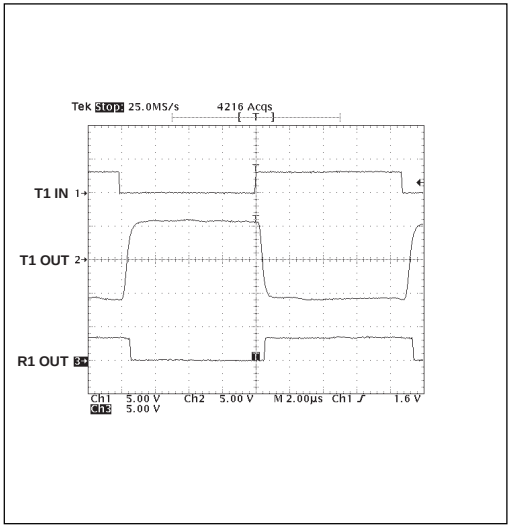


Figure 9. Driver Loopback Test Results at 120Kbps

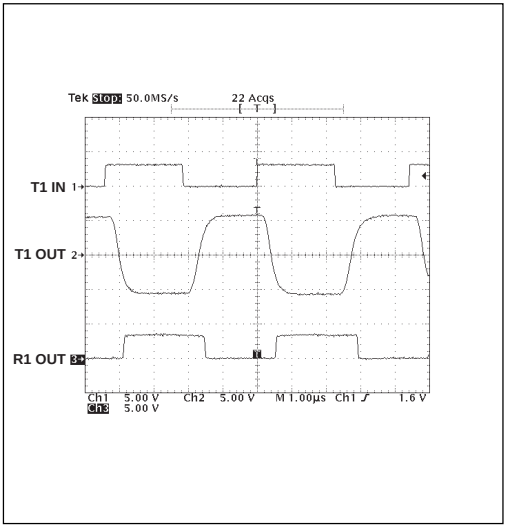


Figure 10. Driver Loopback Test Results at 460Kbps

Receivers

The receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. The SP3222H receivers have an inverting tri-state output.Receiver outputs (RxOUT) are tri-stated when the enable control $\overline{EN}$ = HIGH. In the shutdown mode, the receivers can be active or inactive. $\overline{EN}$ has no effect on TxOUT. The truth table logic of the **SP3222H** driver and receiver outputs can be found in *Table 2*.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal and inject noise, the inputs have a typical hysteresis margin of 300mV. Should an input be left unconnected, a 5kΩ pulldown resistor to ground forces the output of the receiver HIGH.

Charge Pump

The **Sipex** patented charge pump (5,306,954) uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies and requires four external capacitors. The internal power supply consists of a regulated dual charge pump that provides an output voltage of 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range.

$\overline{SHDN}$	$\overline{EN}$	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state

Table 2. Truth Table Logic for Shutdown and Enable Control

In most circumstances, decoupling the power supply can be achieved adequately using a 0.1μF bypass capacitor at C5 (refer to *Figures 6* and *7*). In applications that are sensitive to power-supply noise,V_{CC} and ground can be decoupled with a capacitor of the same value as charge-pump capacitor C1. It is always important to physically locate bypass capacitors close to the IC.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltage is less than 5.5V, the charge pump is enabled. If the output voltage exceeds 5.5V, the charge pump is disabled. An oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1: V_{SS} Charge Storage *(Figure 12)*

During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2: V_{SS} Transfer *(Figure 13)*

Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3: V_{DD} Charge Storage *(Figure 15)*

The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4: V_{DD} Transfer *(Figure 16)*

The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to repeat. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}; in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The charge pump clock rate typically operates at 250kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

ESD Tolerance

The **SP3222H/3232H** series incorporates ruggedized ESD cells on all driver output and receiver input pins.

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 17*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ and 100pF, respectively.

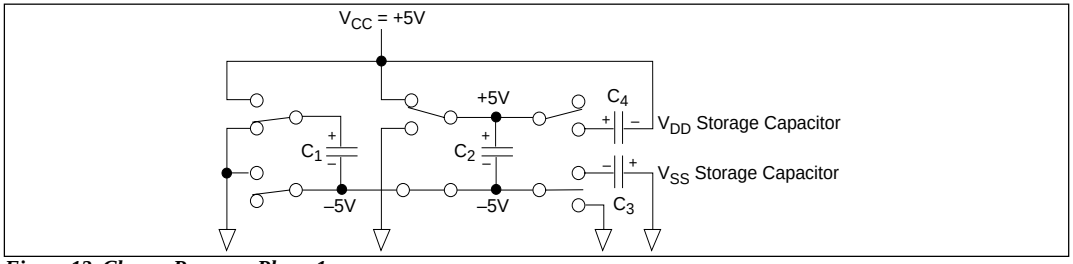


Figure 12. Charge Pump — Phase 1

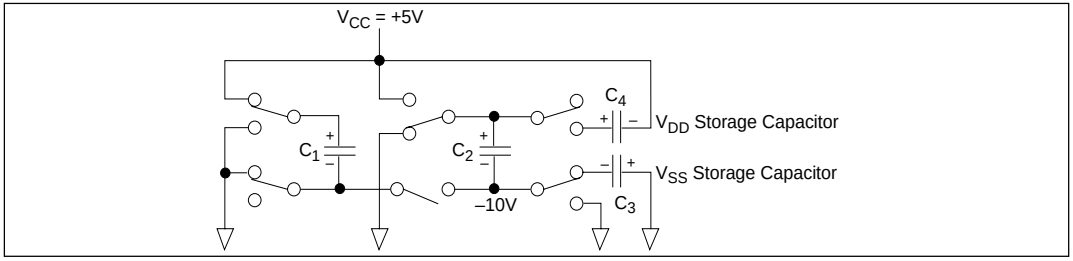


Figure 13. Charge Pump — Phase 2

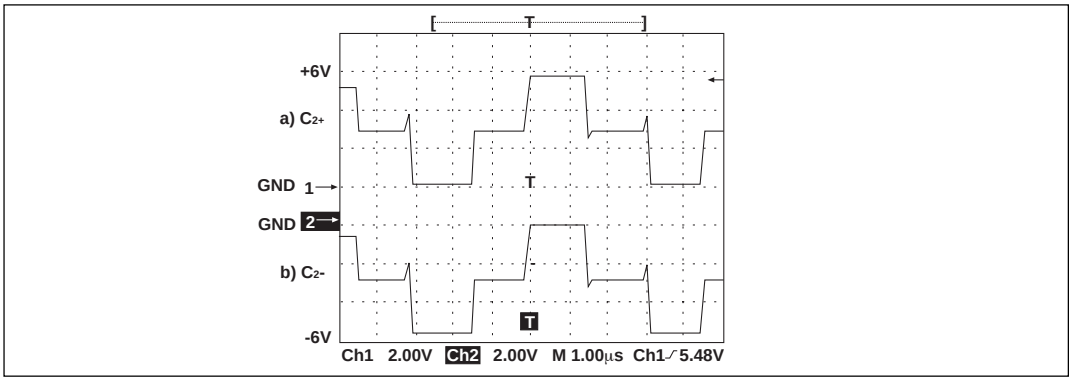


Figure 14. Charge Pump Waveforms

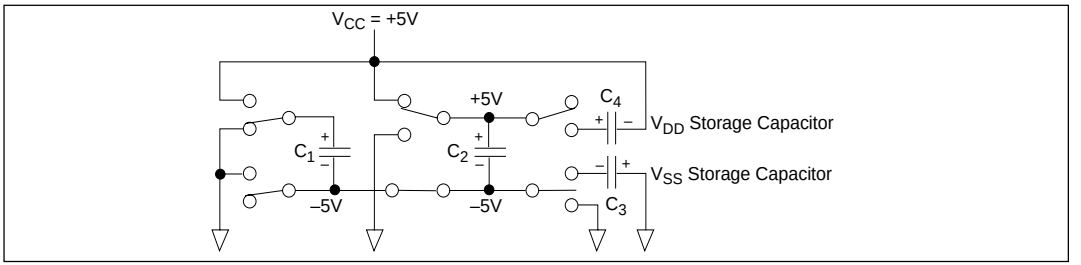


Figure 15. Charge Pump — Phase 3

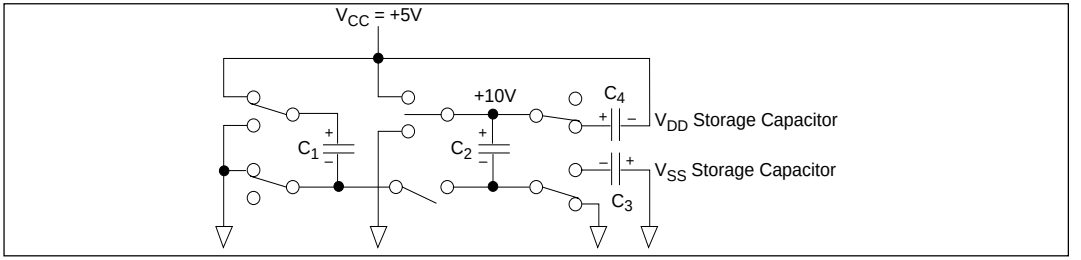


Figure 16. Charge Pump — Phase 4

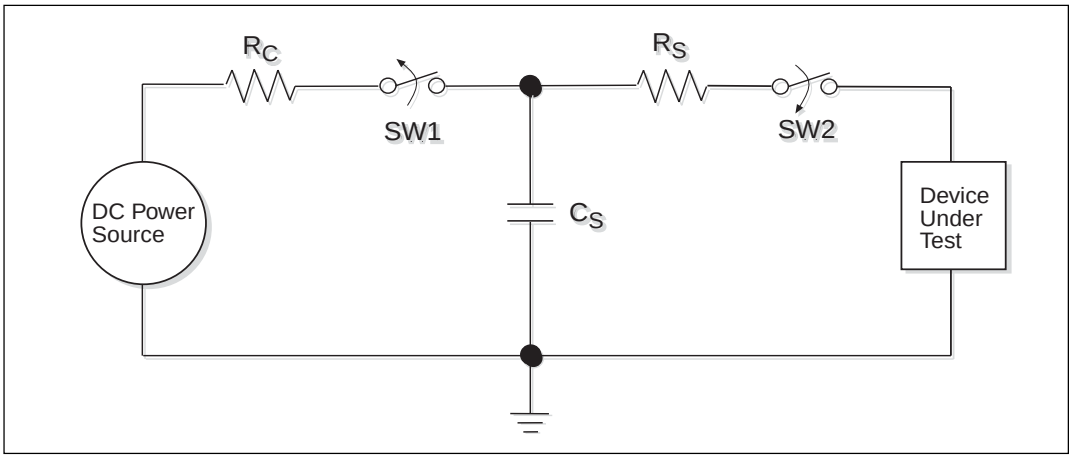
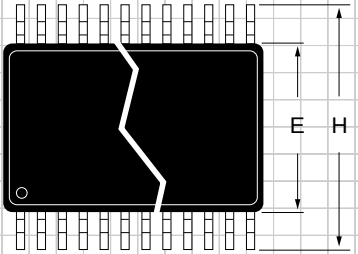
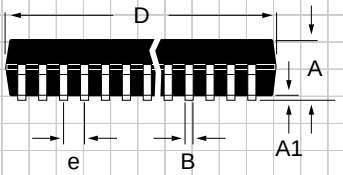
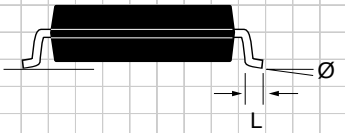


Figure 17. ESD Test Circuit for Human Body Model

PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)

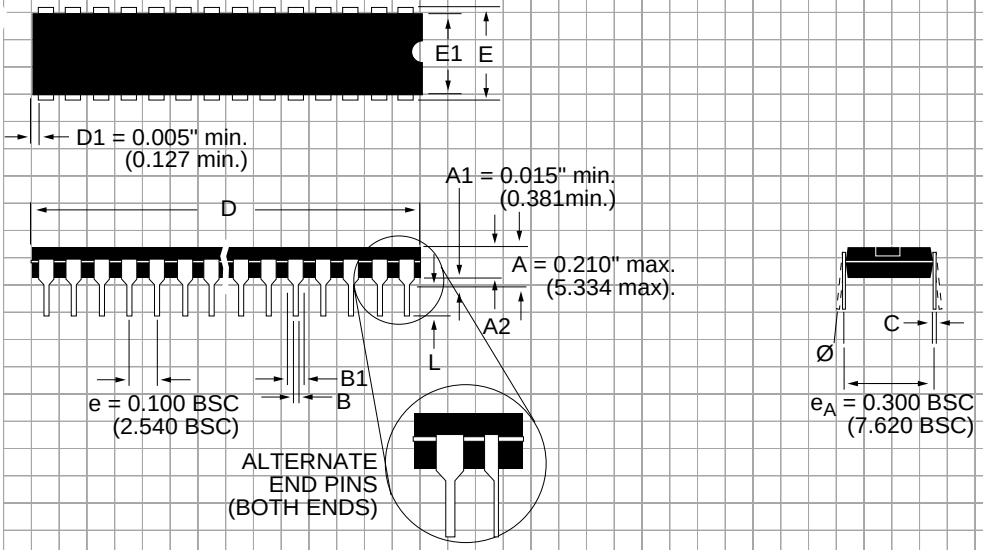






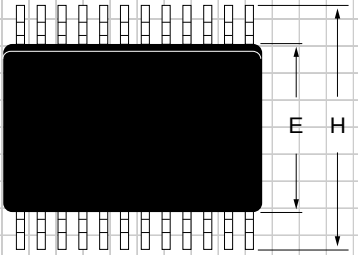
DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	20–PIN	24–PIN	28–PIN
A	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)
D	0.239/0.249 (6.07/6.33)	0.278/0.289 (7.07/7.33)	0.317/0.328 (8.07/8.33)	0.397/0.407 (10.07/10.33)
E	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)
H	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

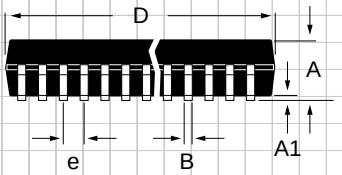
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

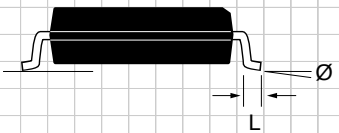


DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	18–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC)

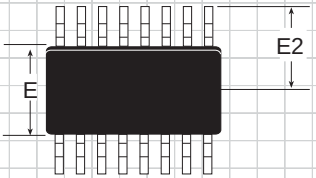


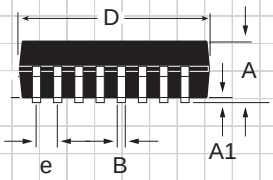


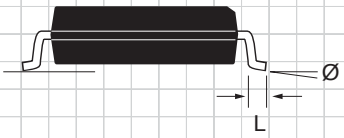


DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	18–PIN
A	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649))
A1	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.398/0.413 (10.10/10.49)	0.447/0.463 (11.35/11.74)
E	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)

PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)







DIMENSIONS in inches (mm) Minimum/Maximum	16–PIN	20–PIN
A	- /0.043 (- /1.10)	- /0.043 (- /1.10)
A1	0.002/0.006 (0.05/0.15)	0.002/0.006 (0.05/0.15)
B	0.007/0.012 (0.19/0.30)	0.007/0.012 (0.19/0.30)
D	0.193/0.201 (4.90/5.10)	0.252/0.260 (6.40/6.60)
E	0.169/0.177 (4.30/4.50)	0.169/0.177 (4.30/4.50)
e	0.026 BSC (0.65 BSC)	0.026 BSC (0.65 BSC)
E2	0.126 BSC (3.20 BSC)	0.126 BSC (3.20 BSC)
L	0.020/0.030 (0.50/0.75)	0.020/0.030 (0.50/0.75)
Ø	0°/8°	0°/8°

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP3222HCA	0˚C to +70˚C	20-Pin SSOP
SP3222HCP	0˚C to +70˚C	18-Pin PDIP
SP3222HCT	0˚C to +70˚C	18-Pin WSOIC
SP3222HCY	0˚C to +70˚C	20-Pin TSSOP
SP3232HCA	0˚C to +70˚C	16-Pin SSOP
SP3232HCP	0˚C to +70˚C	16-Pin PDIP
SP3232HCT	0˚C to +70˚C	16-Pin WSOIC
SP3232HCY	0˚C to +70˚C	16-Pin TSSOP

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

Sipex Corporation

Headquarters and Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com