SANYO

No.676D

2SB808/2SD1012

PNP/NPN Epitaxial Planar Silicon Transistors

Low-Voltage Large-Current Amp Applications

( ):2SB808

Absolute Maximum Ratings at T_a=25°C

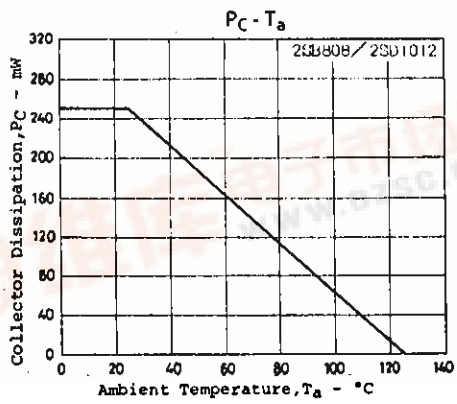
			unit
Collector to Base Voltage	V_{CBO}	(-)20	V
Collector to Emitter Voltage	V_{CEO}	(-)15	V
Emitter to Base Voltage	V_{EBO}	(-)5	V
Collector Current	I_C	(-)0.7	A
Collector Current(Pulse)	I_{CP}	(-)1.5	A
Collector Dissipation	P_C	250	mW
Junction Temperature	Tj	125	°C
Storage Temperature	T_{stg}	-55 to +125	°C

Electrical Characteristics at T_a=25°C

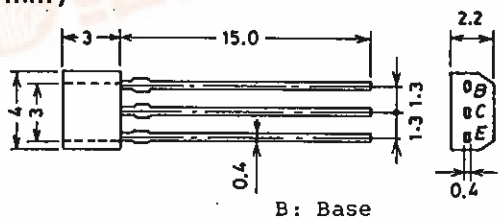
			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	V_{CB}=(-)15V,I_E=0			(-)1.0	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=(-)4V,I_C=0			(-)1.0	μA
DC Current Gain	$h_{FE(1)}$	V_{CE}=(-)2V,I_C=(-)50mA	160*		960*	
	$h_{FE(2)}$	V_{CE}=(-)2V,I_C=(-)500mA Pulse	80			
Gain-Bandwidth Product	f_T	V_{CE}=(-)10V,I_C=(-)50mA		250		MHz
Common Base Output Capacitance	c_{ob}	V_{CB}=(-)10V,f=1MHz		(13)		pF
Collector to Emitter Saturation Voltage	$V_{CE(sat)1}$	I_C=(-)5mA,I_B=(-)0.5mA		8 (-15)	(-35)	mV
	$V_{CE(sat)2}$	I_C=(-)100mA,I_B=(-)10mA		10 (-60)	25 (-120)	mV
Base to Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=(-)100mA,I_B=(-)10mA		30 (-)0.8	80 (-)1.2	V
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	IC=(-)10μA,I_E=0	(-)20			V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=(-)1mA,R_{BE}=∞	(-)15			V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=(-)10μA,I_C=0	(-)5			V

* The 2SB808/2SD1012 are classified by 50mA h_{FE} as follows :

2SB808	160	F	320	280	G	560		
2SD1012	160	F	320	280	G	560	480	H	960

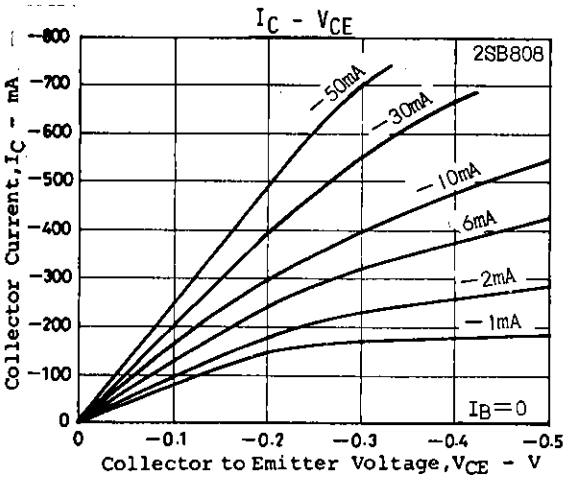


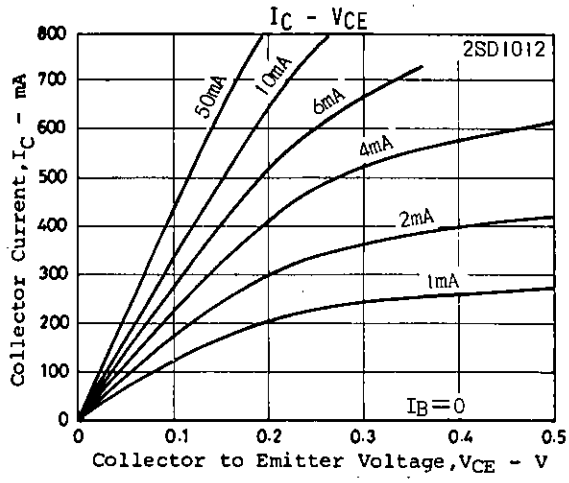
Package Dimensions 2033
(unit: mm)

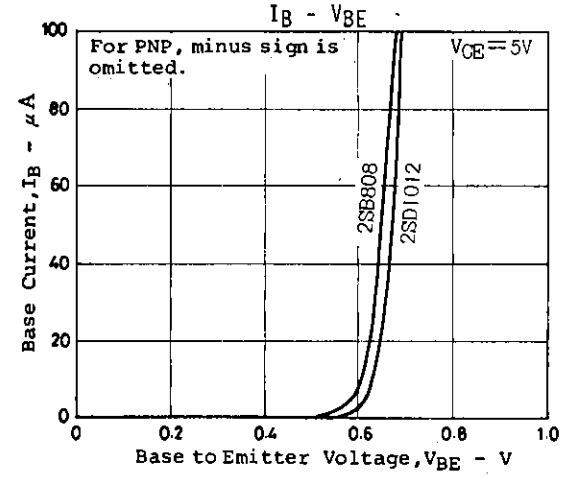


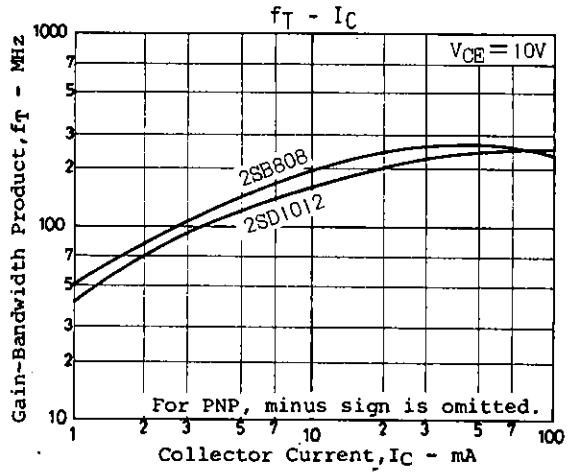
B: Base
C: Collector
E: Emitter

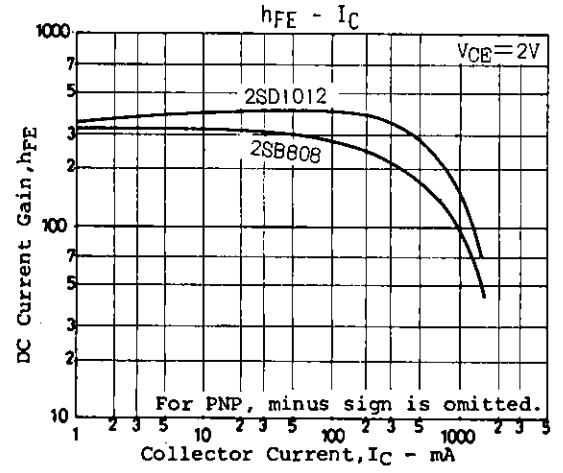
SANYO: SPA

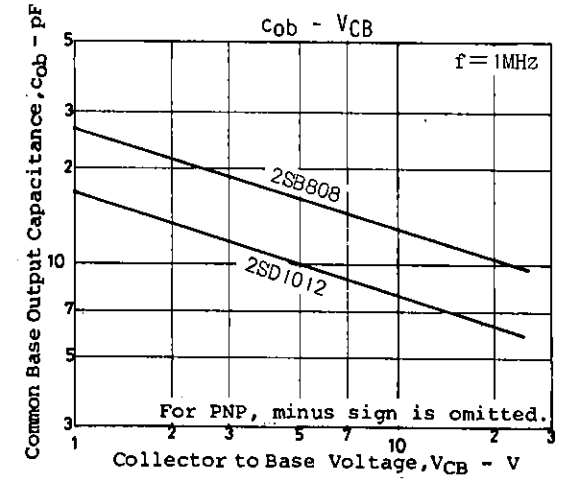

I_C - V_{CE}
2SB808
−50mA
−30mA
−10mA
−6mA
−2mA
−1mA
I_B=0
Collector Current, I_C - mA
Collector to Emitter Voltage, V_{CE} - V

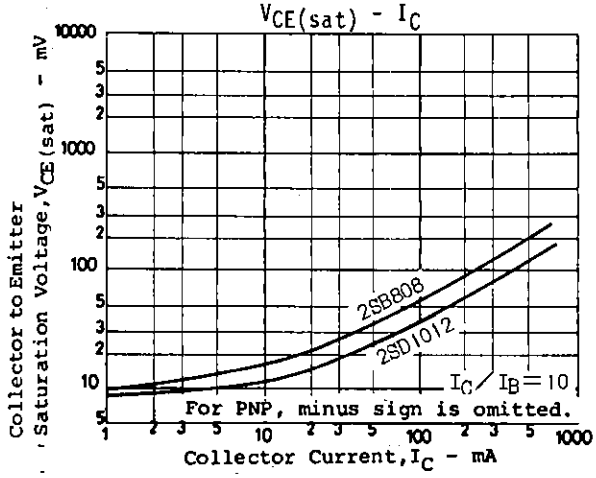

I_C - V_{CE}
2SD1012
50mA
10mA
6mA
4mA
2mA
1mA
I_B=0
Collector Current, I_C - mA
Collector to Emitter Voltage, V_{CE} - V

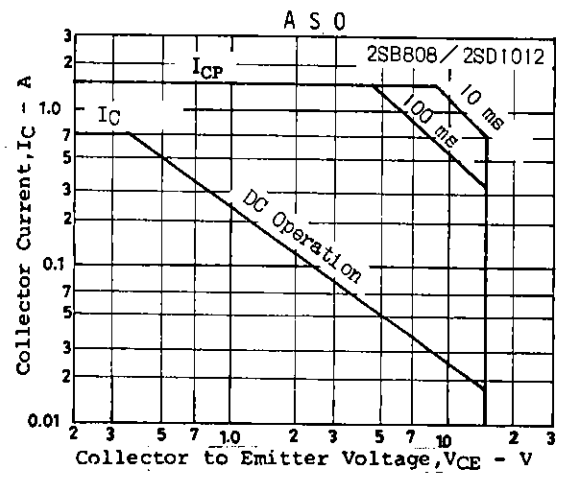

I_B - V_{BE}
For PNP, minus sign is omitted.
V_{CE}=5V
2SB808
2SD1012
Base Current, I_B - μA
Base to Emitter Voltage, V_{BE} - V


f_T - I_C
V_{CE}=10V
2SB808
2SD1012
For PNP, minus sign is omitted.
Gain-Bandwidth Product, f_T - MHz
Collector Current, I_C - mA


h_{FE} - I_C
V_{CE}=2V
2SD1012
2SB808
For PNP, minus sign is omitted.
DC Current Gain, h_{FE}
Collector Current, I_C - mA


Cob - V_{CB}
f=1MHz
2SB808
2SD1012
For PNP, minus sign is omitted.
Common Base Output Capacitance, C_{ob} - pF
Collector to Base Voltage, V_{CB} - V

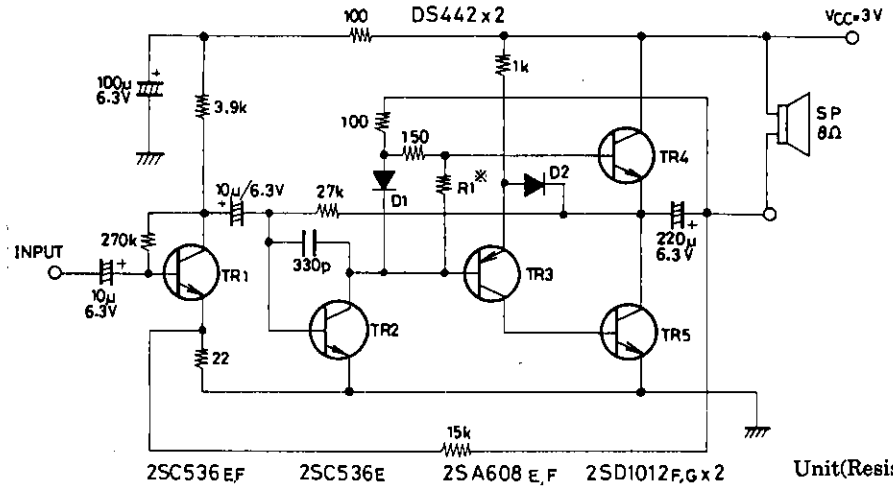

$V_{CE(sat)}$ - I_C
2SB808
2SD1012
I_C / I_B=10
For PNP, minus sign is omitted.
Collector to Emitter Saturation Voltage, $V_{CE(sat)}$ - mV
Collector Current, I_C - mA


A S O
2SB808 / 2SD1012
I_{CP}
I_C
10 ms
100 ms
DC Operation
Collector Current, I_C - A
Collector to Emitter Voltage, V_{CE} - V

Sample Application Circuit : Low-voltage 3V(P_O 120mW) ITL-OTL power amp.

. Circuit configuration

For obtaining an output of more than 100mW, the middle-point voltage at the output stage and the collector voltage of the driver transistor must be $V_{CC}/2$. Therefore, the output stage is of quasi complementary configuration composed of npn/npn transistors. The phase is reversed by the 2SA608 and the middle-point voltage at the output stage and the collector voltage of the driver transistor are made to be $V_{CC}/2$ so that the output can be maximized.



Unit(Resistance : Ω, Capacitance : F)

R_1 : Used control idle current

For $R_1 = 820\Omega$, use rank F for [TR4,5(2SD1012)].

For $R_1 = 680\Omega$, use rank G for [TR4,5(2SD1012)].

. Main Specifications

Characteristic	Conditions	f=400Hz	f=1kHz	unit
Current dissipation	Quiescent,total current dissipation	11.0 to 15.5	11.0 to 15.5	mA
Output power	THD=10%	120 to 125	127 to 130	mW
Voltage gain	P_O=10mW	43.3 to 45.5	43.5 to 45.7	dB
Total harmonic distortion	P_O=50mW	1.4 to 2.6	1.3 to 2.5	%
Input resistance	P_O=10mW	10.4 to 20.5	11.0 to 21.0	kΩ

Note : For above-mentioned h_{FE} rank.