2SJ0364 (2SJ364)

Silicon P-Channel Junction FET

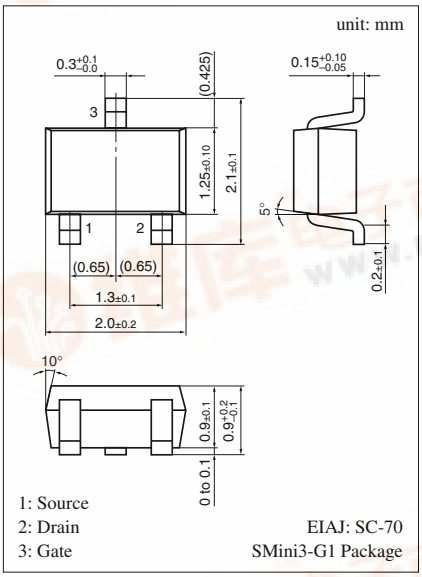
For analog switch

■ Features

- Low ON-resistance
- Low-noise characteristics

■ Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Gate to Drain voltage	V_{GDS}	65	V
Drain current	I_D	−20	mA
Gate current	I_G	−10	mA
Allowable power dissipation	P_D	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	−55 to +150	°C



Marking Symbol (Example): 4M

■ Electrical Characteristics (Ta = 25°C)

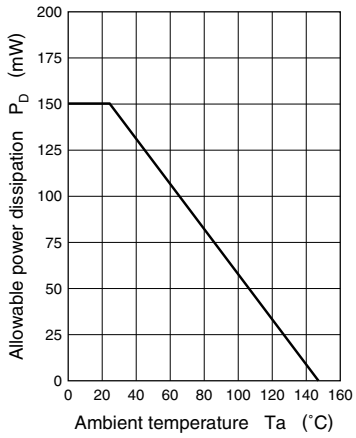
Parameter	Symbol	Conditions	min	typ	max	Unit
Drain to Source cut-off current	I_{DSS}*	V_{DS} = −10V, V_{GS} = 0	− 0.2		−6	mA
Gate to Source leakage current	I_{GSS}	V_{GS} = 30V, V_{DS} = 0			10	nA
Gate to Drain voltage	V_{GDS}	I_G = 10µA, V_{DS} = 0	65			V
Gate to Source cut-off voltage	V_{GSC}	V_{DS} = −10V, I_D = −10µA		1.5	3.5	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = −10V, I_D = −1mA, f = 1kHz	1.8	2.5		mS
Drain to Source ON-resistance	$R_{DS(on)}$	V_{DS} = −10mV, V_{GS} = 0		300		Ω
Input capacitance (Common Source)	C_{iss}	V_{DS} = −10V, V_{GS} = 0, f = 1MHz		12		pF
Reverse transfer capacitance (Common Source)	C_{rss}			4		pF

* I_{DSS} rank classification

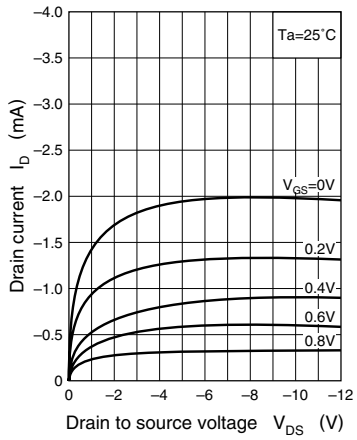
Runk	O	P	Q	R
I_{DSS} (mA)	− 0.2 to −1	− 0.6 to −1.5	−1 to −3	−2.5 to −6
Marking Symbol	4MO	4MP	4MQ	4MR

Note) The part number in the parenthesis shows conventional part number.

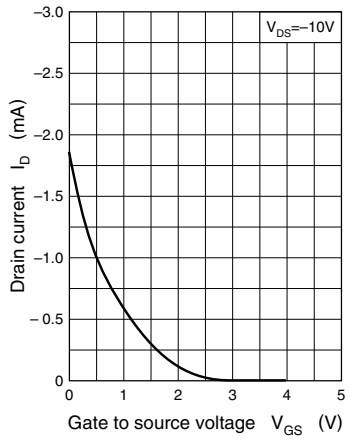
P_D — Ta



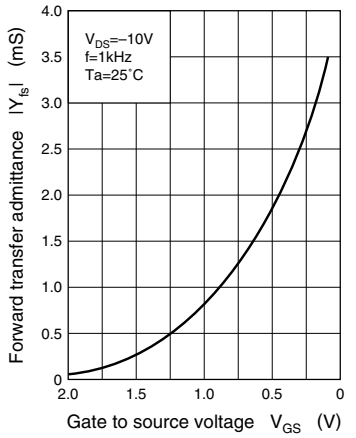
I_D — V_{DS}



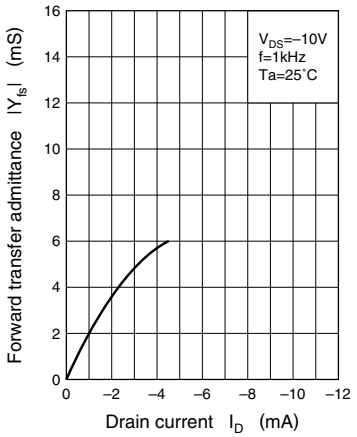
I_D — V_{GS}



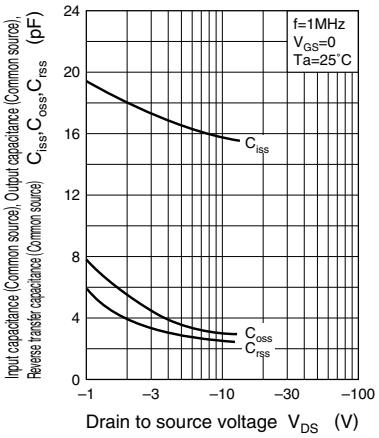
| Y_{fs} | — V_{GS}



| Y_{fs} | — I_D



C_{iss}, C_{oss}, C_{rss} — V_{DS}



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