

MOS FIELD EFFECT TRANSISTOR

2SJ448

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SJ448 is P-Channel MOS Field Effect Transistor designed for high voltage switching applications.

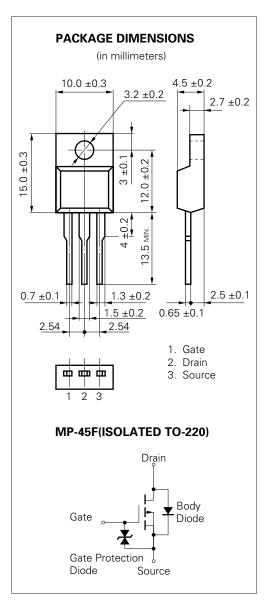
FEATURES

- Low On-Resistance
 - $R_{DS(on)} = 2.0 \Omega MAX$. (@ $V_{GS} = -10 V$, $I_{D} = -2.0 A$)
- Low Ciss Ciss = 470 pF TYP.
- · Built-in G-S Gate Protection Diodes
- · High Avalanche Capability Ratings
- Isolated TO-220 Package

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage	VDSS	-250	V
Gate to Source Voltage	Vgss	∓25	V
Drain Current (DC)	ID(DC)	∓4.0	Α
Drain Current (pulse)*	I _{D(pulse)}	∓16	Α
Total Power Dissipation ($T_c = 25$ °C)	P _{T1}	30	W
Total Power Dissipation (TA = 25 $^{\circ}$ C)	P _{T2}	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current**	las	-4.0	Α
Single Avalanche Energy**	Eas	80	mJ

- * PW \leq 10 μ s, Duty Cycle \leq 1 %
- ** Starting Tch = 25 °C, Rg = 25 Ω , Vgs = -20 V \rightarrow 0





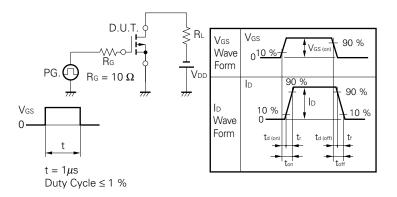
ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	RDS(on)		1.5	2.0	Ω	Vgs = -10 V, ID = -20 A
Gate to Source Cutoff Voltage	V _{GS(off)}	-4.0	-4.8	-5.5	V	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$
Forward Transfer Admittance	yfs	1.0	2.3		S	$V_{DS} = -10 \text{ V}, I_{D} = -20 \text{ A}$
Drain Leakage Current	IDSS			-100	μΑ	V _{DS} = -250 V, V _{GS} = 0
Gate to Source Leakage Current	Igss			∓10	μΑ	$V_{GS} = \mp 25 \text{ V}, V_{DS} = 0$
Input Capacitance	Ciss		470		pF	V _{DS} = -10 V
Output Capacitance	Coss		200		pF	V _G S = 0
Reverse Transfer Capacitance	Crss		70		pF	f = 1 MHz
Turn-On Delay Time	td(on)		13		ns	ID = -2.0 A
Rise Time	tr		7		ns	$V_{GS(on)} = -10 \text{ V}$
Turn-Off Delay Time	td(off)		34		ns	V _{DD} = -125 V
Fall Time	tf		10		ns	$R_G = 10 \Omega$
Total Gate Charge	Qg		15		nC	ID = -4.0 A
Gate to Source Charge	Qgs		4		nC	V _{DD} = -200 V
Gate to Drain Charge	QgD		9		nC	V _{GS} = -10 V
Body Diode Forward Voltage	V _{F(S-D)}		1.0		V	IF = -4.0 A, VGS = 0
Reverse Recovery Time	trr		195		ns	IF = -4.0 A, VGS = 0
Reverse Recovery Charge	Qrr		760		nC	di/dt = 50 A/μs

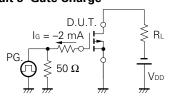
Test Circuit 1 Avalanche Capability

$V_{GS} = -20 \rightarrow 0 \text{ V}_{M} \text{ Jas}$ V_{DD} V_{DD} V_{DS} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}

Test Circuit 2 Switching Time

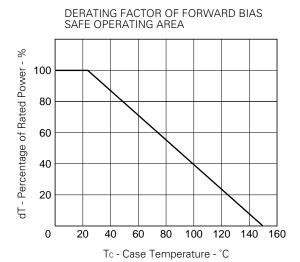


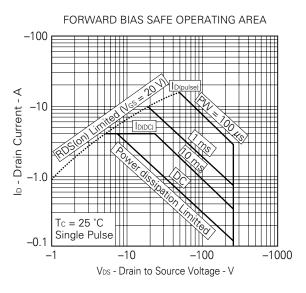
Test Circuit 3 Gate Charge

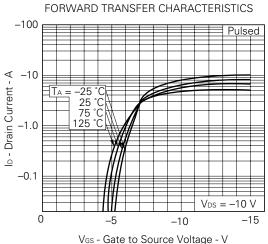


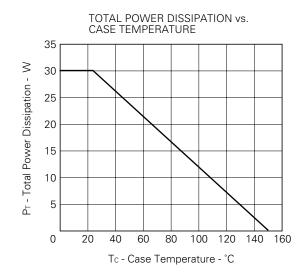
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

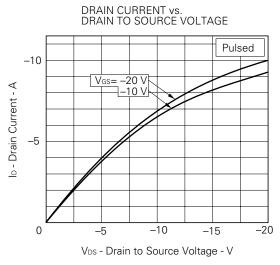
TYPICAL CHARACTERISTICS (TA = 25 °C)





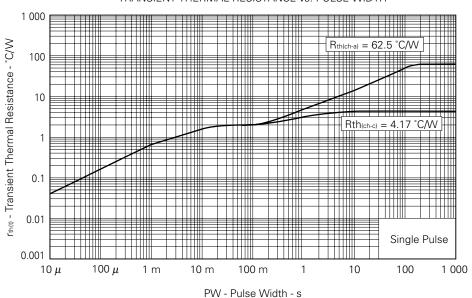




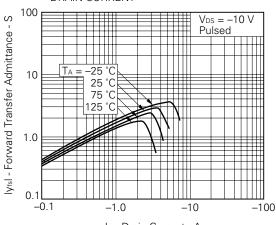


NEC

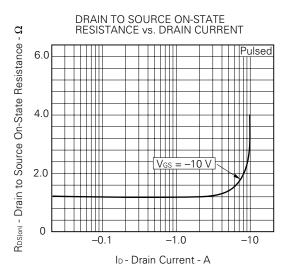
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



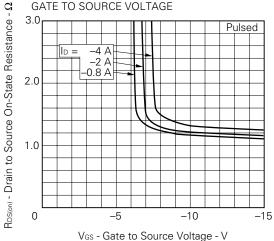
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



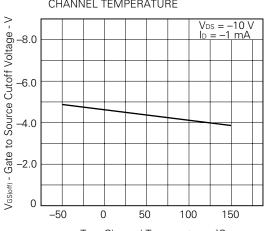
ID - Drain Current - A



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

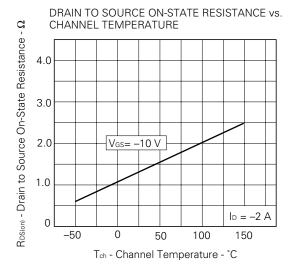


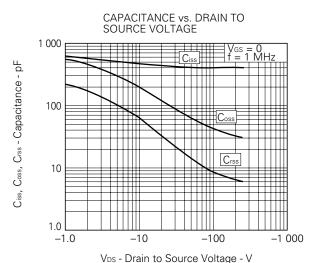
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

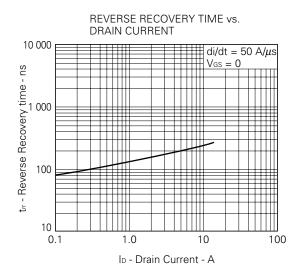


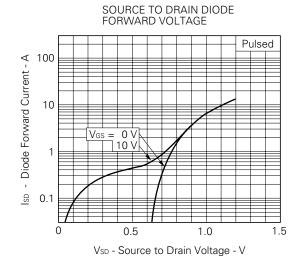
Tch - Channel Temperature - °C

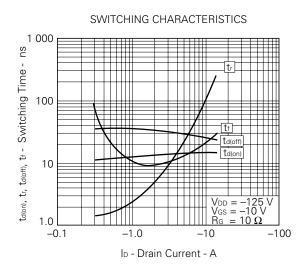


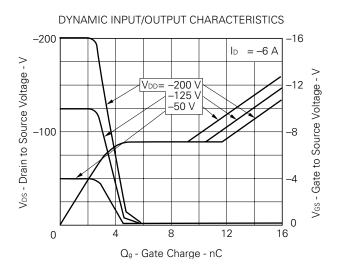


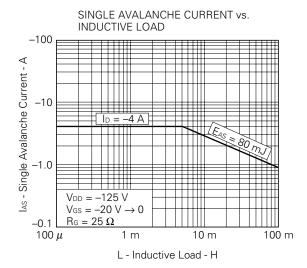


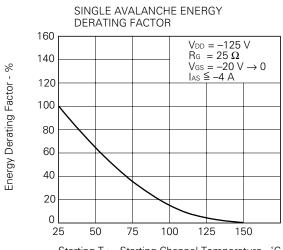












Starting T_{ch} - Starting Channel Temperature - $^{\circ}$ C



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.