HARRIS

HI-508L/HI-509L

Single 8/Differential 4 Channel CMOS Analog Multiplexers With Latches And Overvoltage Protection

FEATURES

- Analog Overvoltage protection
- Resettable Latches ($\overline{RS}$)
- TTL/DTL and CMOS Compatible
- Failsafe for conditions of Overvoltage & Loss of Power
- No SCR Latch-up
- Break-before-make switching
- Microprocessor Bus compatible
- Very low leakage - $I_{D(off)} \leq 4nA$ (typ) over full temp range
- Access time - t_A = 500nS (typ)
- Minimum write pulse width ($\overline{WR}$) = 300 nS
- OFF isolation = −100dB, typ @ 10kHz

DESCRIPTION

These monolithic CMOS multiplexers feature on-board address latches, plus overvoltage protection for the analog inputs and the output as well. Each model includes digital inputs for channel selection and an Enable input for device selection under program control. In addition, Write (WR) and Reset (RS) inputs allow the program to store or clear the channel address.

The overvoltage performance of these multiplexers is particularly useful in redundant systems, where the inputs and output must present a high impedance when power is off. This is achieved by a switch cell with three MOSFET's in series, rather than the conventional transmission gate design.

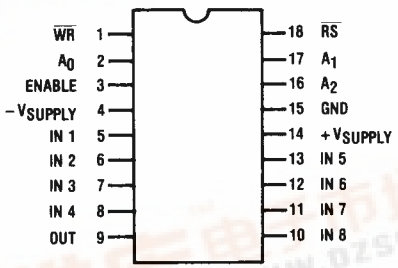
Each channel can withstand overvoltage to +25VDC with respect to ground with power ON or OFF. An OFF channel remains OFF in the presence of overvoltage. If the channel is ON, output voltage is clamped below the supply rail, which protects the load circuit.

The HI-508L offers 8 single-ended channels, and the HI-509L is a 4 channel differential version. The recommended supply voltages are ±15V, though operation at reduced levels or with a single supply may also be implemented. The package is a 18 pin ceramic or plastic DIP.

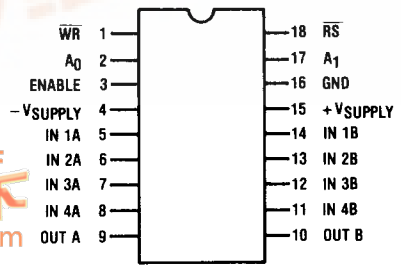
Each product is specified for the commercial temperature range (0°C to 75°C, -5 suffix) and the military range (-55°C to +125°C, -2 suffix). Military high reliability burned-in product is available as a "-8" suffix.

PINOUT

HI-508L

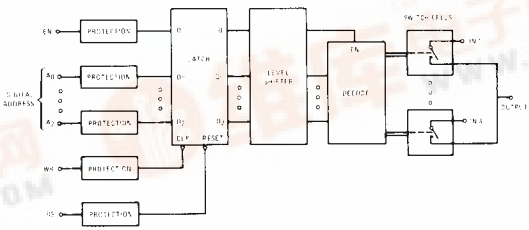


HI-509L

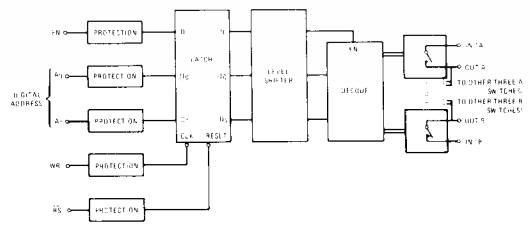


FUNCTIONAL DIAGRAM

HI-508L



HI-509L



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 4 and 14 (15)	44V	Operating Temperature	
Digital Input Overvoltage, V_A, V_{EN}, $V_{\overline{RS}}$, $V_{\overline{WR}}$:			
V supply (+)	+4V	HI-508L/509L-2	−55°C to 125°C
V supply (−)	−4V	HI-508L/509L-5	0°C to 75°C
Analog Overvoltage		Storage Temperature	−65°C to +150°C
Input to Ground	±25VDC		
Total Power Dissipation* (Package)	1200mW	*Derate-8mW/°C above T_A = +75°C	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

+V supply = 15V, −V supply = −15V, V_{AH} (Logic High) = 2.0V, V_{AL} (Logic Low) = 0.8V

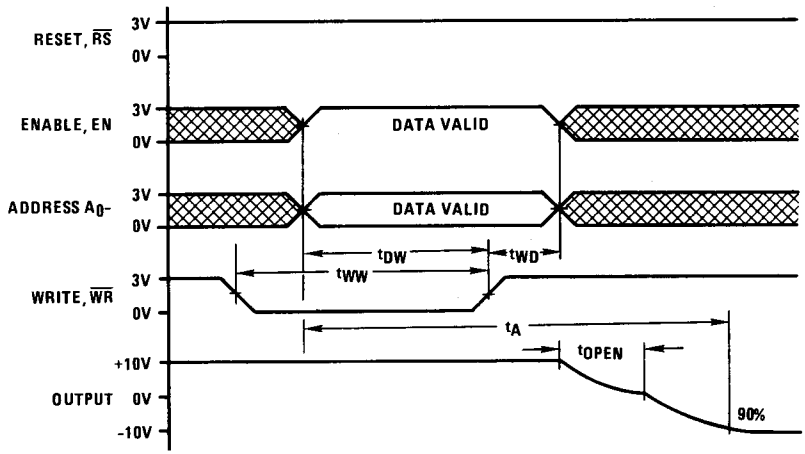
	HI-508L/509L-2 −55°C to +125°C				HI-508L/509L-5 0°C to +75°C			
PARAMETER	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full		±10			±10		V
R_{ON}, ON Resistance (Note 2)	+25°C			1.2			1.5	KΩ
	Full			1.8			1.8	KΩ
ΔR_{ON}, Change In R_{ON} (Note 3) between channels	+25°C		5			5		%
$I_{S(off)}$, OFF input leakage current	+25°C			10			10	nA
	Full		5	50		5	50	nA
$I_{D(off)}$, OFF output leakage current	+25°C			10			10	nA
HI-508L	Full		4	100		4	100	nA
HI-509L	Full		2	50		2	50	nA
$I_{D(On)}$, ON Channel leakage current	+25°C			10			10	nA
HI-508L	Full		5	100		5	100	nA
HI-509L	Full		2	50		2	50	nA
FAULT CHARACTERISTICS								
$I_{S(Off)}$, with Power OFF	Full		10	1000		10	5000	nA
$I_{S(Off)}$, overvoltage (Note 4)	Full		10	750		10	2500	nA
$I_{D(Off)}$, with input over-	+25°C		5			5		nA
voltage applied (Note 4)	Full		10	750		10	2500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full		1.4	0.8		1.4	0.8	V
V_{AH}, Input High Threshold	Full	2.0	1.4		2.0	1.4		V
I_{AH}, Input High Current (Note 5)	Full		10	40		10	40	μA
I_{AL}, Input Low Current (Note 5)	Full		40	200		40	200	μA
DYNAMIC SWITCHING CHARACTERISTICS (Note 6)								
t_a, Access Time	+25°C		0.5	1.0		0.5	1.0	μS
t_{OPEN}, Break-Before-Make	+25°C	.025	0.1		.025	0.1		μS
t_{ON}, (EN), Enable Delay (ON)	+25°C		0.5	1.0		0.5	1.0	μS
t_{OFF}, (EN), Enable	+25°C		0.5	1.0		0.5	1.0	μS
Delay (OFF)								
Settling Time (±0.1%)	+25°C		1.0			1.0		μS
(±0.01%)	+25°C		1.75			1.75		μS
OFF Isolation (Note 7)	+25°C	50	68		50	68		dB
OFF Isolation POWER OFF (Note 8)	+25°C		56			56		dB
$C_{S(Off)}$, Channel Input Cap.	+25°C		5			5		pF
$C_{D(Off)}$, Channel Output Cap.								
HI-508L	+25°C		25			25		pF
HI-509L	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(Off)}$, Input to Output capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation (Note 9)	Full		60	100		60	100	mW
I +, Current Pin 14 (Note 9)	Full		3.7	6.0		3.7	6.0	mA
I −, Current Pin 4 (Note 9)	Full		0.3	0.6		0.3	0.6	mA

NOTES
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ± 10V, I out = -100μA
3. $\Delta R_{ON} = \frac{R_{ON(Max)} - R_{ON(Min)}}{R_{ON(Avg)}}$, V_{IN} = ± 10V
4. Analog Overvoltage = ± 25V
5. I_{AH} and I_{AL} tested at 2.4V and 0.4 V respectively
6. For measurements in this section, input logic levels are 3.0V (High) and 0V (Low).
7. V_{EN} = 0.8V, R_L = 1KΩ, C_L = 15pF, V_S = 7Vrms, f = 500kHz. Off isolation = 20 log $\frac{|V_D|}{|V_S|}$. Worst case isolation on channel 4 due to proximity of the output pin(s).
8. V+ , V- = 0V, R_L = 1KΩ, C_L = 50pF, V_S = 3Vrms, f = 500 kHz
9. See Test Circuit #8 for high toggle frequency applications.

MINIMUM TIMING REQUIREMENTS

PARAMETER	MIN LIMITS FULL TEMP RANGE	UNITS
t_{WW}, Write Pulse Width	300	nS
t_{DW}, A, EN Data Valid To WRITE (Stabilization Time)	225	nS
t_{WD}, A, EN Data Valid After Write (hold Time)	100	nS
t_{RS}, RESET pulse width	400	nS
t_{OFF} ($\overline{RS}$) Reset Delay	1000	nS
t_{ON} ($\overline{WR}$) Write Turn-on Time	1000	nS

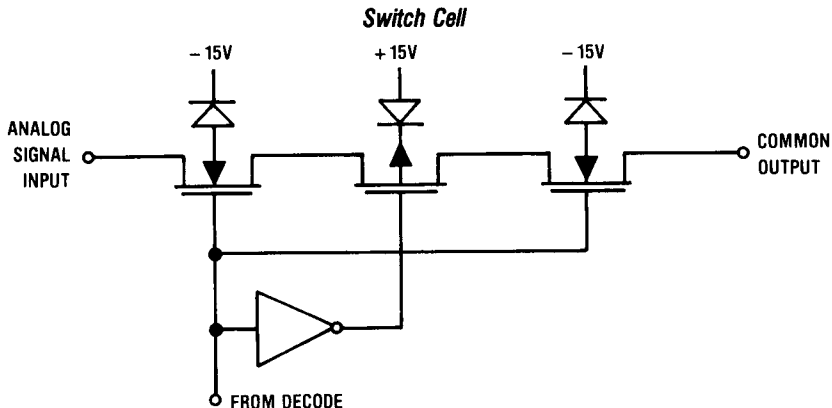
TIMING REQUIREMENTS



1. $+V_{SUPPLY}$ = +15V; $-V_{SUPPLY}$ = -15V.
2. Logic Levels: V_{AL} = 0V; V_{AH} = +3.0V.
3. Time intervals are measured between 50% levels unless otherwise noted.
4. Minimum values for $t_{\overline{RS}}$, t_{DW}, t_{WW} and t_{WD} are guaranteed separately but not simultaneously.

Figure 1

SCHEMATIC DIAGRAM



TRUTH TABLES

508L

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL
X	X	X	L	L	H	None
X	X	X	X	↓	H	Previous ON Channel.
X	X	X	X	X	L	None (latches cleared)
L	L	L	H	L	H	Channel 1
L	L	H	H	L	H	Channel 2
L	H	L	H	L	H	Channel 3
L	H	H	H	L	H	Channel 4
H	L	L	H	L	H	Channel 5
H	L	H	H	L	H	Channel 6
H	H	L	H	L	H	Channel 7
H	H	H	H	L	H	Channel 8

509L

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL PAIR
X	X	L	L	H	None
X	X	X	↓	H	Previous ON Channel.
X	X	X	X	L	None (latches cleared)
L	L	H	L	H	Channel 1A and 1B
L	H	H	L	H	Channel 2A and 2B
H	L	H	L	H	Channel 3A and 3B
H	H	H	L	H	Channel 4A and 4B

DESCRIPTION AND APPLICATION

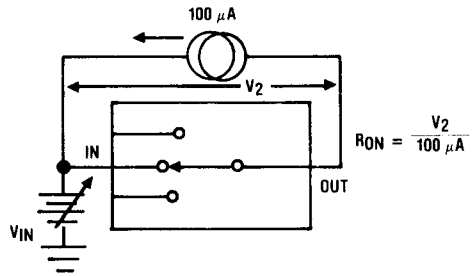
The switch cell of HI-508L/509L has a different structure than earlier Harris designs (HI-508, HI508A). The new switch (Figure 2) consists of an N-channel, P-channel and N-channel MOSFET in series, as opposed to the transmission gate configuration with an N and P-channel device in parallel. The series N-P-N switch offers higher Off isolation with power off, and better fault performance. Channel overvoltage protection is inherent since one of the three MOSFETs turn off in the presence of overvoltage. This turn-off process begins well below the supply rail so the V_{IN} range is less than the power supply range. Electrical performance is guaranteed to ±10V for each channel, and the usable range extends above ±11 Volts.

The address inputs A_0, A_1, A_2, and ENABLE are latched into an internal buffer when $\overline{WR}$ goes high. Each latch output is level shifted into the decode section, which activates the appropriate channel. The device may be reset (all channels OFF) by taking $\overline{RS}$ low. Usually, $\overline{RS}$ is tied to the system RESET line, to assure that all channels are OFF following a turn-on of power. The reset function overrides all others, just as $\overline{WR}$ overrides the address inputs (A_0-A_2 and EN are ignored when $\overline{WR}$ is high). With $\overline{WR}$ low and $\overline{RS}$ high, the switches respond immediately to a change in channel address; i.e., the latches are "transparent". Refer to Figure 1.

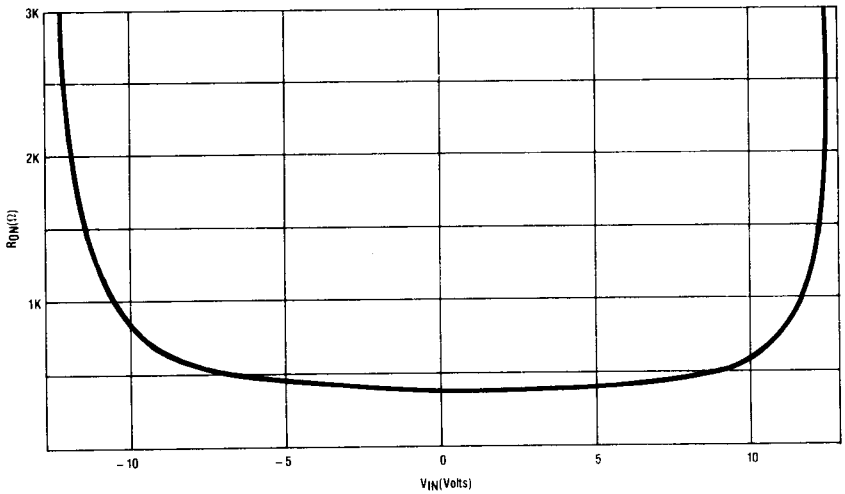
For additional Applications information please see AN 545.

TEST CIRCUIT NO. 1

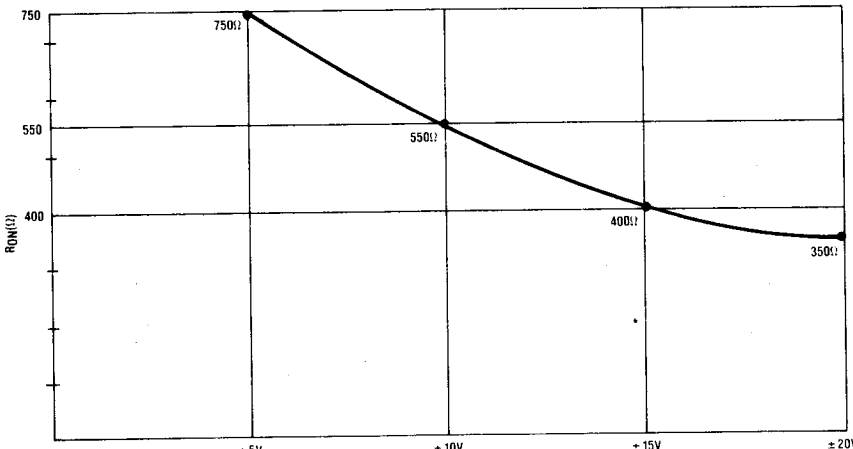
ON RESISTANCE vs.
INPUT SIGNAL LEVEL



VIN vs. RON

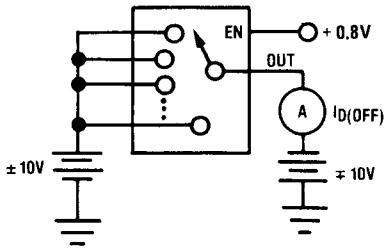


RON vs. POWER SUPPLY VOLTAGES
INPUT = 0V

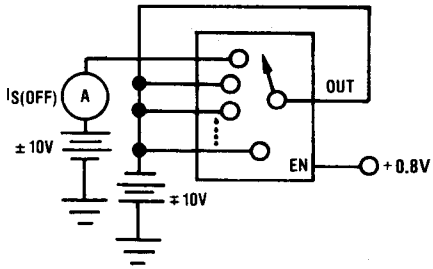


HI-508L TEST CIRCUITS

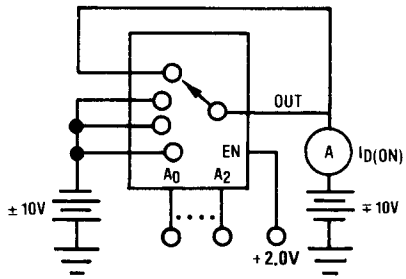
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*



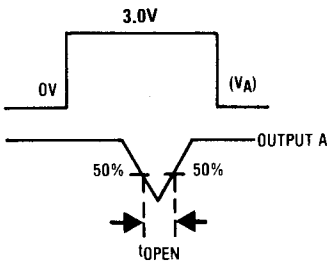
TEST CIRCUIT NO. 4*



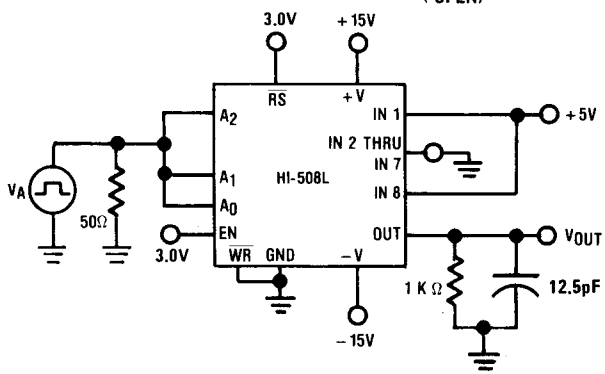
*Two measurements per channel:
+ 10V/– 10V and – 10V/+ 10V.
(Two measurements per device for $I_{D(OFF)}$:
+ 10V/– 10V and – 10V/+ 10V.)

TEST CIRCUIT NO. 5

ADDRESS DRIVE

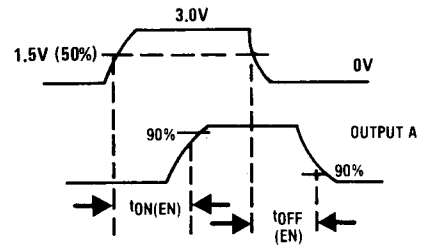


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

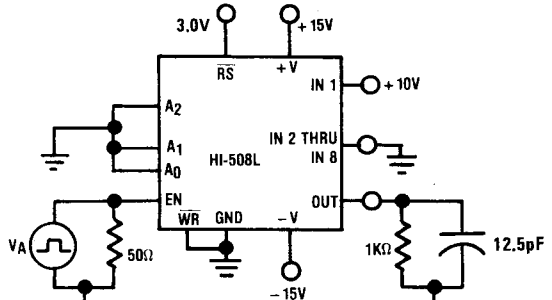


TEST CIRCUIT NO. 6

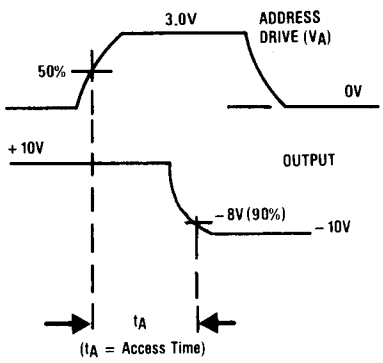
ENABLE DRIVE



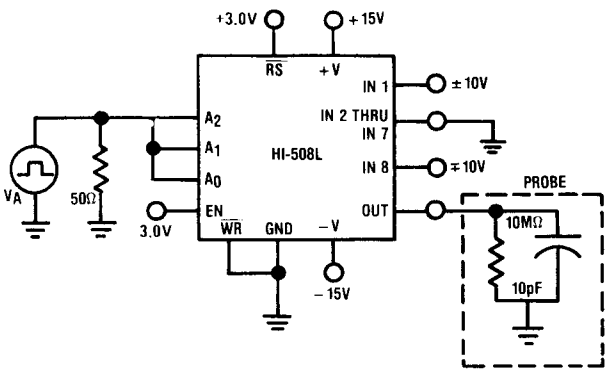
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



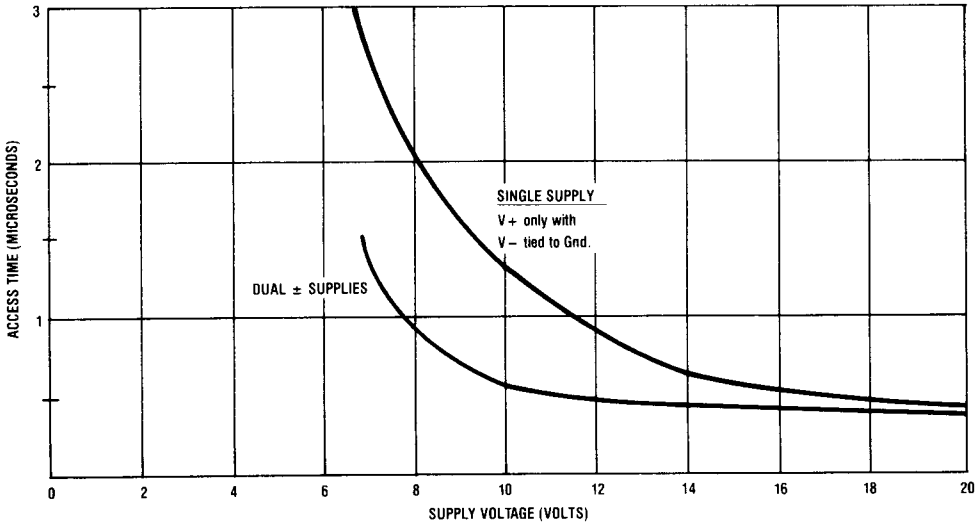
TEST CIRCUIT NO. 7



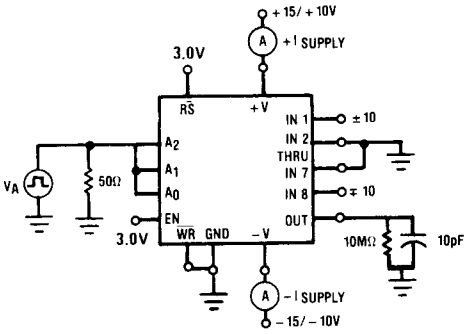
ACCESS TIME



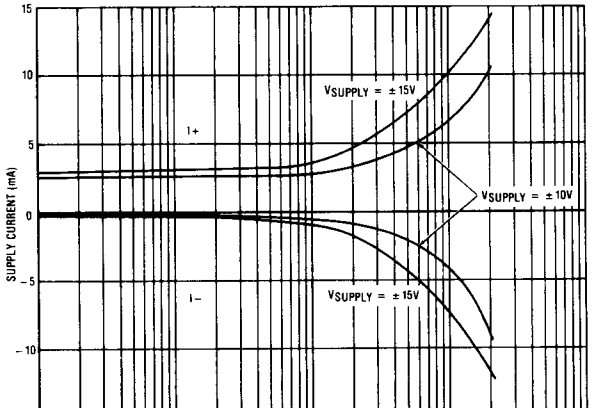
ACCESS TIME vs. SUPPLY VOLTAGE



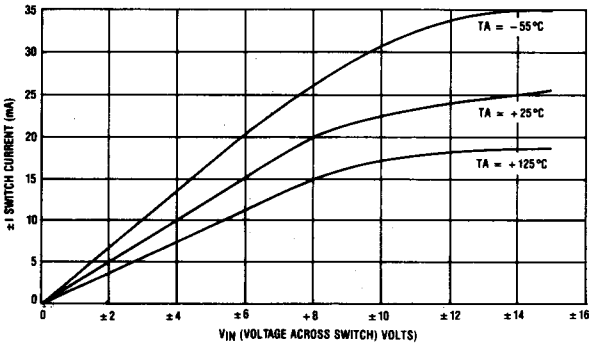
TEST CIRCUIT NO. 8
SUPPLY CURRENTS vs. TOGGLE FREQUENCY

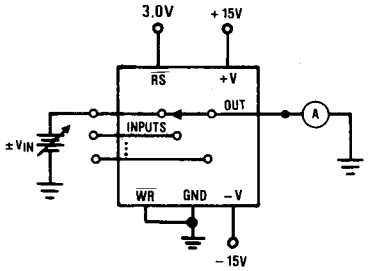


SUPPLY CURRENT vs. TOGGLE FREQUENCY

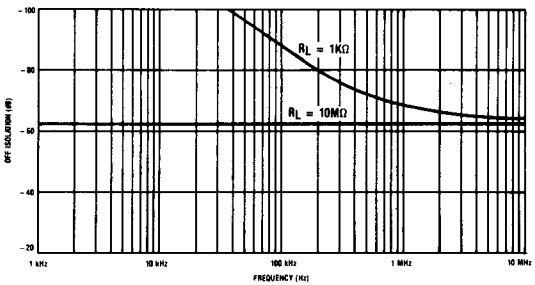


TEST CIRCUIT NO. 9
ON CHANNEL CURRENT vs. INPUT VOLTAGE

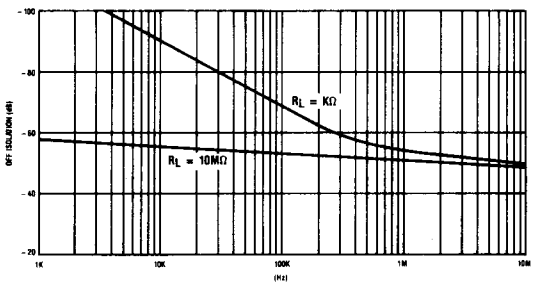




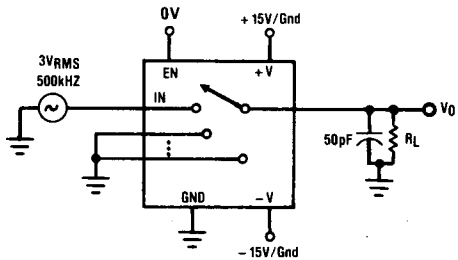
OFF ISOLATION vs. FREQUENCY POWER ON



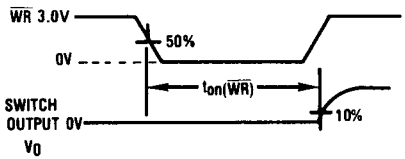
OFF ISOLATION vs. FREQUENCY (POWER OFF)



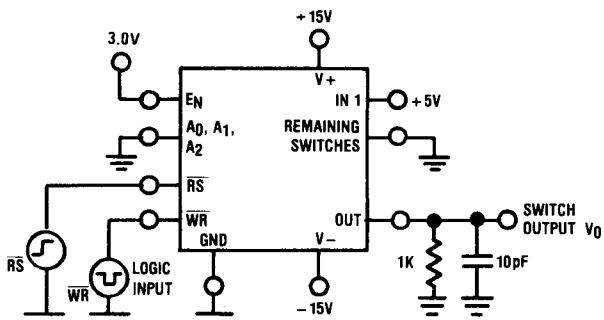
TEST CIRCUIT NO. 10
OFF ISOLATION



TEST CIRCUIT 11
WRITE TURN-ON TIME $t_{ON(\overline{WR})}$

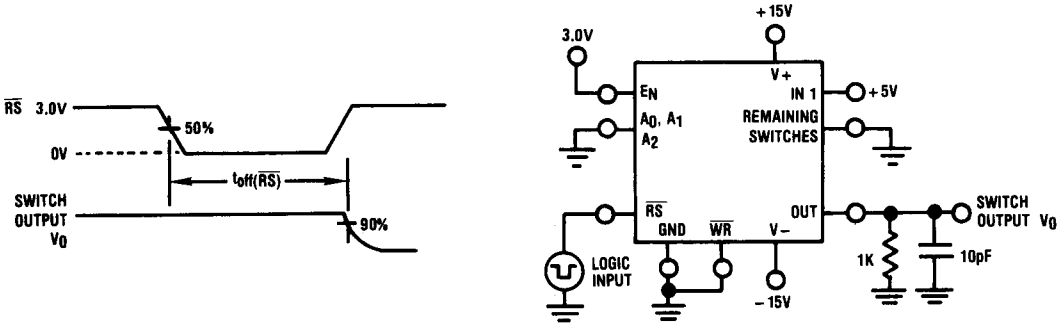


DEVICE MUST BE RESET PRIOR TO APPLYING $\overline{WR}$ PULSE

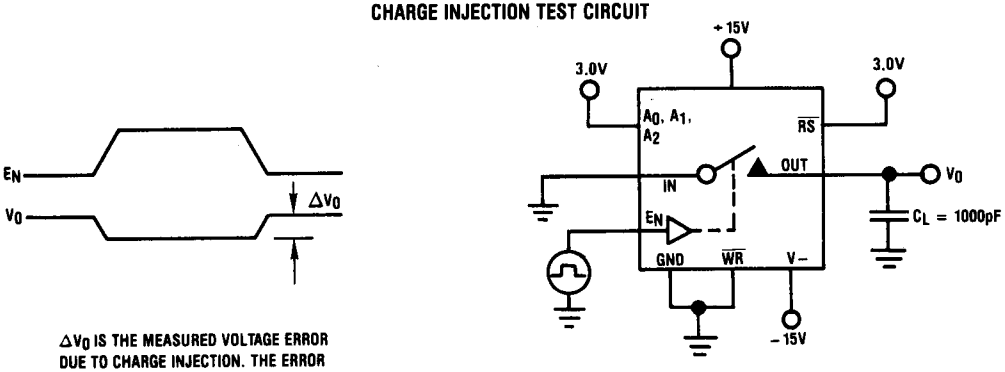


HI-508L TEST CIRCUITS

TEST CIRCUIT 12
RESET TURN-OFF TIME $t_{off(\overline{RS})}$



TEST CIRCUIT 13
CHARGE INJECTION TEST CIRCUIT



ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L X \Delta V_O$.

DIE CHARACTERISTICS

Transistor Count	397
Die Size	124x114mils.
Thermal Impedance	
θ_{JA}	80°C/W
θ_{JC}	22°C/W
Tie Substrate to:	$-V_{Supply}$
Process	CMOS-DI