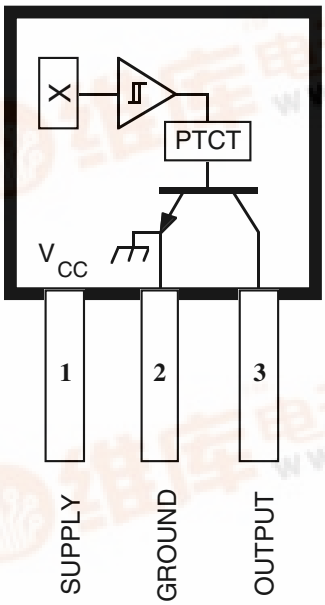
3197

Data Sheet
27609.10A

PROTECTED, HIGH-TEMPERATURE, OPEN-COLLECTOR HALL-EFFECT LATCH



Dwg. PH-003-2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}
(100 ms) ..... **115 V***
(continuous) ..... **28 V***
Reverse Battery Voltage, V_{RCC}
(100 ms) ..... **-100 V**
(continuous) ..... **-35 V**
Magnetic Flux Density, B ..... **Unlimited**
Output OFF Voltage, V_{OUT} ..... **26 V**
Reverse Output Voltage V_{OUT} ..... **-0.5 V**
Continuous Output Current,
I_{OUT} ..... **35 mA***
Reverse Output Current,
I_{OUT} ..... **-100 mA**
Package Power Dissipation,
P_D ..... **See Graph**
Junction Temperature, T_J ..... **170°C**
Operating Temperature Range,
T_A ..... **-40°C to +150°C**
Storage Temperature, T_S ..... **170°C**

*Fault condition, internal overvoltage shutdown above 28 V; output current limited above 35 mA.

These open-collector Hall-effect latches are capable of sensing magnetic fields while using an unprotected power supply. The A3197LLT and A3197LU can provide position and speed information by providing a digital output for magnetic fields that exceed their predefined switch points. These devices operate down to zero speed and have switch points that are designed to be extremely stable over a wide operating temperature and voltage range. The latching characteristics make them ideal for use in pulse counting applications when used with a multi-pole ring magnet. Thermal and output short-circuit protection allow an increased wiring harness fault tolerance. The temperature compensated switch points, the wide operating voltage range, and the integrated protection make these devices ideal for use in automotive applications such as transmission speed sensors and integrated wheel bearing speed sensors.

Each monolithic device contains an integrated Hall-effect transducer, a temperature-compensated comparator, a voltage regulator, and a buffered 35 mA output sink stage. Supply protection is made possible by the integration of overvoltage and undervoltage shutdown circuitry that monitor supply fault conditions and shut down the IC. Noise shutdown circuitry (patent applied for) prevents the propagation of supply transients to the logic load. Output protection circuitry includes a current limit loop that limits the maximum output sink current, and thermal protection circuitry that shuts down the device during an over-heating condition such as with a shorted load.

The A3197LLT and A3197LU are rated for operation over an extended temperature range of -40°C to +150°C. They are supplied in a three-lead SIP (suffix 'U') or a surface-mount SOT-89 (suffix 'LT').

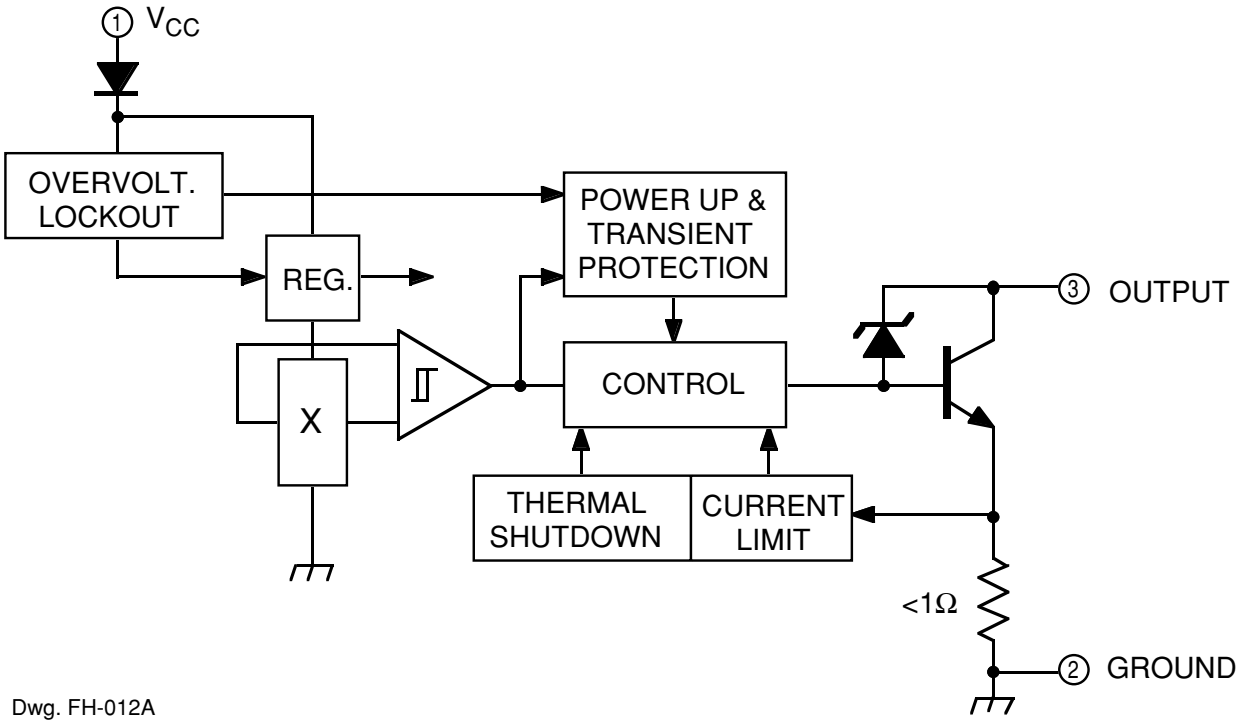
FEATURES

- Internal Protection For Automotive (ISO/DIN) Transients
- Operation From Unregulated Supply
- Reverse Battery Protection
- Undervoltage Lockout
- Supply Noise-Suppression Circuitry
- Output Short-Circuit Protection
- Output Zener Clamp
- Thermal Protection
- Symmetrical Latching Switch Points
- Operable with Multipole Ring Magnets

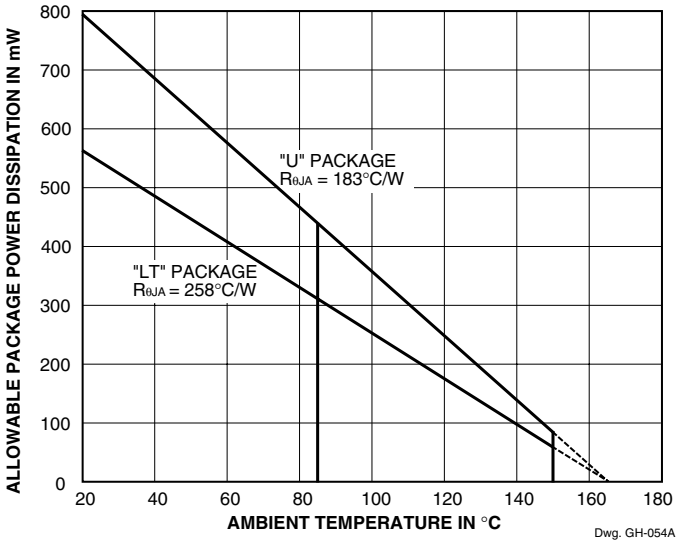
Always order by complete part number, e.g., **A3197LU**.

3197
PROTECTED, HIGH-TEMP., OPEN-COLLECTOR HALL-EFFECT LATCH

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-012A



Dwg. GH-054A

NOTE – Permitted duty cycle will be less than 100% at maximum ambient temperature with high supply voltages, i.e., $T_A \geq 140°C$, $V_{CC} \geq 12$ V, and the "LT" package. The thermal shutdown circuitry does not protect the device from these stresses (see Internal Protective Features).

ELECTRICAL CHARACTERISTICS
over operating voltage and temperature range (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating (but V_{CC} x I_{CC} vs T_A limited)	$V_{CC(UV)}$	12	26	V
Overvoltage Shutdown*	$V_{CC(OV)}$	$B > B_{OP}$	28	—	55	V
Undervoltage Shutdown*	$V_{CC(UV)}$	$B > B_{OP}$	3.7	—	4.5	V
Output Voltage, On	$V_{OUT(SAT)}$	$B > B_{OP}$, I_{OUT} = 30 mA, V_{CC} = 16 V	—	0.2	0.5	V
Output Leakage Current	I_{OFF}	V_{OUT} = 26 V	—	—	5.0	µA
Output Clamp Voltage	$V_{OUT(CLMP)}$	$B < B_{RP}$, V_{CC} = 115 V*, I_{OUT} = 0	28	32	40	V
Output Current Limit	I_{OUTMAX}	$B > B_{OP}$, V_{OUT} = 12 V	35	50	70	mA
Supply Current	I_{CC}	$B < B_{RP}$, V_{CC} = 24 V, I_{OUT} = 0	—	5.2	9.0	mA
		$B > B_{OP}$, V_{CC} = 24 V, I_{OUT} = 20 mA	—	7.8	12	mA
		V_{CC} = +115 V*	—	8.0	17	mA
Reverse Battery Current*	I_{RCC}	V_{RCC} = -35 V*	—	-0.5	-5.0	mA
		V_{RCC} = -100 V*	—	-2.0	-10	mA
Output Rise Time	t_r	C_L = 20 pF, R_L = 330 Ω, V_{BB} = 12 V	—	0.05	2.0	µs
Output Fall Time	t_f	C_L = 20 pF, R_L = 330 Ω, V_{BB} = 12 V	—	0.30	5.0	µs
Thermal Shutdown Temp.*	T_J		165	—	190	°C
Package Thermal Resist.	$R_{\theta JA}$	"LT" Package	—	258	—	°C/W
		"U" Package	—	183	—	°C/W

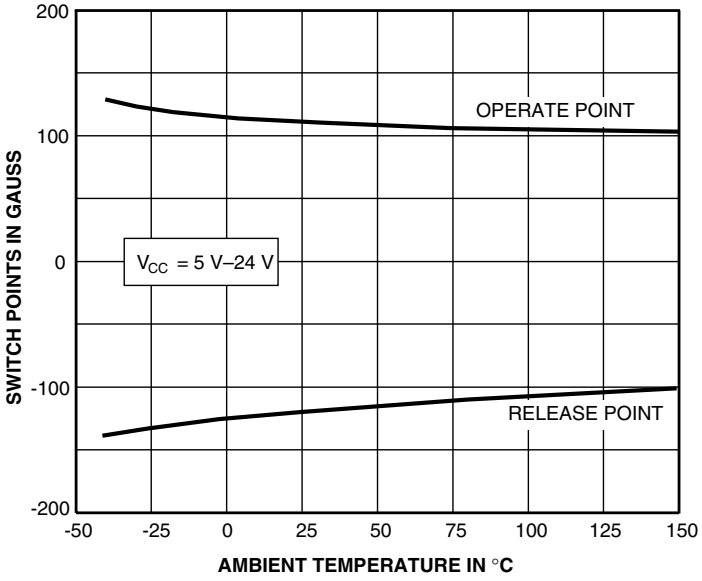
MAGNETIC CHARACTERISTICS over operating voltage range (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operate Point	B_{OP}	T_A = -40°C	60	130	200	G
		T_A = +25°C	50	110	160	G
		T_A = +150°C	40	105	150	G
Release Point	B_{RP}	T_A = -40°C	-200	-140	-60	G
		T_A = +25°C	-160	-120	-50	G
		T_A = +150°C	-150	-100	-40	G
Hysteresis (B_{OP} - B_{RP})	B_{hys}	T_A = -40°C	150	270	—	G
		T_A = +25°C	130	230	—	G
		T_A = +150°C	110	205	—	G

NOTES: B_{OP} = magnetic operate point (output turns ON); B_{RP} = magnetic release point (output turns OFF).
As used here, negative flux densities are defined as less than zero (algebraic convention).
Typical values are at T_A = +25°C and V_{CC} = 12 V (unless otherwise specified).
* Fault condition. Device is shut down and operation is not possible.

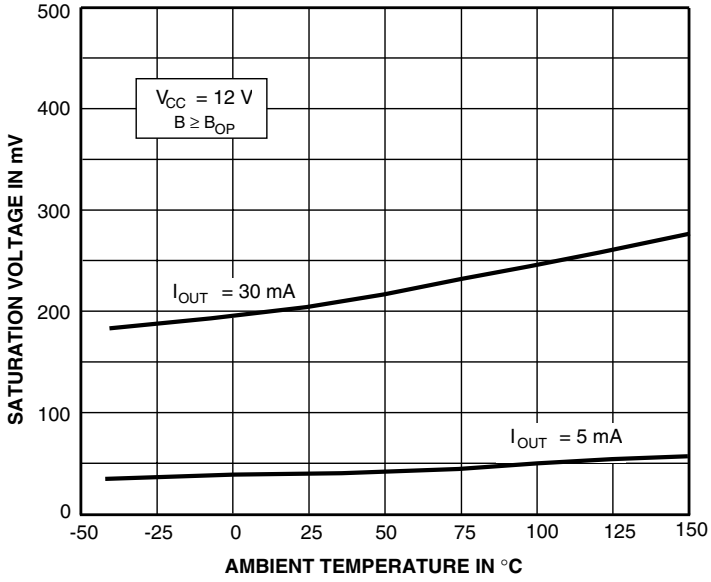
TYPICAL OPERATING CHARACTERISTICS

Switch Points



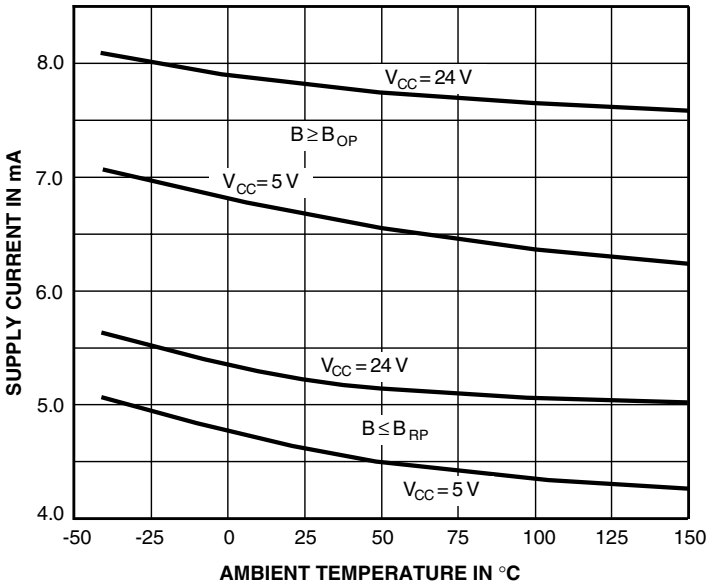
Dwg. GH-052-2

Output Saturation Voltage



Dwg. GH-040-3

Supply Current



Dwg. GH-028-3

3197
PROTECTED, HIGH-TEMP., OPEN-COLLECTOR HALL-EFFECT LATCH

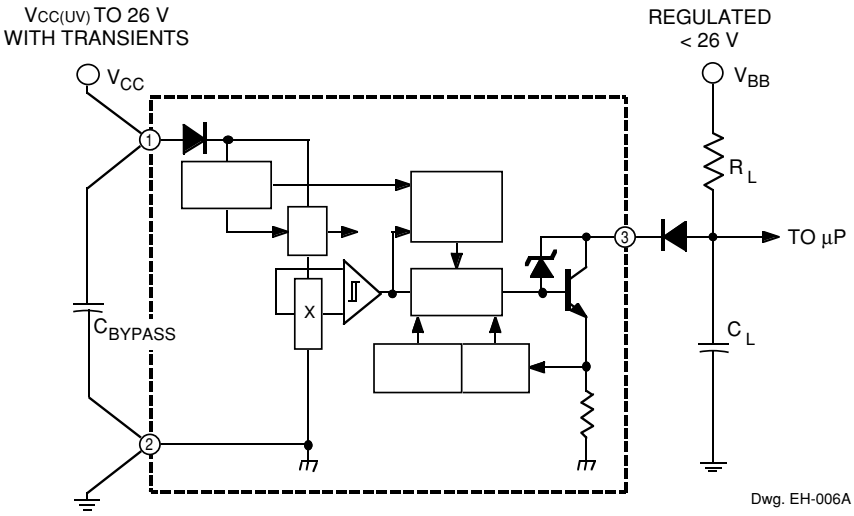
OPERATION

In operation, the output transistor is OFF until the strength of the magnetic field perpendicular to the surface of the chip exceeds the threshold or operate point (B_{OP}). When the field strength exceeds B_{OP}, the output transistor switches ON (a logic low) and is capable of sinking 35 mA of current.

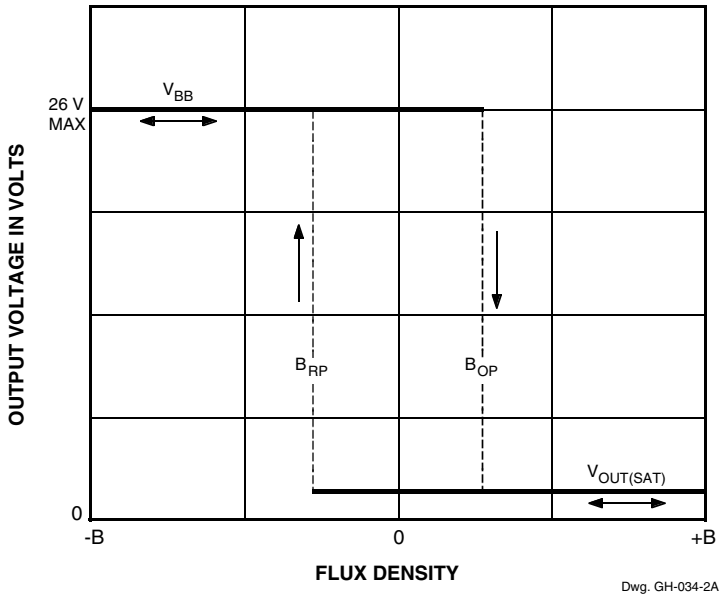
The output transistor switches OFF (a logic high) when magnetic field reversal results in a magnetic flux density below the OFF threshold (B_{RP}). This is illustrated in the transfer characteristics graph. Note that the device latches; that is, a south pole of sufficient strength will turn the device ON. Removal of the south pole will leave the device ON. The presence of a north pole of sufficient strength is required to turn the device OFF.

The switch points increase in sensitivity with increasing temperature to compensate for the typical ferrite magnet temperature characteristic. The simplest form of magnet that will operate these devices is a ring magnet. Other methods of operation are possible.

TEST CIRCUIT AND TYPICAL APPLICATION

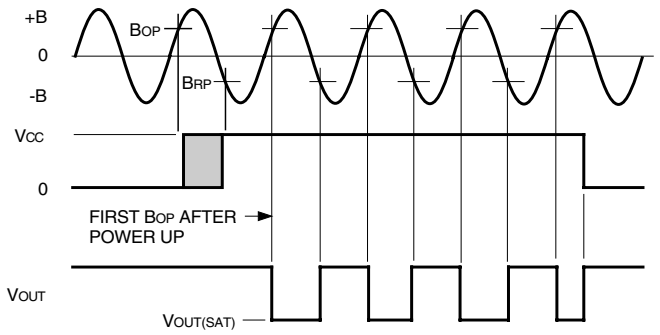


Dwg. EH-006A



Dwg. GH-034-2A

Power Up Reset. These devices are designed to power up with the output OFF without regard to any magnetic field applied. The output will remain OFF until the flux is reduced to below B_{RP} (S-N transition) and then B_{OP} is exceeded, depending on the turn-on state of the internal latches.

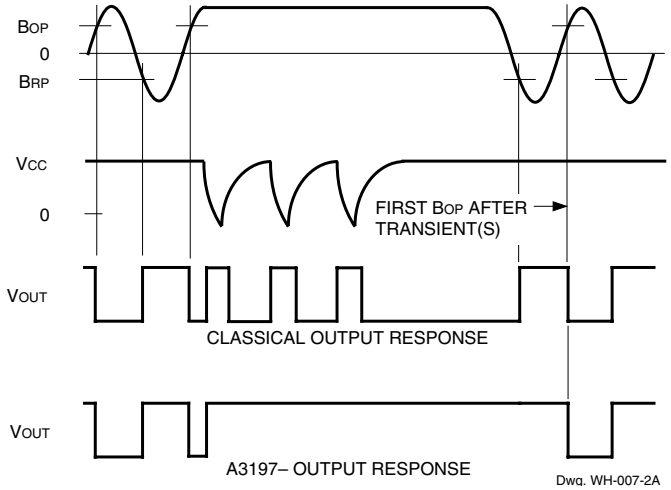


Dwg. WH-006

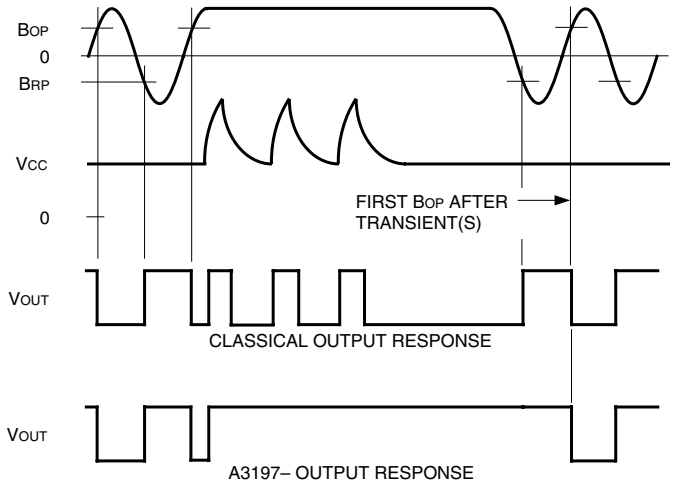
Power Supply Transtransients (Noise); Overvoltage and Undervoltage Lockout. Even in protected devices, positive and negative power supply transients that would not normally cause physical damage can cause logic errors in control systems. The A3197LT and A3197LU include noise suppression features to prevent this.

In a typical application, where the output is externally pulled up to a regulated voltage <28 V, the effects of power supply transients on the device output are suppressed by turning the output driver OFF during the first undervoltage, $V_{CC(UV)}$, (or negative) condition, or first overvoltage (positive) condition, $V_{CC(OV)}$, and maintaining a power up reset mode until normal power is restored. Note that after the initial transient, the output does not change logic state during subsequent power supply noise pulses.

An external 0.1 µF to 0.5 µF capacitor, with good high-frequency characteristics, should be connected between terminals 1 and 2 to bypass high-voltage noise and reduce EMI susceptibility.



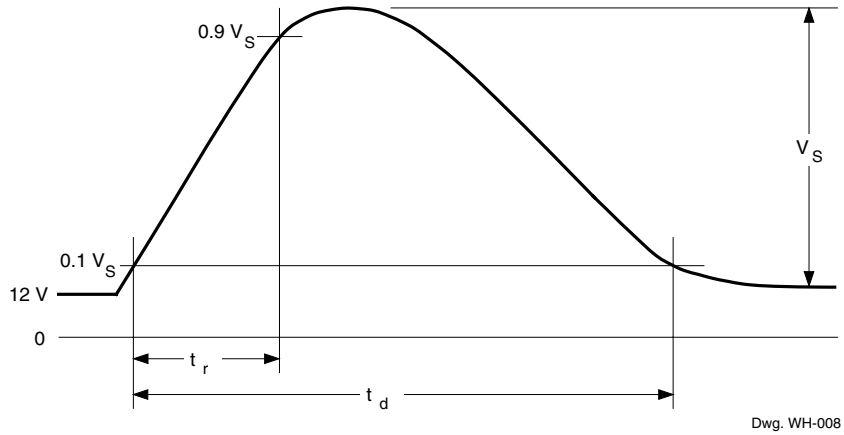
Dwg. WH-007-2A



Dwg. WH-007-1A

INTERNAL PROTECTIVE FEATURES

ISO Pulse No.	Test	Test Conditions (over operating temperature range)
1	Inductive Turn Off (Negative)	V_S = -100 V, R_S = 10 Ω, t_r = 1 µs, t_d = 2 ms
2	Inductive Turn Off (Positive)	V_S = 100 V, R_S = 10 Ω, t_r = 1 µs, t_d = 50 µs
3a	Capacitive/Inductive Coupling (Neg)	V_S = -150 V, R_S = 50 Ω, t_r = 50 ns, t_d = 100 ns
3b	Capacitive/Inductive Coupling (Pos)	V_S = 100 V, R_S = 50 Ω, t_r = 50 ns, t_d = 100 ns
4	Reverse Battery	V_S = -14 V, t_d = 20 s
5	Load Dump (ISO)	V_S = 86.5 V, R_S = 0.5 Ω, t_r = 5 ms, t_d = 400 ms
	(DIN)	V_S = 120 V, R_S = 0.5 Ω, t_r = 100 ns, t_d = 400 ms
6	Ignition Coil Disconnect EXTERNAL PROTECTION REQ'D	V_S = -300 V, R_S = 30 Ω, t_r = 60 µs, t_d = 300 µs
7	Field Decay (Negative)	V_S = -80 V, R_S = 10 Ω, t_r = 5 ms, t_d = 100 ms



Dwg. WH-008

Power supply voltage transients, or device output short circuits, may be caused by faulty connectors, crimped wiring harnesses, or service errors. To prevent catastrophic failure, internal protection against overvoltage, reverse voltage, output overloads, and thermal stress have been incorporated to meet the automotive 12 volt system protection requirements of ISO DP7637/1 and DIN 40839-1. A series-blocking diode or current-limiting resistor is required in order to survive pulse number six.

Output Overloads. Current through the output transistor is sensed with a low-value on-chip aluminum resistor. The voltage drop across this resistor is fed back to control the base drive of the output stage. This feedback prevents the output transistor from exceeding its maximum current density rating by limiting the output current to between 35 mA and 70 mA. Under short-circuit conditions, the device will dissipate an increased amount of power ($P_D = V_{OUT} \times I_{LIMIT}$) and the output transistor will be thermally stressed.

Thermal Stress. When thermal stresses (either internal or external) cause the junction temperature to exceed +165°C, thermal shutdown of the output transistor is activated. The thermal shutdown circuitry only provides protection against thermal stresses caused by increased power dissipation of the output transistor.

Overvoltage. The device protects itself against high-voltage transients by shutting OFF all supply-referenced active components, reducing the supply current, and minimizing device power dissipation. Overvoltage shutdown can occur anywhere between 28 V and 55 V and device operation above 28 V cannot be recommended. Under a sustained overvoltage, the device may be required to dissipate an increased amount of power ($P_D = V_{CC} \times I_{CC}$) and the device may be thermally stressed (see above).

Output Voltage. The output is clamped with an on-chip Zener diode to limit the maximum output voltage that can occur during overvoltage faults or when switching an inductive load.

When any fault condition is removed, the device returns to normal operating mode.

CRITERIA FOR DEVICE QUALIFICATION

All Allegro sensors are subjected to stringent qualification requirements prior to being released to production. To become qualified, except for the destructive ESD tests, no failures are permitted.

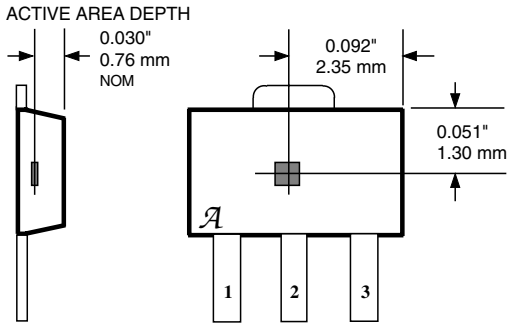
Qualification Test	Test Method and Test Conditions	No. of Lots	Test Length	Samples Per Lot	Comments
Biased Humidity	JESD22-A101 T_A = 85°C, RH = 85%	3	1200 hrs	116	Device biased for minimum power
High-Temperature Operating Life	JESD22-A108 T_A = 150°C, T_J = 165°C	3	1200 hrs	116	
Surge Operating Life	JESD22-A108 T_A = 175°C, T_J = 190°C	1	504 hrs	116	
Pressure Cooker, Unbiased	JESD22-A102, Method C	3	96 hrs	77	
Storage Life	MIL-STD-883, Method 1008 T_A = 170°C	1	1200 hrs	77	
Temperature Cycle	MIL-STD-883, Method 1010	3	1000 cycles	153	
ESD Human Body Model	MIL-STD-883, Method 3015	1	Pre/Post Reading	3 per test	Test to failure HBM > 16 kV
ESD Machine Model		1	Pre/Post Reading	3 per test	Test to failure MM > 800 V

3197
PROTECTED, HIGH-TEMP., OPEN-COLLECTOR HALL-EFFECT LATCH

SENSOR LOCATIONS

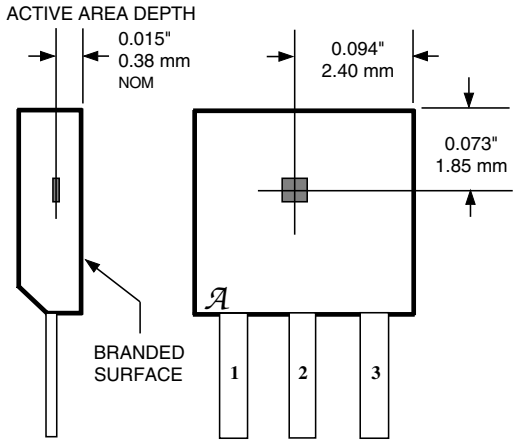
(±0.005" [0.13 mm] die placement)

SUFFIX "LT"



Dwg. MH-008-5A

SUFFIX "U"



Dwg. MH-002-12A

APPLICATIONS INFORMATION

The A3197LLT and A3197LU latches have been optimized for use in automotive ring magnet sensing applications. Such applications include transmission speed sensors, motor position encoders, and wheel bearing speed sensors. Special care has been taken to optimize the operation of these devices in automotive subsystems that require ISO DP9637 protection but NOT operation. Undervoltage lockout is included to prevent propagation of false logic pulses during low battery, cold-start conditions. Noise suppression is included to prevent false switching of the device when subjected to ISO transients. Short-circuit protection is included to prevent damage caused by pinched wiring harnesses.

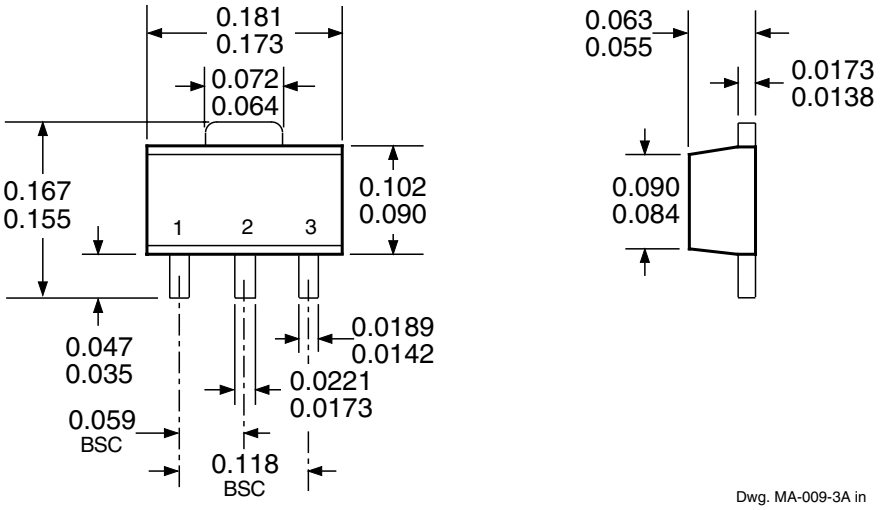
A typical application consists of a ferrite ring magnet located on a rotating shaft. Typically, this shaft is attached to the transmission, the sensor is mounted on a board, with care being taken to keep a tight tolerance on the air gap between the package face and the magnet. The device will provide a change in digital state at the transition of every magnetic pole and, thus, give an indication of the transmission speed. The high magnetic hysteresis allows the device to be immune to vibration of the magnet shaft and relatively good duty cycles can be obtained.

Hall effect applications information is available in the "Hall-Effect IC Applications Guide", which can be found in the *Allegro MicroSystems Electronic Data Book*, AMS-702, or *Application Note* 2770, or at

www.allegromicro.com.

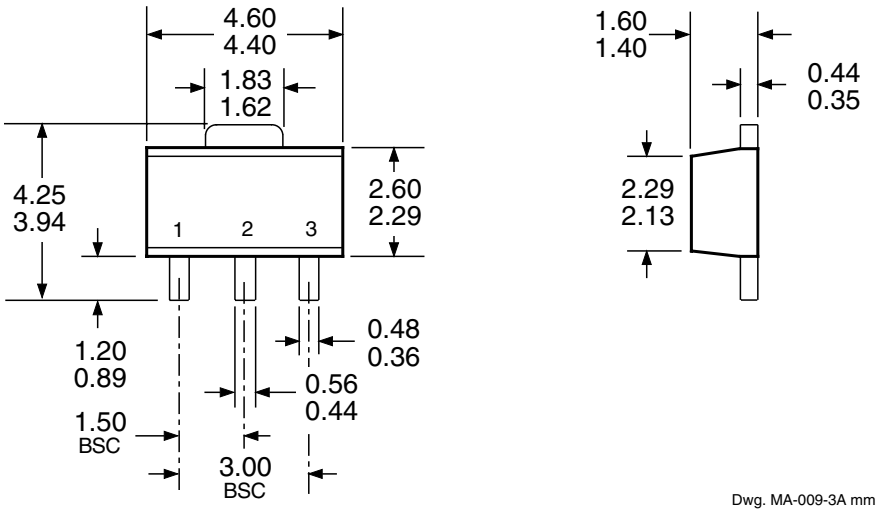
A3197ELT and A3197LLT

Dimensions in Inches
(for reference only)



Dwg. MA-009-3A in

Dimensions in Millimeters
(controlling dimensions)

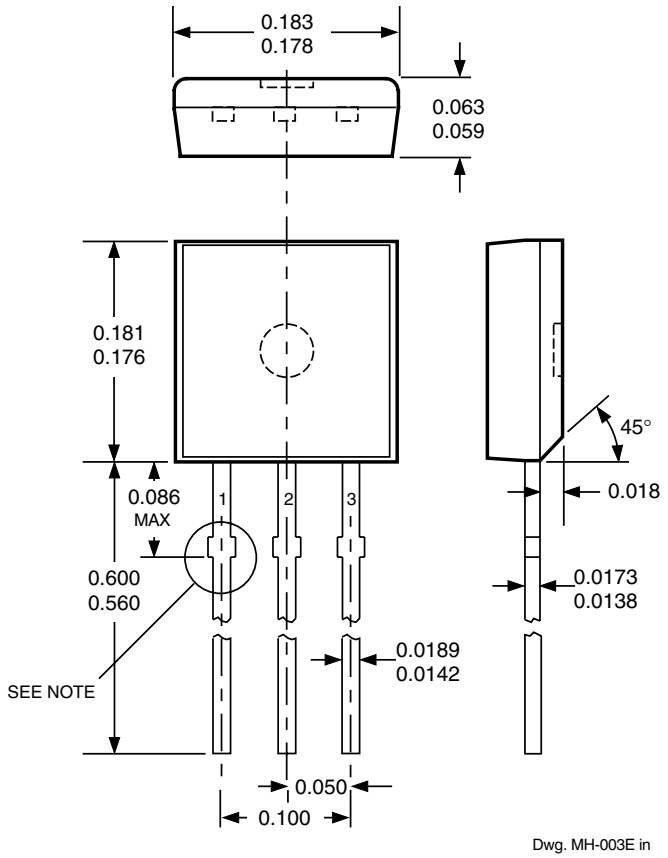


Dwg. MA-009-3A mm

NOTE — Exact body and lead configuration at vendor's option within limits shown.

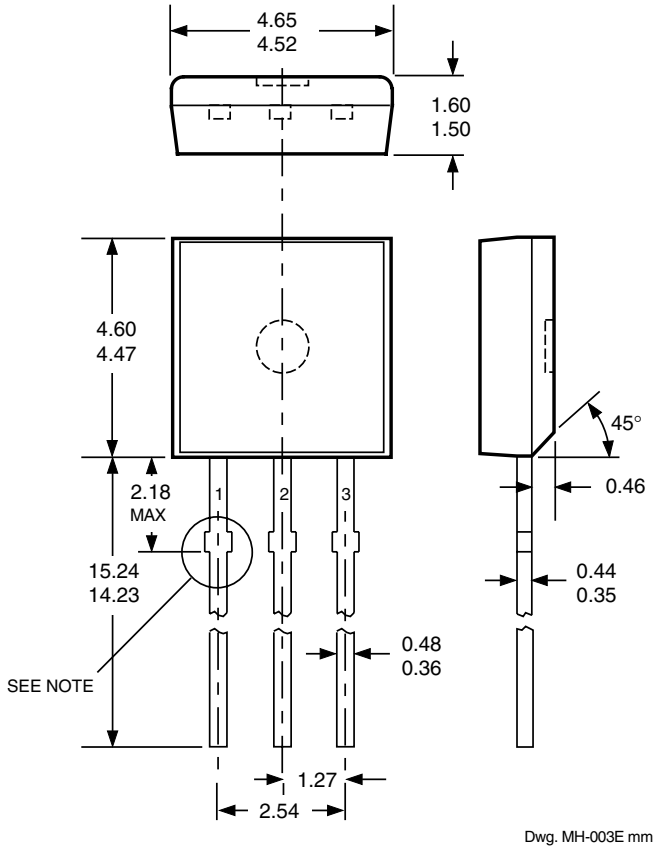
A3197EU and A3197LU

Dimensions in Inches
(controlling dimensions)



Dwg. MH-003E in

Dimensions in Millimeters
(for reference only)



Dwg. MH-003E mm

NOTES: 1. Tolerances on package height and width represent allowable mold offsets.
Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
5. Where no tolerance is specified, dimension is nominal.

3197
PROTECTED, HIGH-TEMP., OPEN-COLLECTOR HALL-EFFECT LATCH

The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro products are not authorized for use as critical components in life-support appliances, devices, or systems without express written approval.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties that may result from its use.

115 Northeast Cutoff, Box 15036