

DATA SHEET

74ABT833

Octal transceiver with parity generator/checker (3-State)

Product specification

1993 Jun 21

IC23 Data Handbook

Octal transceiver with parity generator/checker (3-State)

74ABT833

FEATURES

- Low static and dynamic power dissipation with high speed and high output drive
- Open-collector ERROR output with flag register
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up/down 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT833 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT833 is an octal transceiver with a parity generator/checker and is intended for bus-oriented applications.

When Output Enable A ($\overline{OE}A$) is High, it will place the A outputs in a high impedance state. Output Enable B ($\overline{OE}B$) controls the B outputs in the same way.

The parity generator creates an odd parity output (PARITY) when $\overline{OE}B$ is Low. When $\overline{OE}A$ is Low, the parity of the B port, including the PARITY input, is checked for odd parity. When an error is detected, the error data is sent to the input of a storage register. If a Low-to-High transition happens at the clock input (CP), the error data is stored in the register and the Open-collector error flag (ERROR) will go Low. The error flag register is cleared with a Low pulse on the \overline{CLEAR} input.

If both $\overline{OE}A$ and $\overline{OE}B$ are Low, data will flow from the A bus to the B bus and the part is forced into an error condition which creates an inverted PARITY output. This error condition can be used by the designer for system diagnostics.

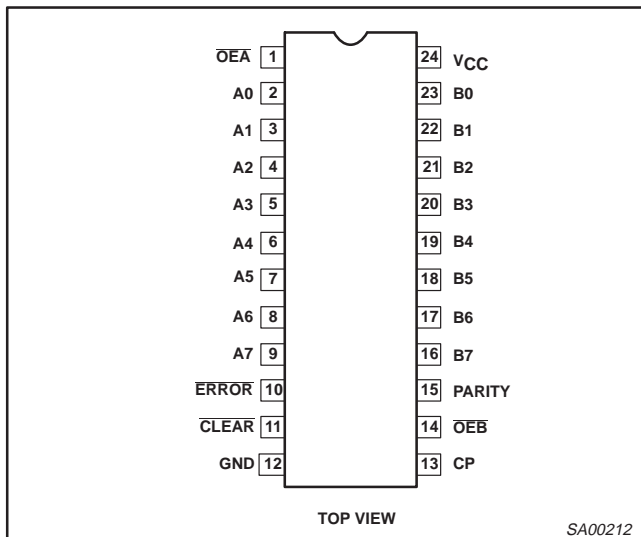
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25^{\circ}C; GND = 0V$ | TYPICAL | UNIT |
|------------------------|---|---|---------|---------|
| t_{PLH} t_{PHL} | Propagation delay An to Bn or Bn to An | $C_L = 50pF; V_{CC} = 5V$ | 3.4 | ns |
| t_{PLH} t_{PHL} | Propagation delay An to PARITY | $C_L = 50pF; V_{CC} = 5V$ | 7.4 | ns |
| C_{IN} | Input capacitance | $V_I = 0V$ or V_{CC} | 4 | pF |
| $C_{I/O}$ | I/O capacitance | Outputs disabled; $V_O = 0V$ or V_{CC} | 7 | pF |
| I_{CCZ} | Total supply current | Outputs disabled; $V_{CC} = 5.5V$ | 50 | μA |

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|-----------------------------|-------------------|-----------------------|---------------|------------|
| 24-Pin Plastic DIP | -40°C to +85°C | 74ABT833 N | 74ABT833 N | SOT222-1 |
| 24-Pin plastic SO | -40°C to +85°C | 74ABT833 D | 74ABT833 D | SOT137-1 |
| 24-Pin Plastic SSOP Type II | -40°C to +85°C | 74ABT833 DB | 74ABT833 DB | SOT340-1 |
| 24-Pin Plastic TSSOP Type I | -40°C to +85°C | 74ABT833 PW | 74ABT833PW DH | SOT355-1 |

PIN CONFIGURATION



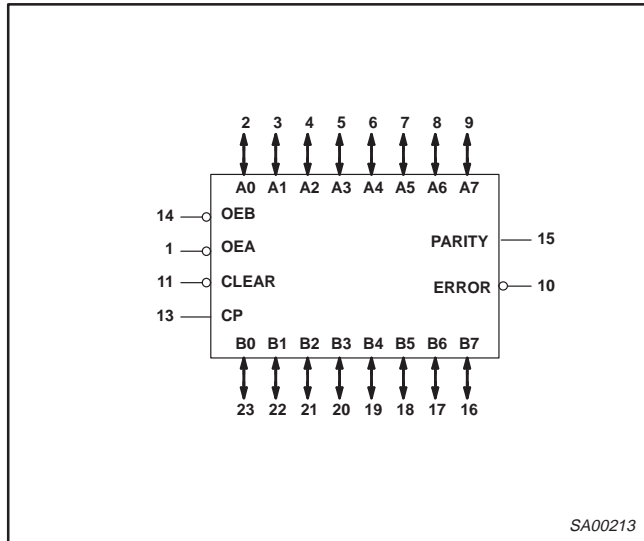
PIN DESCRIPTION

| SYMBOL | PIN NUMBER | NAME AND FUNCTION |
|--------------------|--------------------------------|---|
| A0 – A7 | 2, 3, 4, 5, 6, 7, 8, 9 | A port 3-State inputs/outputs |
| B0 – B7 | 23, 22, 21, 20, 19, 18, 17, 16 | B port 3-State inputs/outputs |
| $\overline{OE}A$ | 1 | Enables the A outputs when Low |
| $\overline{OE}B$ | 14 | Enables the B outputs when Low |
| PARITY | 15 | Parity output/input |
| ERROR | 10 | Error output (open collector) |
| \overline{CLEAR} | 11 | Clears the error flag register when Low |
| CP | 13 | Clock input |
| GND | 12 | Ground (0V) |
| V_{CC} | 24 | Positive supply voltage |

Octal transceiver with parity generator/checker (3-State)

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LOGIC SYMBOL



FUNCTION TABLE

| MODE | INPUTS | | | | OUTPUTS | | |
|---|-------------------------|-------------------------|-------------------------|----------------------------------|---------|---------|---------|
| | $\overline{\text{OEB}}$ | $\overline{\text{OEA}}$ | An Σ of Highs | Bn + Parity Σ of Highs | An | Bn | PARITY |
| A data to B bus and generate odd parity output | L | H | Odd Even | (output) | (input) | An | L H |
| B data to A bus and check for parity error ¹ | H | L | (output) | X | Bn | (input) | (input) |
| A bus and B bus disabled ² | H | H | X | X | Z | Z | Z |
| A data to B bus and generate inverted parity output | L | L | Odd Even | (output) | (input) | An | H L |

NOTES:

1. Error checking is detailed in the Error Flag Function Table below.
2. When clocked, the error output is Low if the sum of A inputs is even or High if the sum of A inputs is odd.

ERROR FLAG FUNCTION TABLE

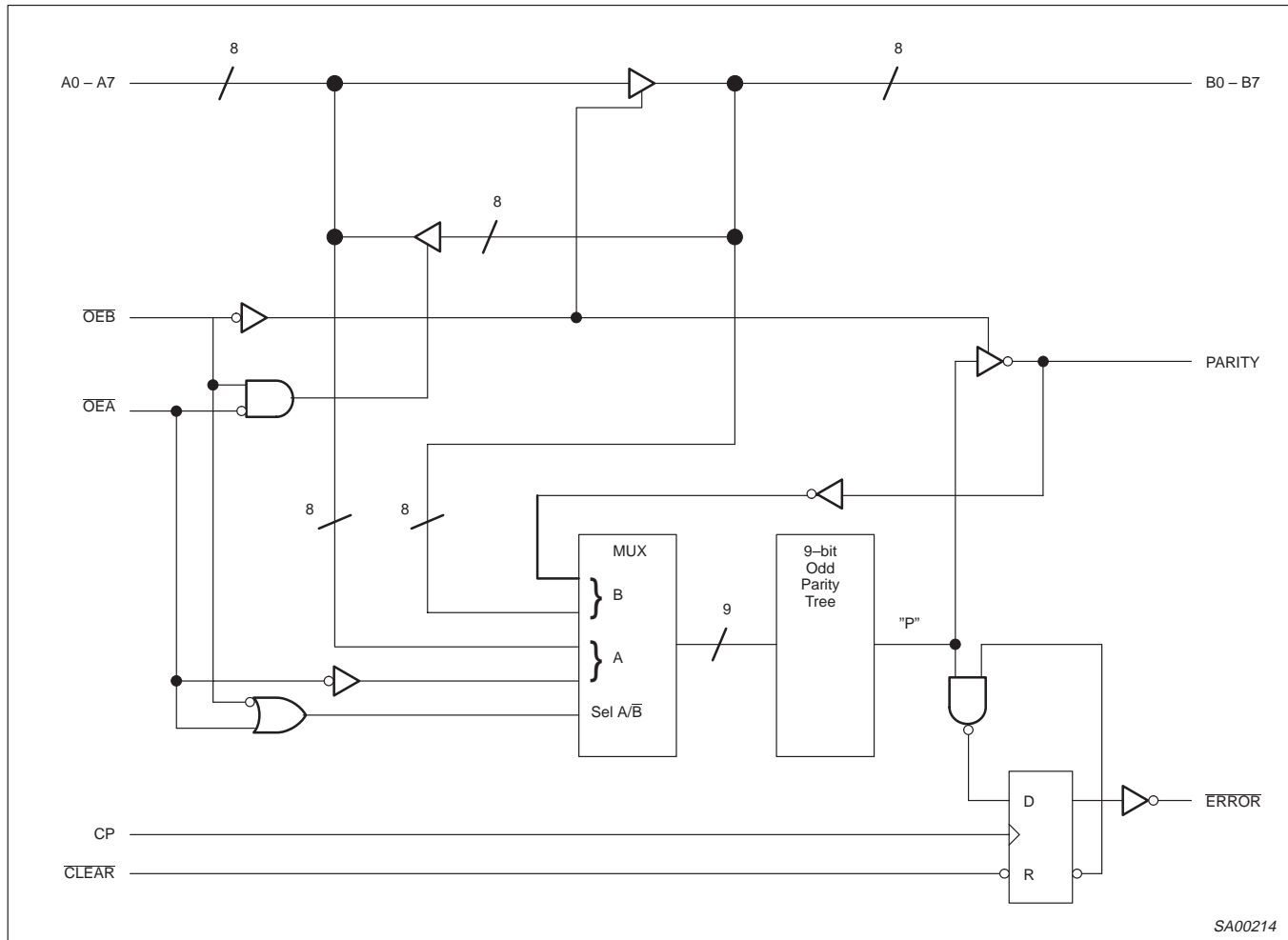
| MODE | INPUTS | | | Internal node Point "P" | Output Pre-state ERROR _{n-1} | ERROR OUTPUT |
|--------|--------|----|----------------------------------|----------------------------|---|-----------------|
| | CLEAR | CP | Bn + Parity Σ of Highs | | | |
| Sample | H | ↑ | Odd | H | H | H |
| | H | ↑ | Even | L | X | L |
| | H | X | X | X | L | L |
| Hold | H | ↑ | X | X | X | NC |
| Clear | L | X | X | X | X | H |

- H = High voltage level steady state
- L = Low voltage level steady state
- X = Don't care
- NC = No change
- Z = High impedance "off" state
- ↑ = Low-to-High clock transition
- ↑̄ = Not a Low-to-High clock transition

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LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|------------------|--------------------------------|-----------------------------|--------------|------|
| V _{CC} | DC supply voltage | | -0.5 to +7.0 | V |
| I _{IK} | DC input diode current | V _I < 0 | -18 | mA |
| V _I | DC input voltage ³ | | -1.2 to +7.0 | V |
| I _{OK} | DC output diode current | V _O < 0 | -50 | mA |
| V _{OUT} | DC output voltage ³ | output in Off or High state | -0.5 to +5.5 | V |
| I _{OUT} | DC output current | output in Low state | 128 | mA |
| T _{stg} | Storage temperature range | | -65 to 150 | °C |

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---------------------|--|--------|----------|------|
| | | Min | Max | |
| V_{CC} | DC supply voltage | 4.5 | 5.5 | V |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_{IH} | High-level input voltage | 2.0 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_{OH} | High-level output voltage, $\overline{\text{ERROR}}$ | | 5.5 | V |
| I_{OH} | High-level output current | | -32 | mA |
| I_{OL} | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 5 | ns/V |
| T_{amb} | Operating free-air temperature range | -40 | +85 | °C |

DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|--------------------|---|---|-------------------------------|------------|-----------|---|-----------|---------------|
| | | | $T_{amb} = +25^\circ\text{C}$ | | | $T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | |
| | | | Min | Typ | Max | Min | Max | |
| V_{IK} | Input clamp voltage | $V_{CC} = 4.5\text{V}; I_{IK} = -18\text{mA}$ | | -0.9 | -1.2 | | -1.2 | V |
| I_{OH} | High-level output current ERROR ONLY | $V_{CC} = 5.5\text{V}; V_{OH} = 5.5\text{V}; V_I = V_{IL}$ or V_{IH} | | | 20 | | 20 | μA |
| V_{OH} | High-level output voltage All outputs except $\overline{\text{ERROR}}$ | $V_{CC} = 4.5\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL}$ or V_{IH} | 2.5 | 3.5 | | 2.5 | | V |
| | | $V_{CC} = 5.0\text{V}; I_{OH} = -3\text{mA}; V_I = V_{IL}$ or V_{IH} | 3.0 | 4.0 | | 3.0 | | V |
| | | $V_{CC} = 4.5\text{V}; I_{OH} = -32\text{mA}; V_I = V_{IL}$ or V_{IH} | 2.0 | 2.6 | | 2.0 | | V |
| V_{OL} | Low-level output voltage | $V_{CC} = 4.5\text{V}; I_{OL} = 64\text{mA}; V_I = V_{IL}$ or V_{IH} | | 0.42 | 0.55 | | 0.55 | V |
| I_I | Input leakage current | Control pins $V_{CC} = 5.5\text{V}; V_I = \text{GND}$ or 5.5V | | ± 0.01 | ± 1.0 | | ± 1.0 | μA |
| | | Data pins $V_{CC} = 5.5\text{V}; V_I = \text{GND}$ or 5.5V | | ± 5 | ± 100 | | ± 100 | μA |
| I_{OFF} | Power-off leakage current | $V_{CC} = 0.0\text{V}; V_I$ or $V_O \leq 4.5\text{V}$ | | ± 5.0 | ± 100 | | ± 100 | V |
| I_{PUPD} | Power-up/down 3-State output current ³ | $V_{CC} = 2.0\text{V}$; or $V_O = 0.5\text{V}; V_I = \text{GND}$ or V_{CC} ; $V_{OE} = \text{Don't care}$ | | ± 5.0 | ± 50 | | ± 50 | V |
| $I_{IH} + I_{OZH}$ | 3-State output High current | $V_{CC} = 5.5\text{V}; V_O = 2.7\text{V}; V_I = V_{IL}$ or V_{IH} | | 5.0 | 50 | | 50 | μA |
| $I_{IL} + I_{OZL}$ | 3-State output Low current | $V_{CC} = 5.5\text{V}; V_O = 0.5\text{V}; V_I = V_{IL}$ or V_{IH} | | -5.0 | -50 | | -50 | μA |
| I_{CEX} | Output High leakage current | $V_{CC} = 5.5\text{V}; V_O = 5.5\text{V}; V_I = \text{GND}$ or V_{CC} | | 5.0 | 50 | | 50 | μA |
| I_O | Output current ¹ | $V_{CC} = 5.5\text{V}; V_O = 2.5\text{V}$ | -50 | -80 | -180 | -50 | -180 | mA |
| I_{CCH} | Quiescent supply current | $V_{CC} = 5.5\text{V}$; Outputs High, $V_I = \text{GND}$ or V_{CC} | | 50 | 250 | | 250 | μA |
| I_{CCL} | | $V_{CC} = 5.5\text{V}$; Outputs Low, $V_I = \text{GND}$ or V_{CC} | | 20 | 30 | | 30 | mA |
| I_{CCZ} | | $V_{CC} = 5.5\text{V}$; Outputs 3-State; $V_I = \text{GND}$ or V_{CC} | | 50 | 250 | | 250 | μA |
| ΔI_{CC} | Additional supply current per input pin ² | $V_{CC} = 5.5\text{V}$; one input at 3.4V, other inputs at V_{CC} or GND | | 0.3 | 1.5 | | 1.5 | mA |

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V_{CC} between 0V and 2.1, with a transition time of up to 10msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$, a transition of up to 100 μsec is permitted. The $\overline{\text{ERROR}}$ output pin 10 is not included in this spec due to the open collector design.

Octal transceiver with parity generator/checker (3-State)

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AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

| SYMBOL | PARAMETER | WAVEFORMS | LIMITS | | | | | UNIT |
|--------------------------------------|---|-----------|--|------------|------------|---|--------------|------|
| | | | $T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$ | | | $T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 10\%$ | | |
| | | | Min | Typ | Max | Min | Max | |
| t_{PLH} t_{PHL} | Propagation delay An to Bn or Bn to An | 2 | 1.2 1.0 | 3.4 2.6 | 4.8 4.0 | 1.2 1.0 | 5.3 4.5 | ns |
| t_{PLH} t_{PHL} | Propagation delay An to PARITY | 1 2 | 2.1 2.5 | 7.4 7.4 | 9.5 9.7 | 2.1 2.5 | 11.2 11.0 | ns |
| t_{PLH} t_{PHL} | Propagation delay OE \bar{A} to PARITY | 1 2 | 2.6 3.1 | 6.6 6.7 | 8.5 8.6 | 2.6 3.1 | 10.5 10.0 | ns |
| t_{PLH} | Propagation delay CLEAR to ERROR | 5 | 1.0 | 2.9 | 4.4 | 1.0 | 5.2 | ns |
| t_{PHL} | Propagation delay CP to ERROR | 1 | 2.5 | 4.2 | 5.7 | 2.5 | 6.2 | ns |
| t_{pZH} t_{pZL} | Output enable time OE \bar{A} to An or OE \bar{B} to Bn, PARITY | 3 4 | 1.0 2.1 | 3.2 4.1 | 5.1 5.8 | 1.0 2.1 | 6.2 6.7 | ns |
| t_{pHZ} t_{pLZ} | Output disable time OE \bar{A} to An or OE \bar{B} to Bn, PARITY | 3 4 | 3.1 3.2 | 5.1 5.6 | 7.3 7.7 | 3.1 3.2 | 7.9 8.1 | ns |

AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

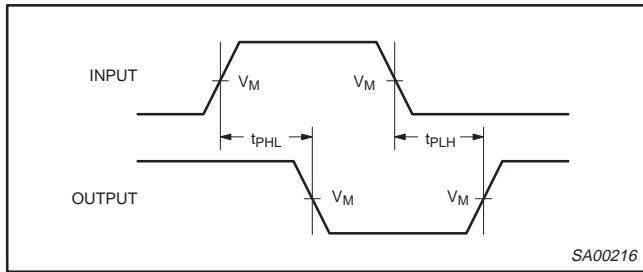
| SYMBOL | PARAMETER | WAVEFORMS | LIMITS | | | UNIT |
|------------------------------------|---|-----------|--|--------------|---|------|
| | | | $T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$ | | $T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 10\%$ | |
| | | | Min | Typ | Min | |
| $t_s(\text{H})$ $t_s(\text{L})$ | Setup time, High or Low Bn or PARITY to CP | 6 | 9.8 8.1 | 6.9 4.0 | 9.8 8.1 | ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, High or Low Bn or PARITY to CP | 6 | 0.0 0.0 | -3.7 -6.7 | 0.0 0.0 | ns |
| $t_w(\text{H})$ $t_w(\text{L})$ | Pulse width, High or Low CP | 6 | 3.0 3.0 | 1.5 1.0 | 3.0 3.0 | ns |
| $t_w(\text{L})$ | Pulse width, Low CLEAR | 5 | 3.0 | 1.0 | 3.0 | ns |
| t_{rec} | Recovery time CLEAR to CP | 5 | 2.0 | -0.3 | 2.0 | ns |

Octal transceiver with parity generator/checker (3-State)

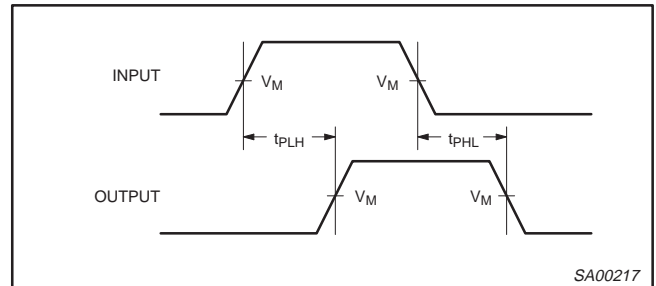
74ABT833

AC WAVEFORMS

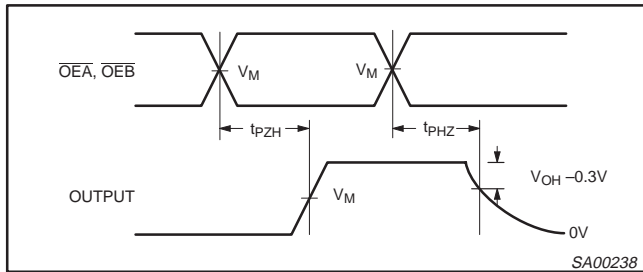
$V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$



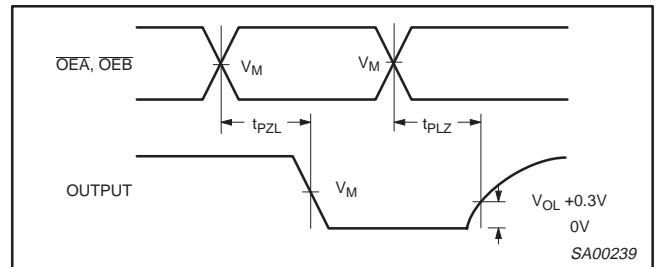
Waveform 1. Propagation Delay For Inverting Output



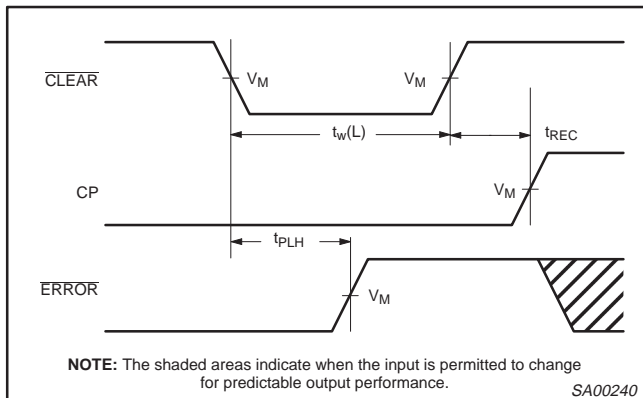
Waveform 2. Propagation Delay For Non-Inverting Output



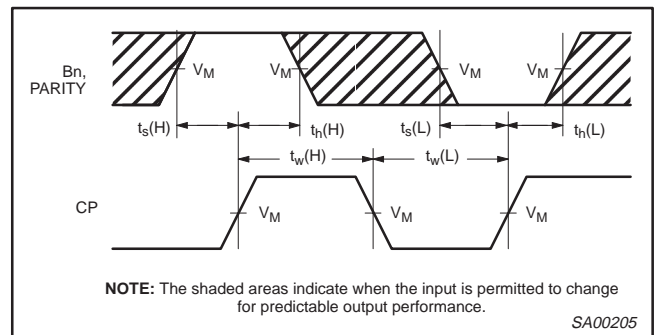
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 5. CLEAR Pulse Width, CLEAR to ERROR Delay and CLEAR to Clock Recovery Time



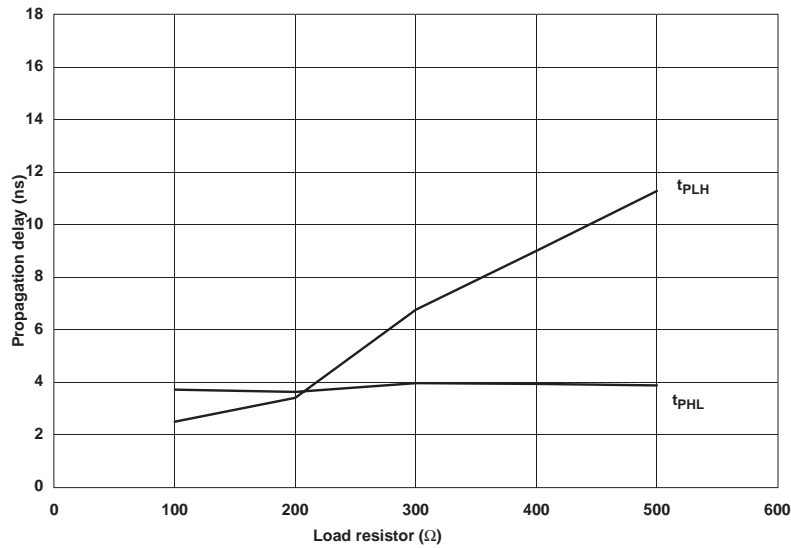
Waveform 6. Data Setup and Hold Times and Clock Pulse Width

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Octal transceiver with parity generator/checker (3-State)

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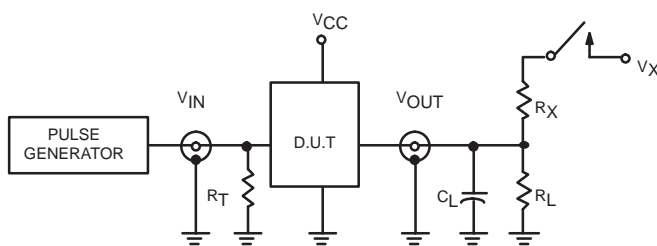
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



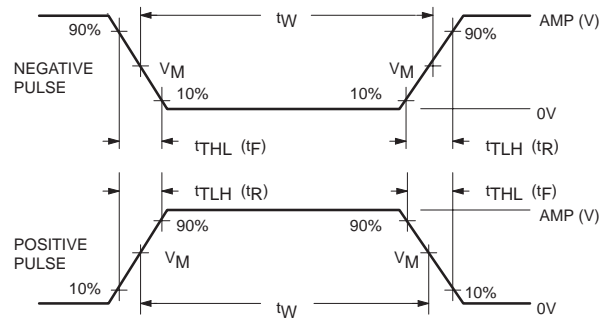
NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} over 300% with only a slight change in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

SA00241

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition
V_M = 1.5V

SWITCH POSITION

| TEST | SWITCH |
|------------------|--------|
| t _{PLZ} | closed |
| t _{pZL} | closed |
| All other | open |

LOAD VALUES

| OUTPUT | R _X | V _X |
|-----------|----------------|-----------------|
| ERROR | 100Ω | V _{CC} |
| All other | 500Ω | 7.0V |

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|--------|--------------------------|-----------|----------------|----------------|----------------|
| | Amplitude | Rep. Rate | t _W | t _R | t _F |
| 74ABT | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

SA00242

**Octal transceiver with parity generator/checker
(3-State)**

74ABT833**DIP24: plastic dual in-line package; 24 leads (300 mil)****SOT222-1****SO24: plastic small outline package; 24 leads; body width 7.5 mm****SOT137-1****SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm****SOT340-1****TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm****SOT355-1**

Octal transceiver with parity generator/checker
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NOTES

Octal transceiver with parity generator/checker (3-State)

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| <i>Preliminary Specification</i> | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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