

# SN54AC533, SN74AC533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS555A – NOVEMBER 1995 – REVISED MAY 1996

- **3-State Inverting Outputs Drive Bus Lines Directly**
- **Full Parallel Access for Loading**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs**

## description

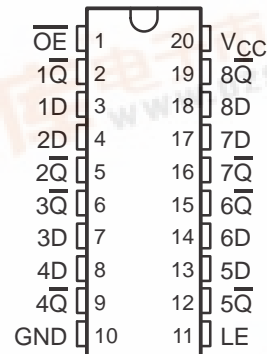
The 'AC533 are octal transparent D-type latches with 3-state outputs. When the latch-enable (LE) input is high, the  $\bar{Q}$  outputs follow the complements of the data (D) inputs. When LE is taken low, the  $\bar{Q}$  outputs are latched at the inverse logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

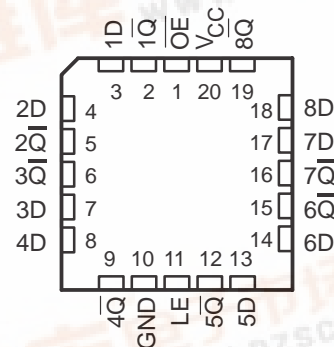
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AC533 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AC533 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54AC533 . . . J OR W PACKAGE  
SN74AC533 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54AC533 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

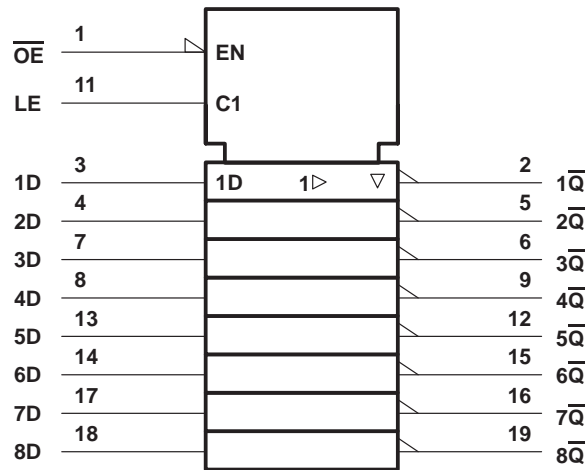
TEXAS  
INSTRUMENTS

Copyright © 1996, Texas Instruments Incorporated

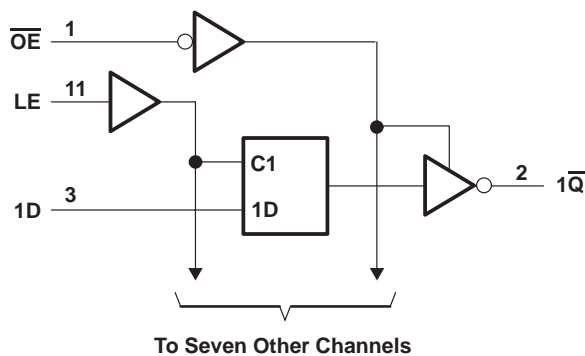
# SN54AC533, SN74AC533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS555A – NOVEMBER 1995 – REVISED MAY 1996

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
N package	1.3 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

# SN54AC533, SN74AC533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS555A – NOVEMBER 1995 – REVISED MAY 1996

## recommended operating conditions (see Note 3)

			SN54AC533		SN74AC533		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		2	6	2	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1		2.1		V
		$V_{CC} = 4.5\text{ V}$	3.15		3.15		
		$V_{CC} = 5.5\text{ V}$	3.85		3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$		0.9		0.9	V
		$V_{CC} = 4.5\text{ V}$		1.35		1.35	
		$V_{CC} = 5.5\text{ V}$		1.65		1.65	
$V_I$	Input voltage		0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$		–12		–12	mA
		$V_{CC} = 4.5\text{ V}$		–24		–24	
		$V_{CC} = 5.5\text{ V}$		–24		–24	
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$		12		12	mA
		$V_{CC} = 4.5\text{ V}$		24		24	
		$V_{CC} = 5.5\text{ V}$		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	8	0	8	ns/V
$T_A$	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54AC533		SN74AC533		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	$I_{OH} = -12\text{ mA}$	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
$V_{OL}$	$I_{OL} = 50\text{ }\mu\text{A}$	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 12\text{ mA}$	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.25$		$\pm 5$		$\pm 2.5$	$\mu\text{A}$
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V		4.5						pF

# SN54AC533, SN74AC533

## OCTAL TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

SCAS555A – NOVEMBER 1995 – REVISED MAY 1996

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		SN54AC533		SN74AC533		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration, LE high	6		8		6.5		ns
$t_{su}$	Setup time, data before LE $\downarrow$	5.5		7.5		6		ns
$t_h$	Hold time, data after LE $\downarrow$	1.5		2.5		1		ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		SN54AC533		SN74AC533		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration, LE high	4.5		6.5		5		ns
$t_{su}$	Setup time, data before LE $\downarrow$	4		6		4.5		ns
$t_h$	Hold time, data after LE $\downarrow$	1.5		2.5		1		ns

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$		SN54AC533		SN74AC533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	$\overline{Q}$	2	14	1	17.5	1.5	16	ns
$t_{PHL}$			2	13	1	16	1.5	14.5	
$t_{PLH}$	LE	$\overline{Q}$	2	14.5	1	18	1.5	16.5	ns
$t_{PHL}$			2	13	1	16	1.5	14.5	
$t_{PZH}$	$\overline{OE}$	$\overline{Q}$	2	12.5	1	15.5	1.5	14	ns
$t_{PZL}$			2	12.5	1	15.5	1.5	14	
$t_{PHZ}$	$\overline{OE}$	$\overline{Q}$	2	13	1	16	1.5	14.5	ns
$t_{PLZ}$			2	13	1	16	1.5	14.5	

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$		SN54AC533		SN74AC533		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	$\overline{Q}$	2	10	1	12.5	1.5	11	ns
$t_{PHL}$			2	9.5	1	12	1.5	10.5	
$t_{PLH}$	LE	$\overline{Q}$	2	10.5	1	13	1.5	11.5	ns
$t_{PHL}$			2	10	1	13	1.5	11	
$t_{PZH}$	$\overline{OE}$	$\overline{Q}$	2	9.5	1	12	1.5	10.5	ns
$t_{PZL}$			2	9.5	1	12	1.5	10.5	
$t_{PHZ}$	$\overline{OE}$	$\overline{Q}$	2	10	1	12.5	1.5	11	ns
$t_{PLZ}$			2	10	1	12.5	1.5	11	

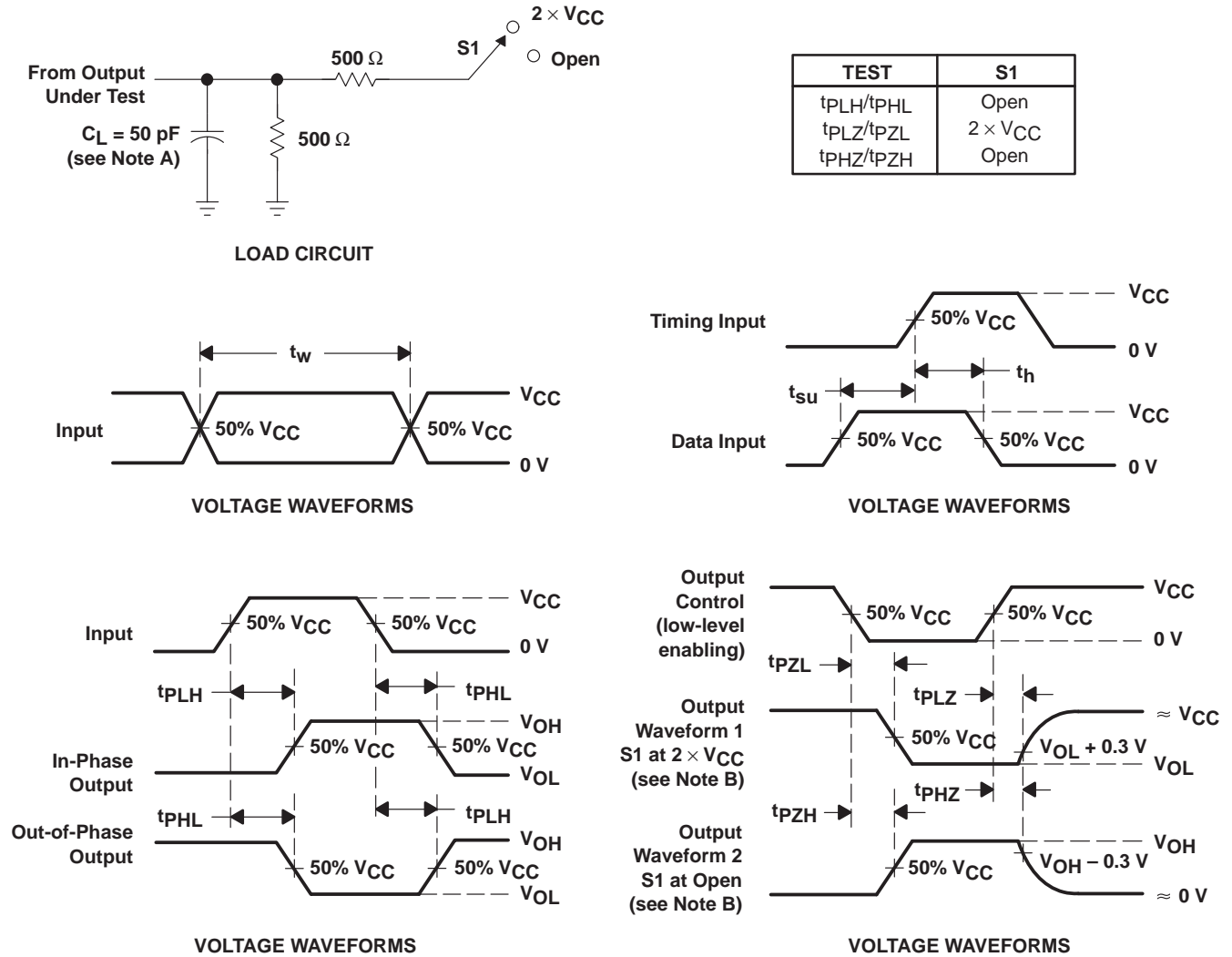
**operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	40	pF

# SN54AC533, SN74AC533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS555A – NOVEMBER 1995 – REVISED MAY 1996

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.