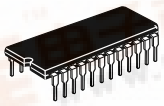
MC14534B

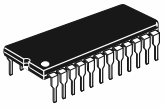
5 Cascaded BCD Counters

The MC14534B is composed of five BCD ripple counters that have their respective outputs multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four (BCD) pins. Selection is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three–state controls providing an “open–circuit” when these controls are high and allowing multiplexing. Cascading may be accomplished by using the carry–out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534B was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

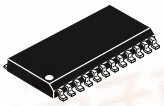
- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 623



P SUFFIX
PLASTIC
CASE 709



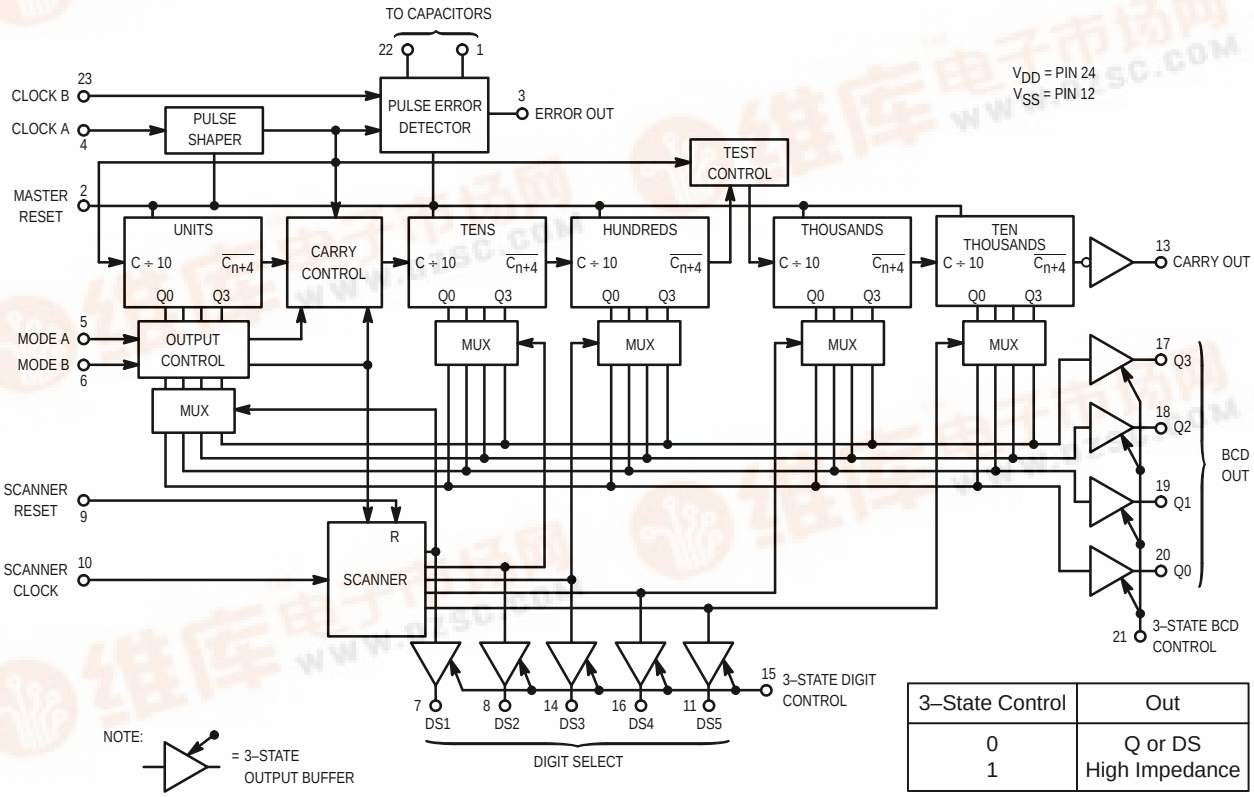
DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

T_A = – 55° to 125°C for all packages.

BLOCK DIAGRAM



3–State Control	Out
0	Q or DS
1	High Impedance

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.0	—	1.5	1.0	—	1.0	
(V_O = 9.0 or 1.0 Vdc)		10	—	2.0	—	3.0	2.0	—	2.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	3.0	—	4.5	3.0	—	3.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	4.0	—	4.0	3.5	—	4.0	—	
(V_O = 1.0 or 9.0 Vdc)		10	8.0	—	8.0	7.0	—	8.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	12	—	12	11	—	12	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Output Drive Current — Pins 1 and 22	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)		5.0	– 0.31		– 0.25	– 0.8		– 0.17		
(V_{OH} = 9.5 Vdc) Source		10	– 0.31	—	– 0.25	– 0.4	—	– 0.17	—	
(V_{OH} = 13.5 Vdc)		15	– 0.9	—	– 0.75	– 1.6	—	– 0.51	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.024	—	0.02	0.03	—	0.014	—	mAdc
(V_{OL} = 0.5 Vdc)		10	0.06	—	0.05	0.09	—	0.035	—	
(V_{OL} = 1.5 Vdc)		15	1.3	—	0.25	1.63	—	0.175	—	
Input Current	I_{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance. (continued)

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}) (continued)

Characteristic	Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.010 0.020 0.030	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.5 μA/kHz) f + I_{DD} I_T = (1.0 μA/kHz) f + I_{DD} I_T = (1.5 μA/kHz) f + I_{DD}		Scan Oscillator Frequency = 1.0 kHz					μAdc
Three–State Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	μAdc

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

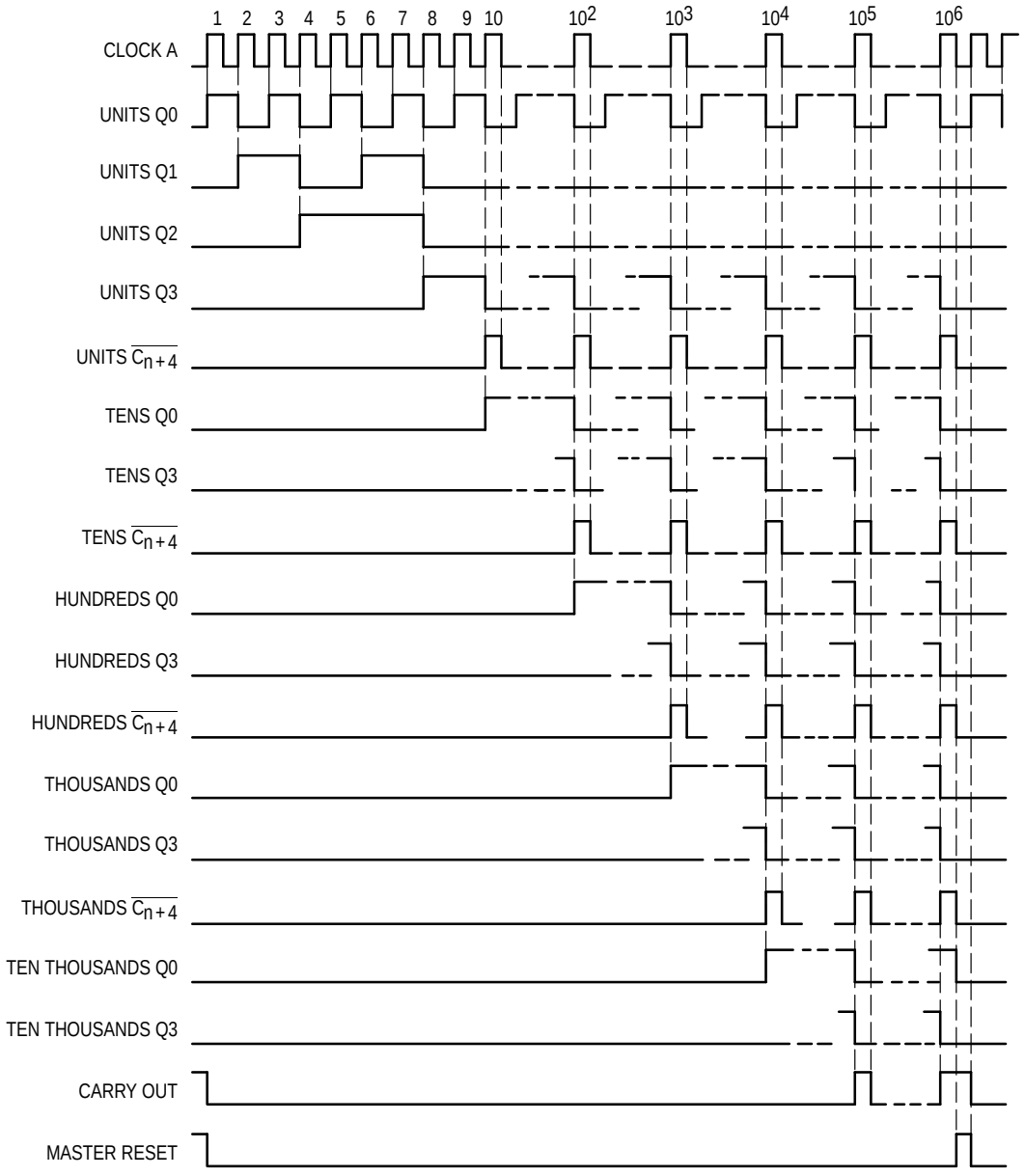
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C, see Figure 1)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time, Clock to Q t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 4.0 µs t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 1.5 µs t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 1.0 µs	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 4.0 1.5 1.0	 8.0 3.0 2.25	µs
Clock to Carry Out t_{PLH} = (1.8 ns/pF) C_L + 3.3 µs t_{PLH} = (0.8 ns/pF) C_L + 1.1 µs t_{PLH} = (0.6 ns/pF) C_L + 0.8 µs	t_{PLH}	 5.0 10 15	 — — —	 3.3 1.1 0.8	 6.6 2.2 1.7	µs
Master Reset to Q t_{PHL} = (1.8 ns/pF) C_L + 1.8 µs t_{PHL} = (0.8 ns/pF) C_L + 0.6 µs t_{PHL} = (0.6 ns/pF) C_L + 0.5 µs	t_{PHL}	 5.0 10 15	 — — —	 1.8 0.6 0.5	 3.6 1.2 0.9	µs
Master Reset to Error Out t_{PHL} = (1.8 ns/pF) C_L + 0.57 µs t_{PHL} = (0.8 ns/pF) C_L + 0.19 µs t_{PHL} = (0.6 ns/pF) C_L + 0.11 µs	t_{PHL}	 5.0 10 15	 — — —	 0.6 0.2 0.12	 1.5 .5 0.38	µs
Scanner Clock to Q t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 1.8 µs t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 0.6 µs t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 0.5 µs	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 1.8 0.6 0.5	 3.6 1.2 0.9	µs
Scanner Clock to Digit Select t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 1.5 µs t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 0.5 µs t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 0.4 µs	t_{PLH}, t_{PLH}	 5.0 10 15	 — — —	 1.5 0.5 0.4	 3.0 1.0 0.75	µs
Propagation Delay Time 3–State Control to Q	t_{PHZ}	5.0 10 15	— — —	75 45 40	150 90 80	ns
	t_{PZH}	5.0 10 15	— — —	120 55 40	240 110 80	ns
	t_{PLZ}	5.0 10 15	— — —	120 55 45	240 110 90	ns
	t_{PZL}	5.0 10 15	— — —	160 70 45	320 140 90	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	1.0 3.0 5.0	0.5 1.0 1.2	MHz
Clock or Scanner Clock Pulse Width	t_{WH}	5.0 10 15	1000 500 375	500 190 125	— — —	ns
Scanner Reset Pulse Width	t_w	5.0 10 15	320 130 80	160 65 40	— — —	ns
Scanner Reset Removal Time	t_{rem}	5.0 10 15	900 150 100	270 80 50	— — —	ns
Master Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	2000 600 450	900 300 250	— — —	ns
Master Reset Removal Time	t_{rem}	5.0 10 15	1060 350 250	550 205 140	— — —	ns

* The formulas given are for the typical characteristics only at 25°C.

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

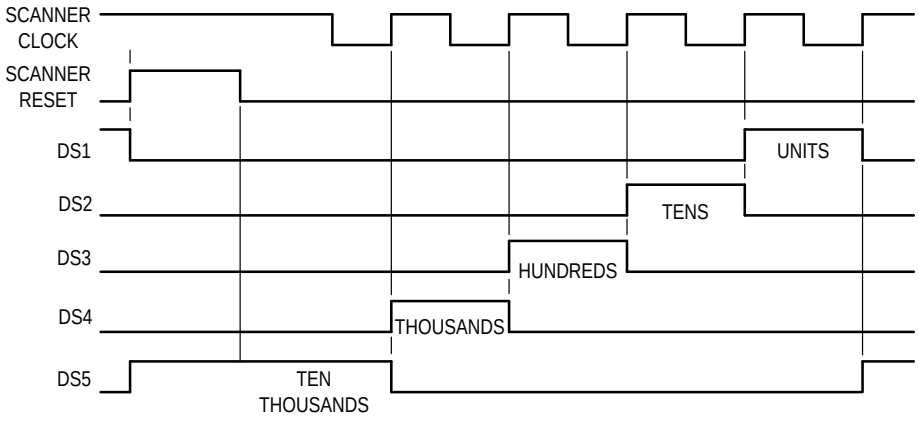
COUNTER TIMING DIAGRAM



MODE CONTROL TRUTH TABLE

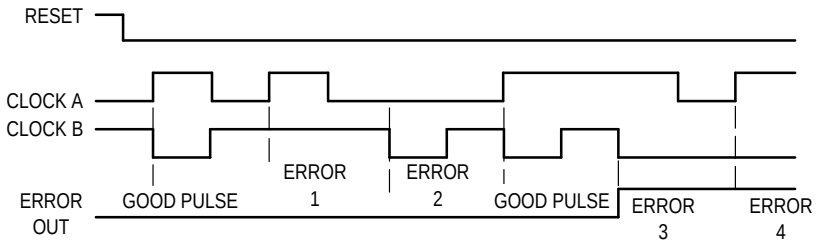
Mode A	Mode B	First Stage Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first stage	5–digit Counter
0	1	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2, and 4.
1	1	Inhibited	At 4 to 5 transition of first stage	4–digit counter with ÷ 10 and roundoff at front end.
1	0	Counts 3, 4, 5, 6, 7 = 5 Counts 8, 9, 0, 1, 2 = 0	At 7 to 8 transition of first stage	4–digit counter with 1/2 pence capability.

SCANNER TIMING DIAGRAM



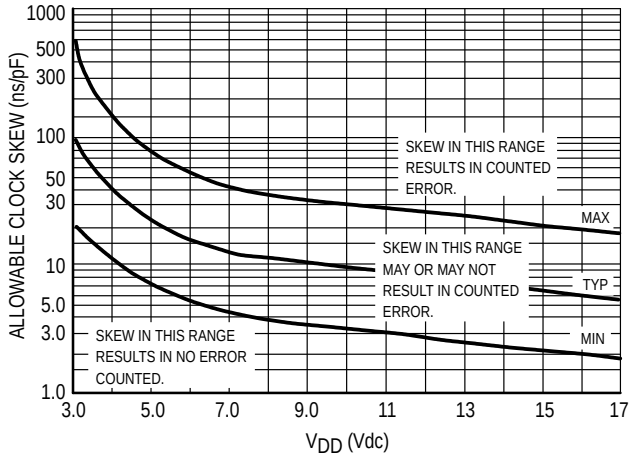
NOTE: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages.
DS5 is selected automatically when Scanner Reset goes high.

ERROR DETECTION TIMING DIAGRAM



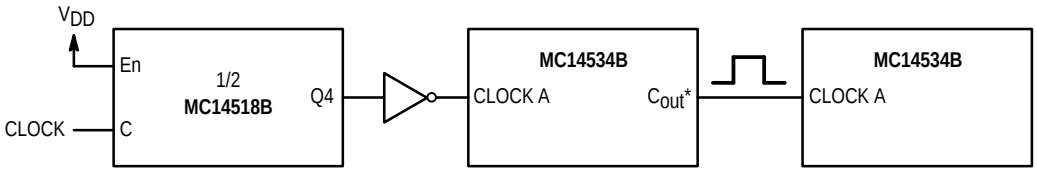
NOTE: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice–versa) within a time period of the one–shots an error is counted. Three errors result in Error Out to go to a “1”. If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

CLOCK SKEW RANGE



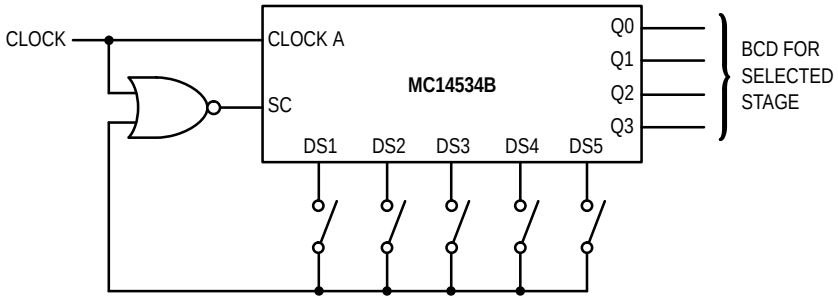
NOTES:
1. The skew is the time difference between the low–to–high transition of C_A to the high–to–low transition of C_B or vice–versa. Capacitors C1 = C22 tied from pins 1 and 22 to V_{SS}.
2. This graph is accurate for C1 = C22 ≥ 100 pF.
3. When the error detection circuitry in not used, pins 1 and 22 are left open.

APPLICATIONS INFORMATION



* Carry Out is high for a single clock period when all five BCD stages go to zero. (Carry Out also goes high when MR is applied.)

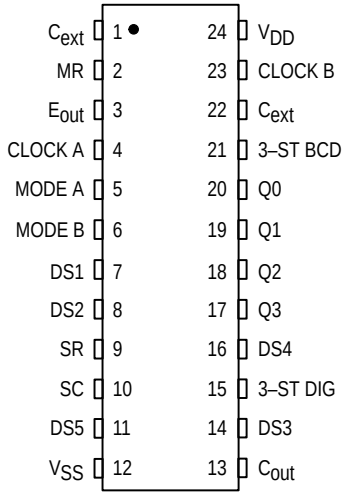
Figure 1. Cascade Operation



When the Q outputs of a given stage are required, this configuration will lock up the selected stage within four clock cycles. The select line feedback may be hardwired or switched.

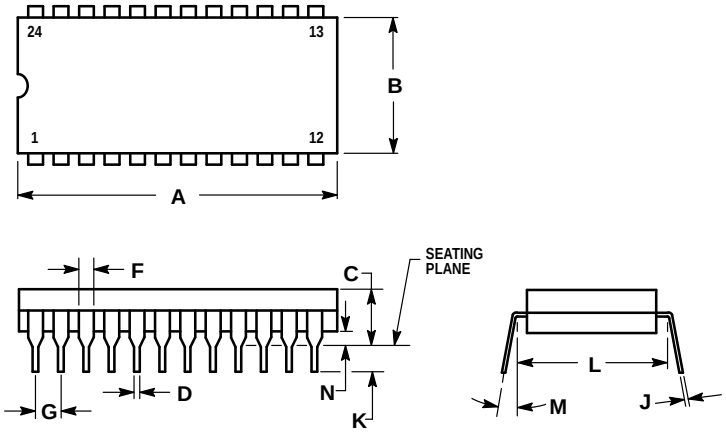
Figure 2. Forcing a BCD Stage to the Q Outputs

PIN ASSIGNMENT



OUTLINE DIMENSIONS

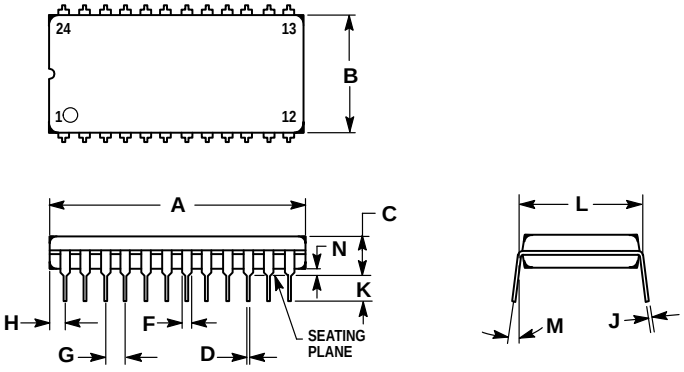
L SUFFIX
CERAMIC DIP PACKAGE
CASE 623–05
ISSUE M



NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.27	0.020	0.050

P SUFFIX
PLASTIC DIP PACKAGE
CASE 709–02
ISSUE C

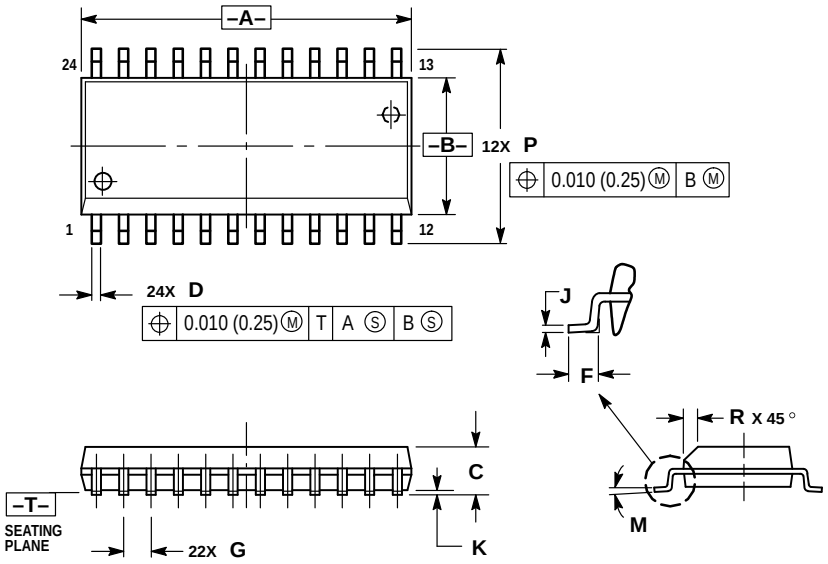


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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