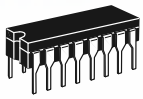
Universal Hexadecimal Counter

MC10136

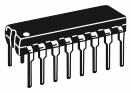
The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. Carry Out goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.



L SUFFIX
CERAMIC PACKAGE
CASE 620–10

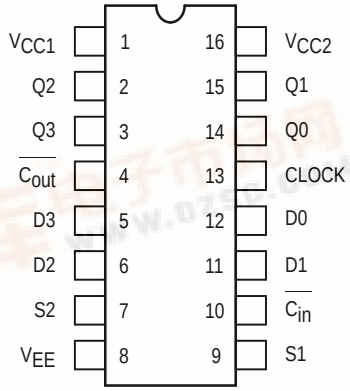


P SUFFIX
PLASTIC PACKAGE
CASE 648–08

FN SUFFIX
PLCC
CASE 775–02

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ
t_{pd} = 3.3 ns typ (C-Q)
7.0 ns typ ($\overline{C}$-C_{out})
5.0 ns typ (C_{in}-C_{out})

DIP PIN ASSIGNMENT

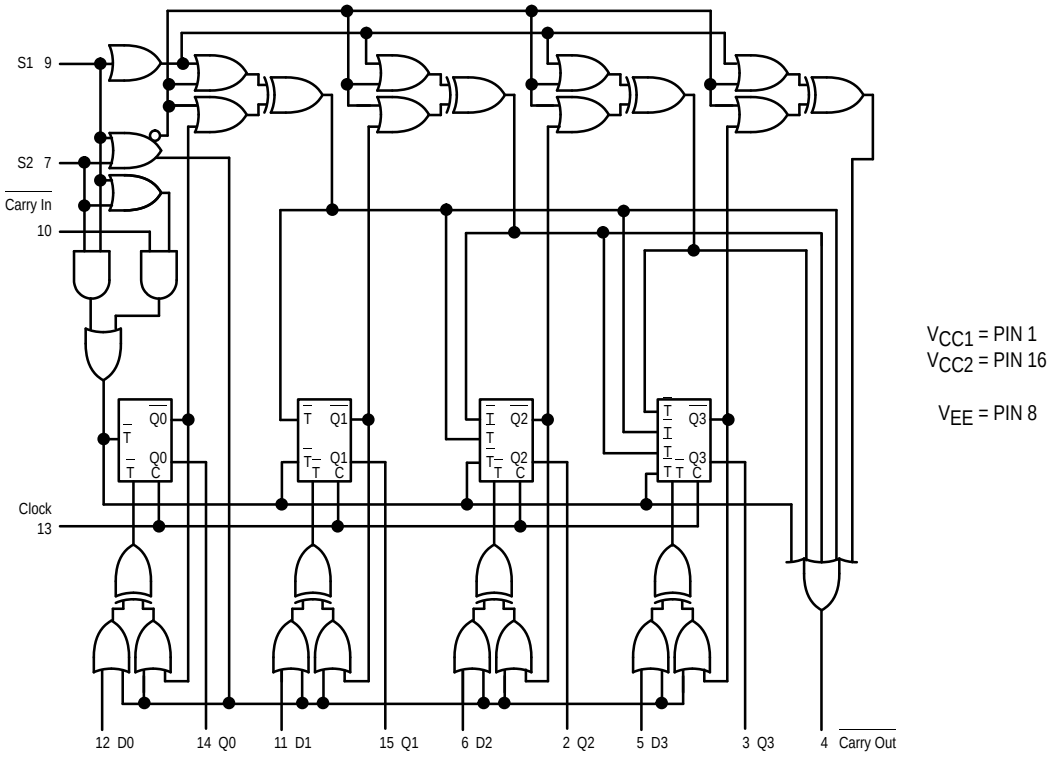


Pin assignment is for Dual–in–Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).

FUNCTION TABLE

C_{in}	S1	S2	Operating Mode
X	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
X	H	H	Hold (Stop Count)

LOGIC DIAGRAM



NOTE: Flip-flops will toggle when all $\overline{T}$ inputs are low.

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	X	H	L	L	H	H	L
L	H	X	X	X	X	L	H	H	L	H	H	H
L	H	X	X	X	X	L	H	L	H	H	H	H
L	H	X	X	X	X	L	H	H	H	H	H	L
L	H	X	X	X	X	H	L	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H
H	H	X	X	X	X	X	H	H	H	H	H	H
L	L	H	H	L	L	X	H	H	H	L	L	L
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L
H	L	X	X	X	X	L	H	H	H	H	H	H

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		138		100	125		138	mAdc
Input Current	I_{inH}	5,6,11,12 7 9,10 13		350 425 390 460			220 265 245 290		220 265 245 290	µAdc
	I_{inL}	All	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	14 (2.)	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	14 (2.)	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	14 (2.)	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	14 (2.)		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Clock Input	t_{13+14+} t_{13+14-} t_{13+4+} t_{13+4-}	14 14 4 4	0.8 0.8 2.0 2.0	4.8 4.8 10.9 10.9	1.0 1.0 2.5 2.5	3.3 3.3 7.0 7.0	4.5 4.5 10.5 10.5	1.4 1.4 2.4 2.4	5.0 5.0 11.5 11.5	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{10-4-} t_{10+4+}	4 (3.) 4	1.6 1.6	7.4 7.4	1.6 1.6	5.0 5.0	6.9 6.9	1.9 1.9	7.5 7.5	
Setup Time Data Inputs	t_{12+13+} t_{12-13+}	14 14	3.5 3.5		3.5 3.5			3.5 3.5		
Select Inputs	t_{9+13+} t_{7+13+}	14 14	6.0 6.0		6.0 6.0			6.0 6.0		
$\overline{\text{Carry In}}$ Input	t_{10-13+} t_{10+13+}	14 14	2.5 1.5		2.5 1.5			3.0 1.5		
Hold Time Data Inputs	t_{13+12+} t_{13+12-}	14 14	0 0		0 0			0 0		
Select Inputs	t_{13+9+} t_{13+7+}	14 14	–1.0 –1.0		–1.0 –1.0			–1.0 –1.0		
$\overline{\text{Carry In}}$ Input	t_{13+10-} t_{13+10+}	14 14	0 0		0 0			0 0		
Counting Frequency	$f_{countup}$ $f_{countdown}$	14 14	125 125		125 125	150 150		125 125		MHz
Rise Time (20 to 80%)	t_{4+} t_{14+}	4 14	0.9 0.9	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.5 3.5	ns
Fall Time (20 to 80%)	t_{4-} t_{14-}	4 14	0.9 0.9	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.5 3.5	

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Measure output after clock pulse V_{IL} ⟋ V_{IH} appears at clock input (Pin 13).
3. Before test set all Q outputs to a logic high.
4. To preserve reliable performance, the MC10136 (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500lfpm blown air or equivalent heat sinking is provided.

ELECTRICAL CHARACTERISTICS (continued)

				TEST VOLTAGE VALUES (Volts)					
			@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
			–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
			+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
			+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	5,6,11,12 7 9,10 13	5,6,11,12 7 9,10 13				8 8 8 8	1, 16 1, 16 1, 16 1, 16
		I_{inL}	All		Note 1.			8	1, 16
Output Voltage	Logic 1	V_{OH}	14 (2.)	12	7, 9			8	1, 16
Output Voltage	Logic 0	V_{OL}	14 (2.)		7, 9			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	14 (2.)		7, 9	12		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	14 (2.)		7, 9		12	8	1, 16
Switching Times	(50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Clock Input	t_{13+14+}	14	12		13	14	8	1, 16
		t_{13+14-}	14			13	14	8	1, 16
		t_{13+4+}	4	7		13	4	8	1, 16
		t_{13+4-}	4	7		13	4	8	1, 16
	$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{10-4-}	4 (3.)	7	13	10	4	8	1, 16
		t_{10+4+}	4	7	13	10	4	8	1, 16
Setup Time	Data Inputs	t_{12+13+}	14		7, 9	12, 13	14	8	1, 16
		t_{12-13+}	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t_{9+13+}	14			9, 13	14	8	1, 16
		t_{7+13+}	14			7, 13	14	8	1, 16
	$\overline{\text{Carry In}}$ Inputs	t_{10-13+}	14	7	9	10, 13	14	8	1, 16
		t_{10+13+}	14	7	9	10, 13	14	8	1, 16
Hold Time	Data Inputs	t_{13+12+}	14		7, 9	12, 13	14	8	1, 16
		t_{13+12-}	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t_{13+9+}	14			9, 13	14	8	1, 16
		t_{13+7+}	14			7, 13	14	8	1, 16
	$\overline{\text{Carry In}}$ Inputs	t_{13+10-}	14	7	9	10, 13	14	8	1, 16
		t_{13+10+}	14	7		10, 13	14	8	1, 16
Counting Frequency		$f_{countup}$	14	7		13	14	8	1, 16
		$f_{countdown}$	14	9		13	14	8	1, 16
Rise Time	(20 to 80%)	t_{4+}	4	7		13	4	8	1, 16
		t_{14+}	14	7		13	14	8	1, 16
Fall Time	(20 to 80%)	t_{4-}	4	7		13	4	8	1, 16
		t_{14-}	14	7		13	14	8	1, 16

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Measure output after clock pulse V_{IL} ⟋ V_{IH} appears at clock input (Pin 13).
3. Before test set all Q outputs to a logic high.
4. To preserve reliable performance, the MC10136 (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500lfpm blown air or equivalent heat sinking is provided.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

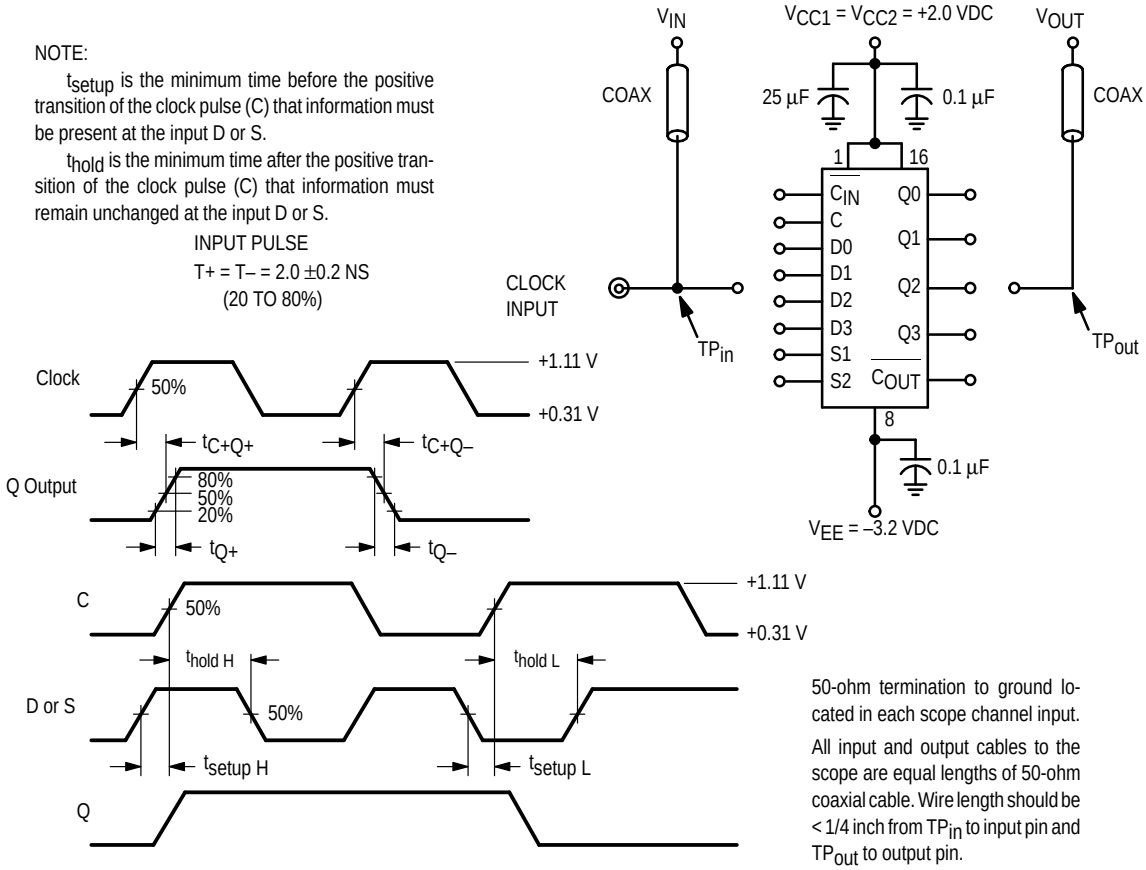
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

INPUT PULSE
T+ = T– = 2.0 ±0.2 NS
(20 TO 80%)

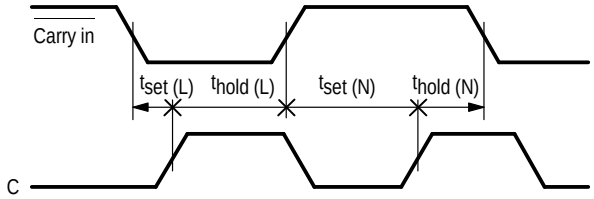


50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

$\overline{\text{CARRY IN}}$ SET UP AND HOLD TIMES



APPLICATIONS INFORMATION

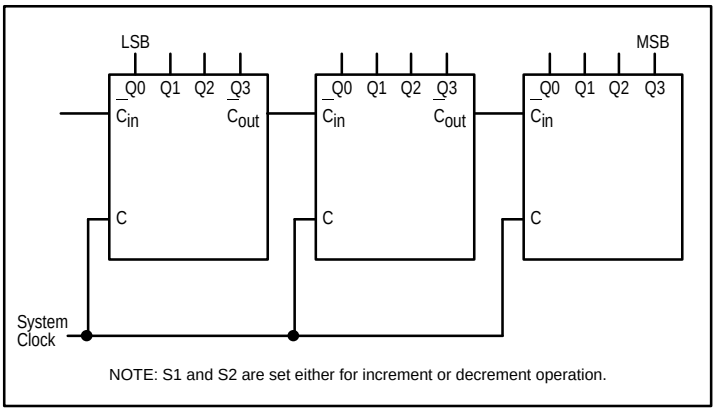
To provide more than four bits of counting capability several MC10136 counters may be cascaded. The Carry In input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The Carry In of the first device may be left open. The system clock is common to all devices.

The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL III devices, prescalers with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10136 and MC1670. Use of the MC10231 in place of the MC1670 permits 200 MHz operation.

The MC10136 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one (M = N + 1), therefore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input (M = N). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as $^1/_2$MC10109 and a flip-flop such as $^1/_2$MC10131.

FIGURE 1 — 12 BIT SYNCHRONOUS COUNTER



NOTE: S1 and S2 are set either for increment or decrement operation.

FIGURE 2 — 300 MHz PRESCALER

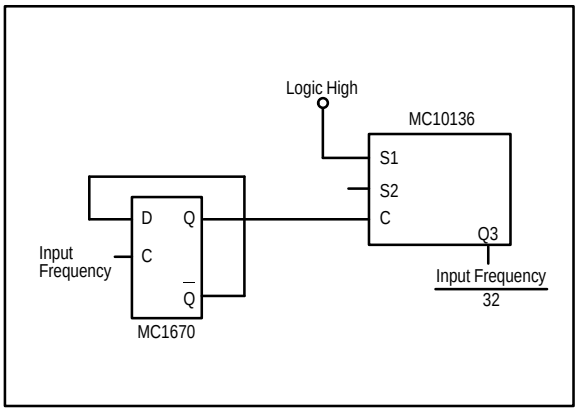
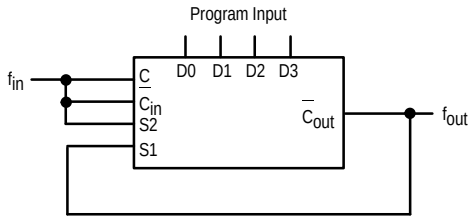


FIGURE 3 — 50 MHz PROGRAMMABLE COUNTER

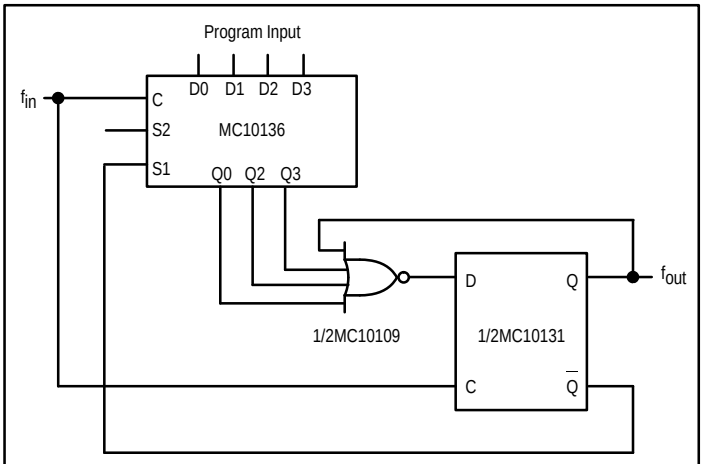


1 $f_{out} = \frac{f_{in}}{\text{Program Input} + 1}$

2 $f_{max} \cong$ 50 MHz Typ.

3 Divide Ratio is from 1 to 16.

FIGURE 4 — 100 MHz PROGRAMMABLE COUNTER



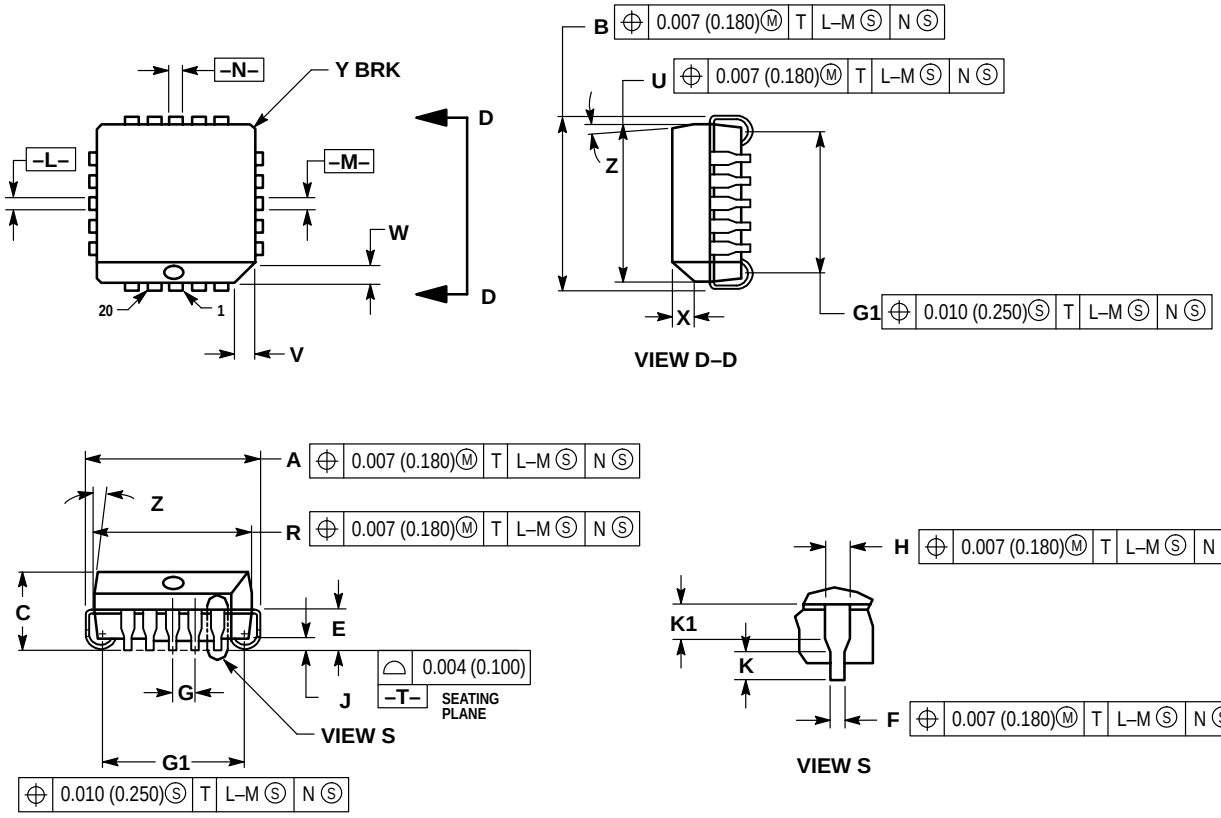
1 $f_{out} = \frac{f_{in}}{\text{Program Input}}$

2 $f_{max} \cong$ 110 MHz Typ.

3 Divide Ratio is from 2 to 15.

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C

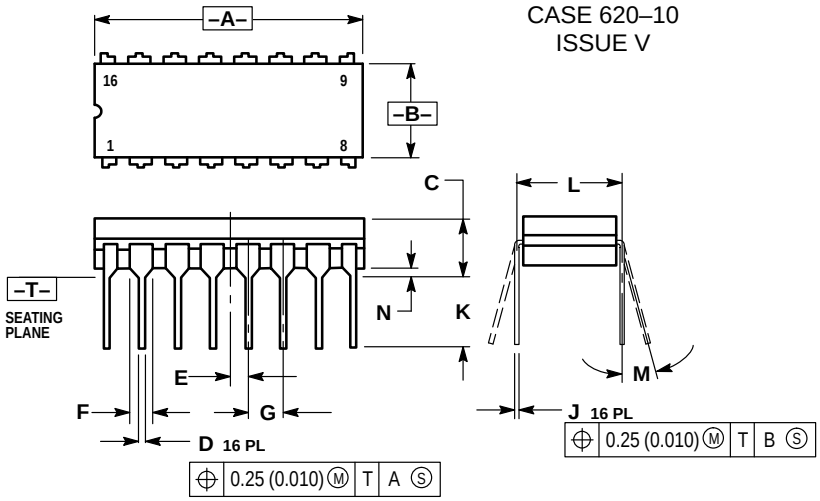


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

OUTLINE DIMENSIONS

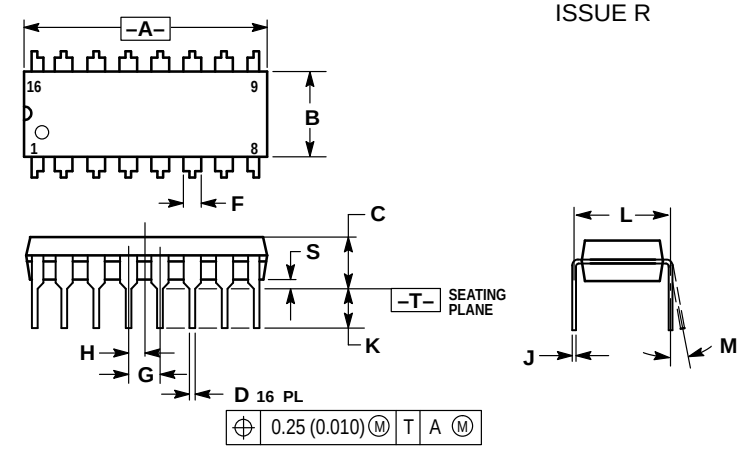
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298