3971

DUAL DMOS
FULL-BRIDGE DRIVER

Designed to interface between external PWM control logic and inductive loads such as relays, solenoids, dc motors, or stepper motors, each full bridge can operate with output currents to ±2.5 A and operating voltages to 50 V.

Low $r_{DS(on)}$ DMOS output drivers provide low power dissipation during PWM operation. Internal charge pump circuitry is used to create a boosted voltage to fully enhance the high-side DMOS switches.

Three TTL-compatible logic-input terminals per bridge allow flexibility in configuring PWM control.

Internal circuit protection includes thermal shutdown with hysteresis, and crossover-current protection. Special power -up sequencing is not required.
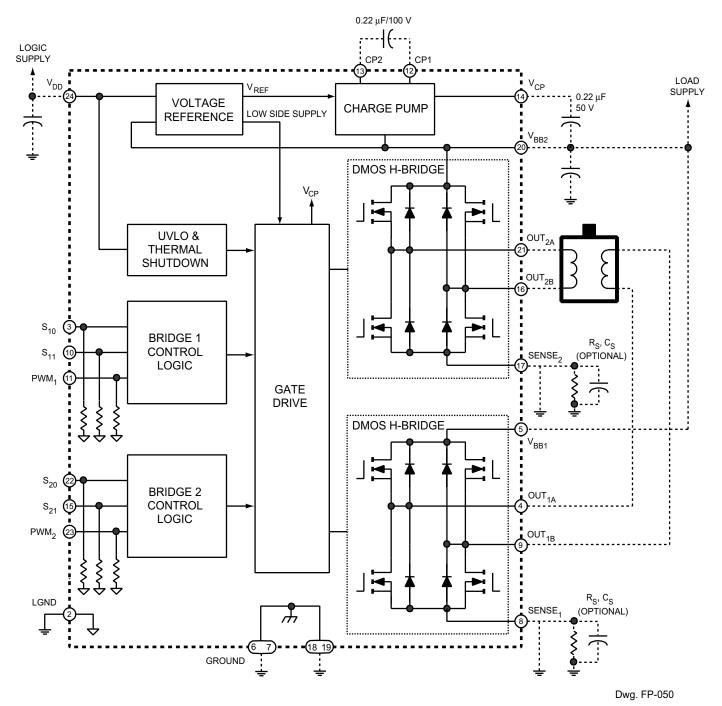
The A3971SLB is supplied in a 24-lead plastic SOIC with a copper batwing tab. The power tab is at ground potential and needs no electrical isolation.

Pinout

Pin	Name		Pin	Name
1	NC — NO CONNECTION		24	V_DD — LOGIC SUPPLY
2	LOGIC GROUND		23	PWM2
3	S10		22	S20
4	OUT1A		21	OUT2A
5	LOAD SUPPLY1 / V_BB1		20	LOAD SUPPLY2 / V_BB2
6	GROUND		19	GROUND
7	GROUND		18	GROUND
8	SENSE1		17	SENSE2
9	OUT1B		16	OUT2B
10	S11		15	S21
11	PWM1		14	V_CP
12	CP1	CHARGE PUMP	13	CP2

Dwg. PP-069-2

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Load Supply Voltage, V_{BB} .... **50 V**
Output Current, I_{OUT}
    Transient (<500 ns) .... **±5 A**
Logic Supply Voltage,
    V_{DD} .... **7.0 V**
Sense Voltage, V_{SENSE} .... **0.5 V**
Logic Input Voltage Range,
    V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
High-Side Gate Voltage .... **V_{BB} + 8 V**
Package Power Dissipation,
    P_D .... **2.2 W**
Operating Temperature Range,
    T_A .... **-20°C to +85°C**
Junction Temperature, T_J .... **+150°C**
Storage Temperature Range,
    T_S .... **-55°C to +150°C**

Output duty cycle, ambient temperature, and heat sinking may limit current rating. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150 °C.

FEATURES

■ ±2.5 A Load Current Capability per Bridge

■ Parallel Outputs for 5 A Load-Current Capability

■ Low $r_{DS(on)}$ Outputs
   Typically 325 mΩ source, 175 mΩ sink

■ Synchronous Rectification via Control Logic

■ Internal Undervoltage Monitor

■ Crossover-Current Protection

■ Source Connections for External Current Sensing

■ Thermal Shutdown Circuitry

Always order by complete part number: **A3971SLB** .

Allegro

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FUNCTIONAL BLOCK DIAGRAM

Dwg. FP-050

ELECTRICAL CHARACTERISTICS at T$_A$ = +25°C, V$_{BB}$ = 50 V, V$_{DD}$ = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
			\[Limits\]			
Load Supply Voltage Range	V$_{BB}$	Operating	10	—	50	V
Logic Supply Voltage Range	V$_{DD}$	Operating	4.5	5.0	5.5	V
Load Supply Current	I$_{BB}$	Operating, each supply, no load	—	—	3.0	mA
Logic Supply Current	I$_{DD}$	Operating	—	—	5.0	mA
Output Drivers						
Output Leakage Current	I$_{DSS}$	V$_{OUT}$ = V$_{BB}$	—	<1.0	20	µA
		V$_{OUT}$ = 0 V	—	<-1.0	-20	mA
Output ON Resistance	r$_{DS(on)}$	High-side switch, I$_{OUT}$ = -2.5 A	—	325	375	mΩ
		Low-side switch, I$_{OUT}$ = 2.5 A	—	175	200	mΩ
Body Diode Forward Voltage	V$_F$	Source diode, I$_F$ = 2.5 A	—	1.2	—	V
		Sink diode, I$_F$ = 2.5 A	—	1.0	—	V
High-Side Gate Voltage	V$_{CP}$	C = 0.22 µF, reference V$_{BB}$	6.0	6.5	7.0	V
Control Logic						
Logic Input Voltage	V$_{IN(0)}$		—	—	0.8	V
	V$_{IN(1)}$		2.0	—	—	V
Logic Input Current	I$_{IN(0)}$	V$_{IN}$ = 0 V	—	<1.0	-5.0	µA
	I$_{IN(1)}$	V$_{IN}$ = 5.0 V	—	20	50	µA
Propagation Delay Time	t$_{PD}$	50% to 90%:				
		PWM change to source off	—	50	—	ns
		PWM change to sink off	—	60	—	ns
		PWM change to source on	—	565	—	ns
		PWM change to sink on	—	665	—	ns
		Disable to source on	—	150	—	ns
		Disable to sink on	—	250	—	ns
Thermal Shutdown Temperature	T$_J$		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT$_J$		—	15	—	°C
UVLO Threshold	V$_{UVLO}$	Increasing V$_{DD}$	3.9	4.15	4.4	V
UVLO Hysteresis	ΔV$_{UVLO}$		—	0.15	—	V

NOTES: 1. Typical Data is for design information only.
   2. Negative current is defined as coming out of (sourcing) the specified device terminal.

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Logic Truth Table

PWM$_x$	S$_{x0}$	S$_{x1}$	OUT$_{xA}$	OUT$_{xB}$	Function
X	0	0	Z	Z	Disable
0	0	1	L	H	Forward
0	1	0	H	L	Reverse
0	1	1	L	L	Synchronous
1	0	1	L	L	Rectification/
1	1	1	L	L	Slow Decay
1	1	0	L	L	Chop

Terminal List

Terminal	Name	Description
1	NC	No (Internal) connection
2	LGND	Logic ground
3	S$_{10}$	Control input, bridge 1
4	OUT$_{1A}$	Output A, bridge 1
5	V$_{BB1}$	Load supply voltage, bridge 1
6, 7	GND	Ground
8	SENSE$_1$	Sense resistor, bridge 1
9	OUT$_{1B}$	Output B, bridge 1
10	S$_{11}$	Control input, bridge 1
11	PWM$_1$	Control input, bridge 1
12	CP1	Charge-pump capacitor
13	CP2	Charge-pump capacitor
14	V$_{CP}$	Reservoir capacitor
15	S$_{21}$	Control input, bridge 2
16	OUT$_{2B}$	Output B, bridge 2
17	SENSE$_2$	Sense resistor, bridge 2
18, 19	GND	Ground
20	V$_{BB2}$	Load supply voltage, bridge 2
21	OUT$_{2A}$	Output A, bridge 2
22	S$_{20}$	Control input, bridge 2
23	PWM$_2$	Control input, bridge 2
24	V$_{DD}$	Logic supply voltage

Functional Description

Charge Pump. The DMOS output stage requires a charge pump to bring the high-side gate-source voltage approximately 8 V above the V_{BB} supply. Two external components are required, a pumping capacitor connected between CP1 and CP2 and a reservoir capacitor connected between V_{BB} and V_{CP}. Ceramic 0.22 µF capacitors are recommended.

Control Logic. Each bridge is controlled by three TTL-compatible inputs. The inputs are resistively pulled to ground (via 250 kΩ). A crossover-delay circuit protects the outputs from a shoot-thru condition when going from a forward or reverse on state to synchronous rectification/slow decay chop (both sink drivers on). If the logic is in the DISABLE state and changes to an on state the 415 ns crossover delay does not occur.

Protection Circuitry. In the event of a fault due to excessive junction temperature, or low voltage on V_{CP} or V_{DD}, the outputs of the device are disabled until the fault condition is removed.
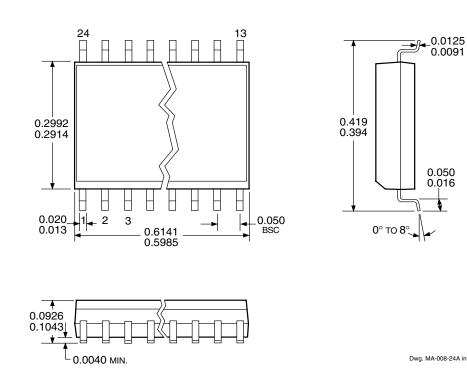
Current Sensing. If external current-sensing circuitry is used, the sense resistor should have an independent ground return to the ground terminal of the device. Due to current transients during switching, a 0.1 µF capacitor should be connected from the sense terminal to the batwing tab connection of the package. This capacitor reduces voltage swings at the terminal due to the fast di/dt, which in turn ensures that the sink driver gate-source voltage stays within the safe operating area. Allegro MicroSystems recommends a value of R_S given by:

$$R_S = 0.5/I_{TRIP} \text{ max.}$$

Thermal protection. Circuitry turns off all drivers when the junction temperature reaches 165°C, typically. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

Layout. The printed wiring board should use a heavy ground plane. For optimum electrical and thermal performance, the driver should be soldered directly onto the board. If external current sensing is used, the ground side of R_S should have an individual path to the ground terminal(s) of the device. This path should be as short as is possible physically and should not have any other components connected to it. The load supply terminal should be decoupled with an electrolytic capacitor (>47 µF is recommended) placed as close to the device as is possible.

Parallel Operation. For high-power applications, the two DMOS full bridges in the A3971 may be connected in parallel as shown below. The current will be shared equally in each full bridge due to the positive temperature coefficient of the DMOS $r_{DS(on)}$.

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Dimensions in Inches
(for reference only)

24   13

0.2992
0.2914

0.020
0.013

1   2   3

0.6141
0.5985

0.050
BSC

0.0125
0.0091

0.419
0.394

0.050
0.016
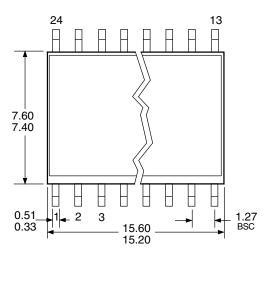
0° TO 8°

0.0926
0.1043

0.0040 MIN.

Dwg. MA-008-24A in
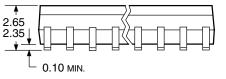
NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative
3. Webbed lead frame. Leads 6, 7, 18, and 19 are internally one piece.

Dimensions in Millimeters
(controlling dimensions)

Dwg. MA-008-24A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative
3. Webbed lead frame. Leads 6, 7, 18, and 19 are internally one piece.

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