DATA SHEET

74LVC823A

9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

Product specification

1998 Sep 24

Philips Semiconductors

PHILIPS

9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

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FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 9-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Flow-through pin-out architecture

DESCRIPTION

The 74LVC823A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-state operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC823A is a 9-bit D-type flip-flop with common clock (CP), Clock Enable ($\overline{CE}$), Master Reset ($\overline{MR}$) and 3-State outputs for bus-oriented applications.

The nine flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition provided $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH the flip-flops hold their data.

A LOW on $\overline{MR}$ resets all flip-flops.

When $\overline{OE}$ is LOW, the contents of the nine flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	5.1	ns
	Propagation delay MR to Q_n		5.2	ns
f_{max}	Maximum clock frequency	C_L = 50 pF; V_{CC} = 3.3 V	150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	27	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDERING CODE	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC823A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC823A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC823A PW	SOT355-1

9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

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PIN DESCRIPTION

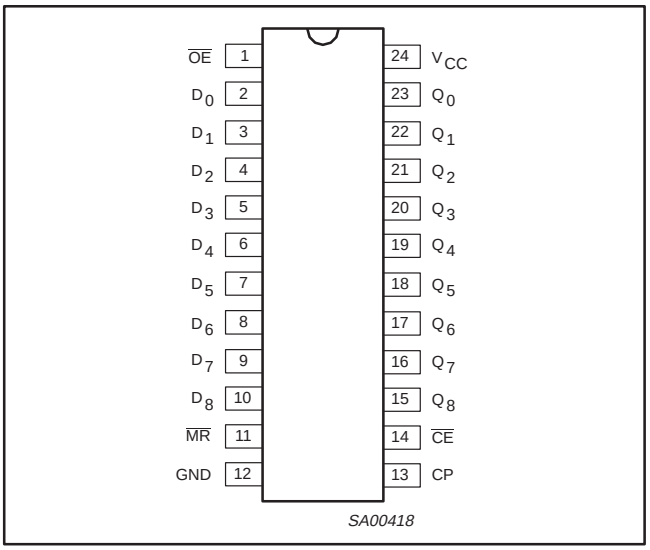
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10	D_0 to D_8	Data inputs
11	$\overline{MR}$	Master reset (active LOW)
12	GND	Ground (0 V)
13	CP	Clock pulse (active rising)
14	$\overline{CE}$	Clock enable (active LOW)
23, 22, 21, 20, 19, 18, 17, 16, 15	Q_0 to Q_8	3-State flip-flop outputs
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

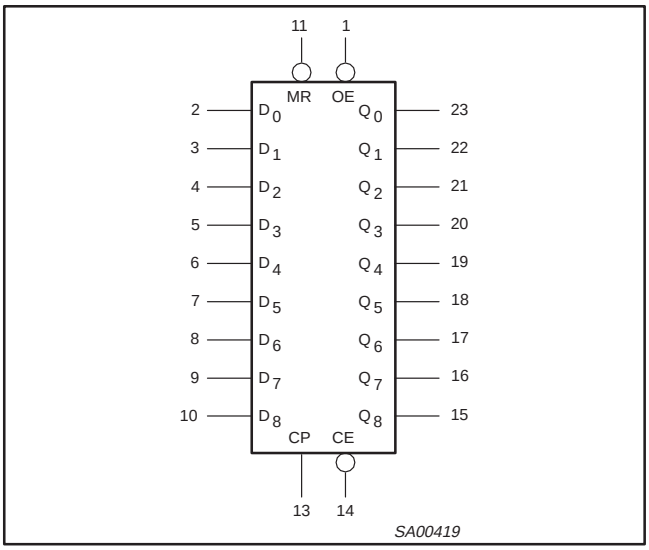
OPERATING MODES	INPUTS					INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	D_n		Q_0 to Q_8
Clear	L	L	X	X	X	L	L
Load and read register	L L	H H	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	H H	L L	X X	l h	L H	Z Z
Hold	L	H	H	NC	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW–to–HIGH clock transition
NC= no change

PIN CONFIGURATION



LOGIC SYMBOL



9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

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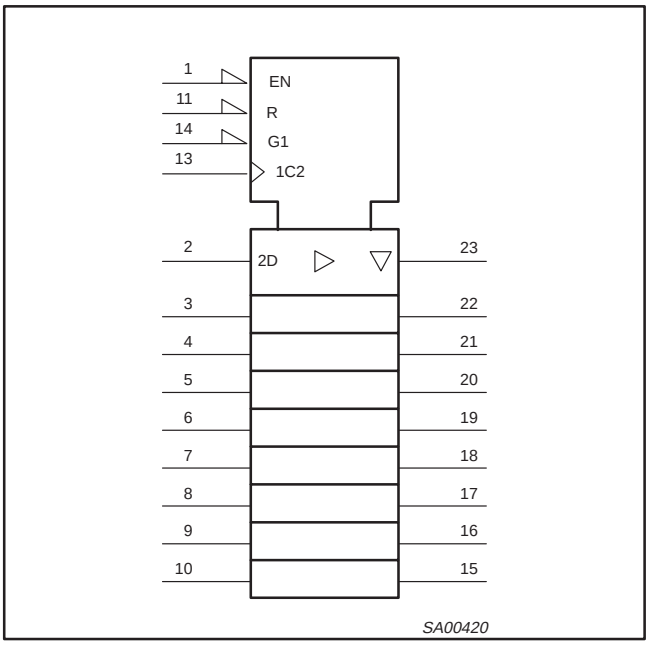
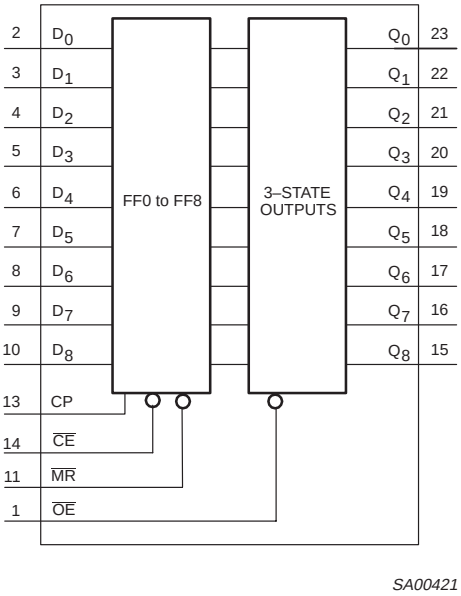
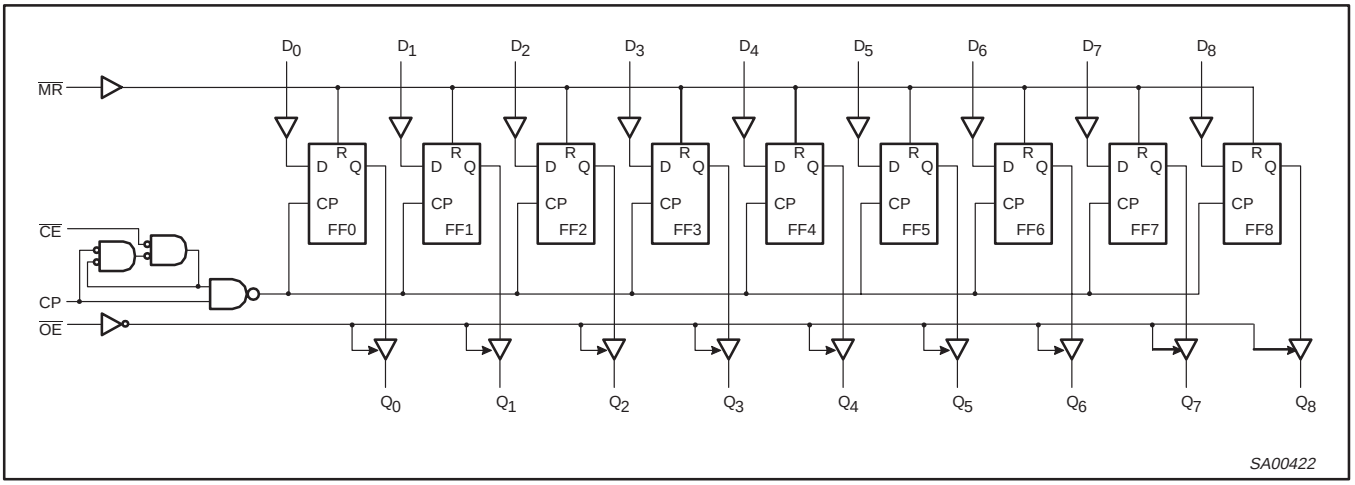
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or $V_{IL;}$ I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or $V_{IL;}$ I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or $V_{IL;}$ I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL} t_{PLH}	Propagation delay CP to Q_n	Figures 1, 4	1.5	5.1	8.0	1.5	8.9	ns
t_{PHL}	Propagation delay MR to Q_n	Figures 1, 4	1.5	5.2	7.9	1.5	8.8	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	Figures 2, 4	1.5	5.2	7.65	1.5	8.65	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	Figures 2, 4	1.5	3.8	6.0	1.5	7.1	ns
t_W	Clock pulse width HIGH or LOW	Figure 1	3.3			3.3		ns
t_W	Master Reset pulse width HIGH or LOW	Figure 1	3.3			3.3		ns
t_{SU}	Setup time D_n to CP	Figure 3	1.3			1.8		ns
t_{SU}	Setup time CE low before CP	Figure 3	1.8			1.0		ns
t_{rem}	Removal time MR	Figure 3	1.0			2.0		ns
t_h	Hold time HIGH or LOW Dn after CP	Figure 3	2.0			2.0		ns
t_h	Hold time CE LOW before CP	Figure 3	1.3			1.3		ns
f_{max}	Maximum clock pulse frequency	Figure 1	150	200		150		MHz

NOTE:

1. Unless otherwise stated, all typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25°C$.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V

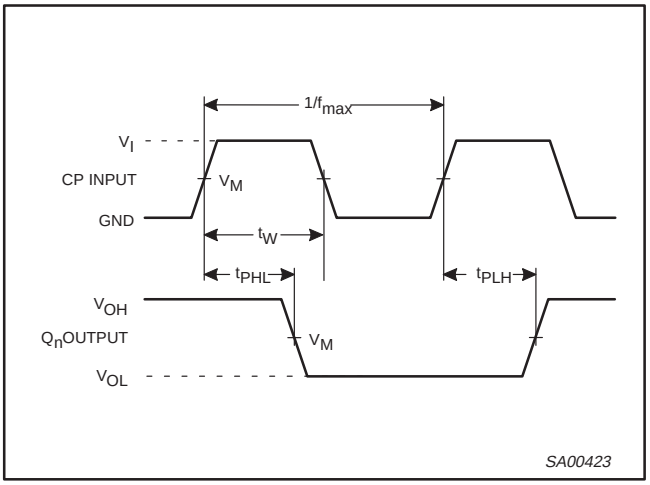


Figure 1. Clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

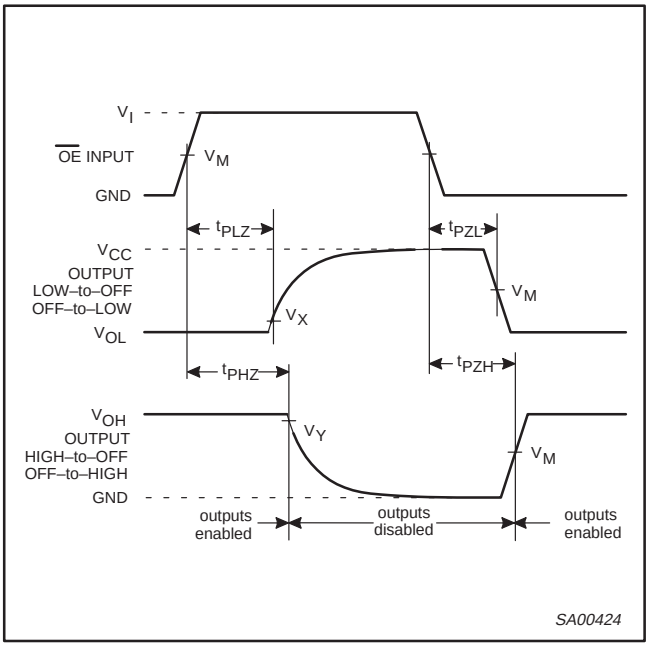


Figure 2. 3-State enable and disable times.

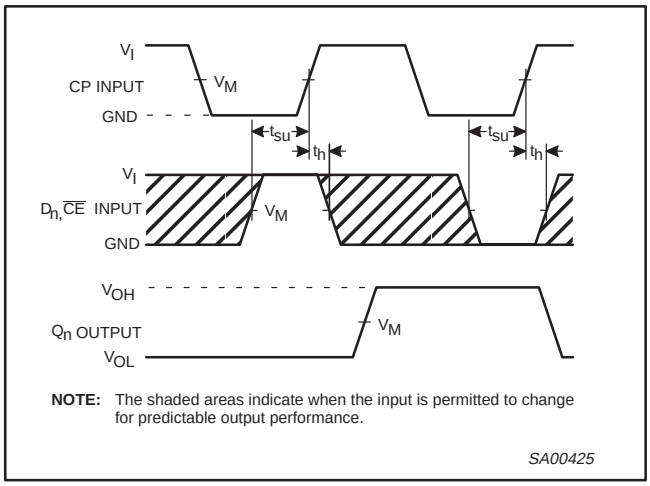


Figure 3. Data setup and hold times for the D_n input and $\overline{CE}$ input to the CP input.

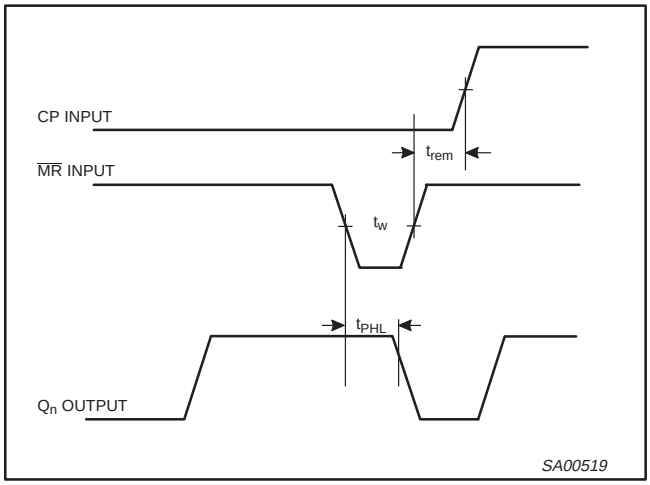
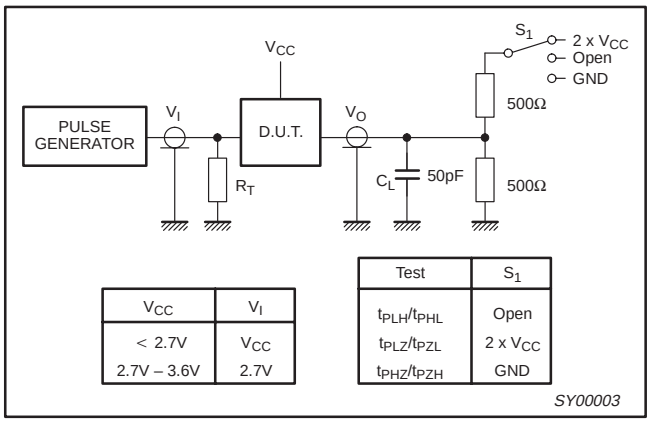


Figure 4. Master reset pulse width, master reset to clock removal time, master reset to output propagation delay.

TEST CIRCUIT

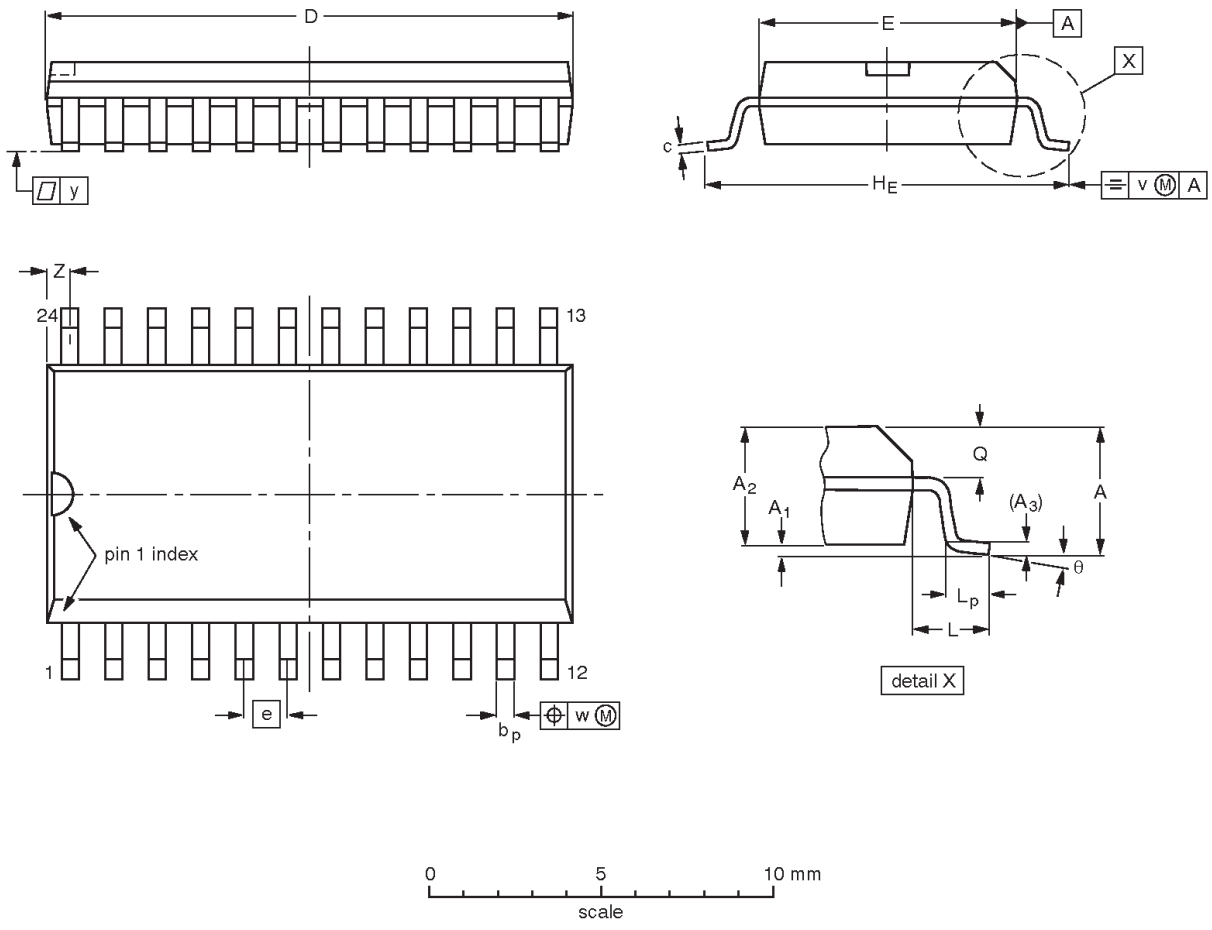


V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 5. Load circuitry for switching times.

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

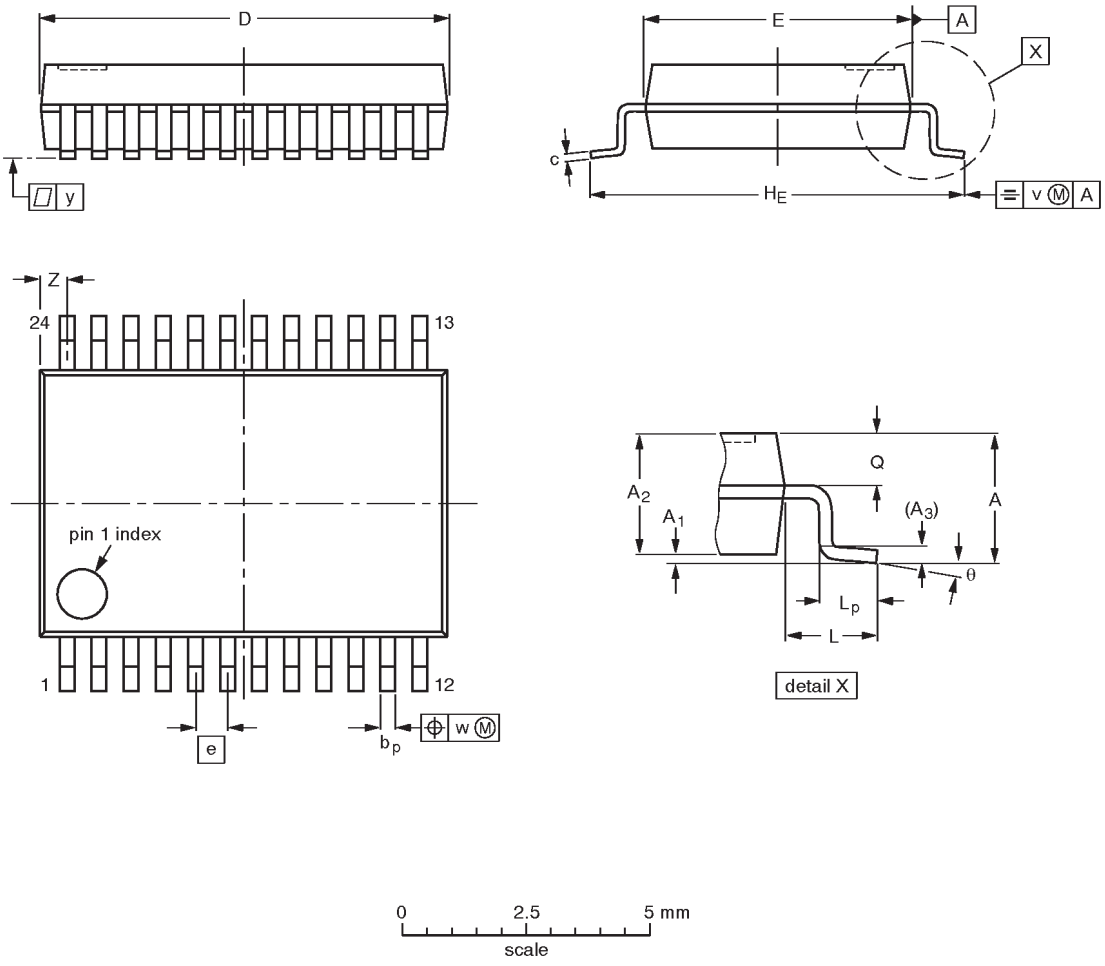
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

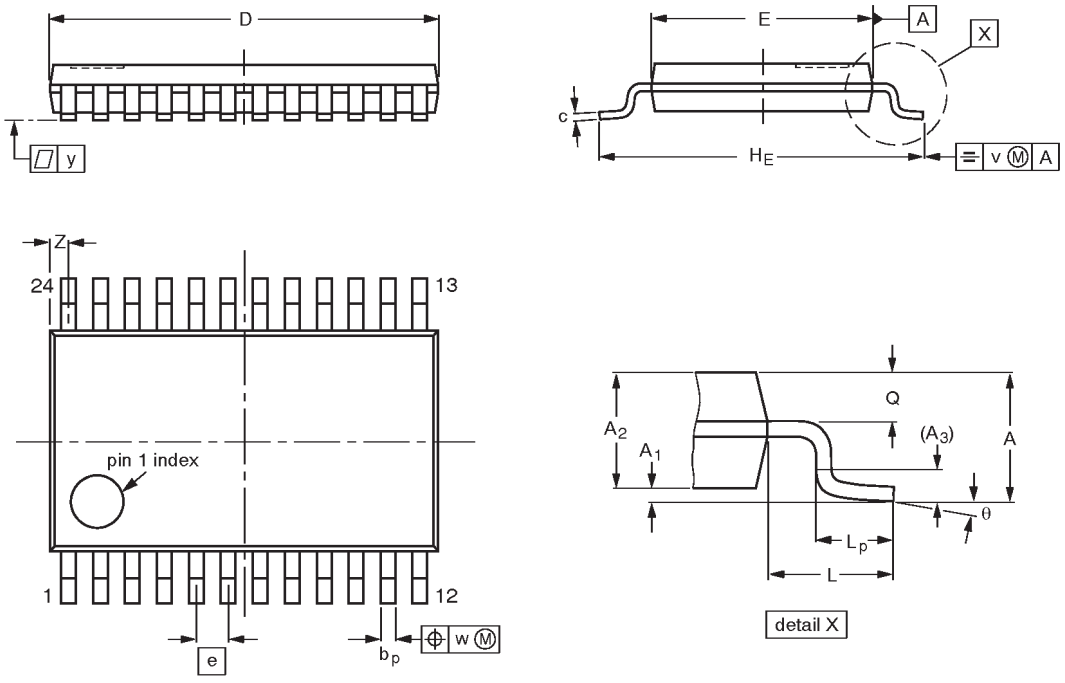
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

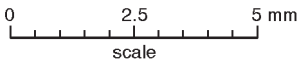
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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