Precision Quad SPDT Analog Switch

FEATURES

- ±22-V Supply Voltage Range
- TTL and CMOS Compatible Logic
- Low On-Resistance (25 Ω)
- On-Resistance Matched Between Channels (<2 Ω)
- Flat On-Resistance Over Analog Signal Range (Δ <3 Ω)
- Low Charge Injection (1 pC)
- Low Leakage (0.2 nA)
- Fast Switching (175 ns)
- Single-Supply Operation (5 V to 40 V)
- ESD tolerance >2 kV per 3015.x
- Low Power (<1 μA) – DG333A/333AL

BENEFITS

- Rail-to-Rail Analog Signal Range
- Simple Logic Interface
- High Precision and Accuracy
- Minimal Transients
- Low Distortion
- Reduced Power Consumption
- Improved Reliability
- Break-Before-Make Switching Action

APPLICATIONS

- Audio Switching
- Test Equipment
- Portable Instrumentation
- Communication Systems
- PBX, PABX
- Computer Peripherals
- Mass Storage Systems
- Switched-Capacitor Networks
- Battery-Powered Systems

DESCRIPTION

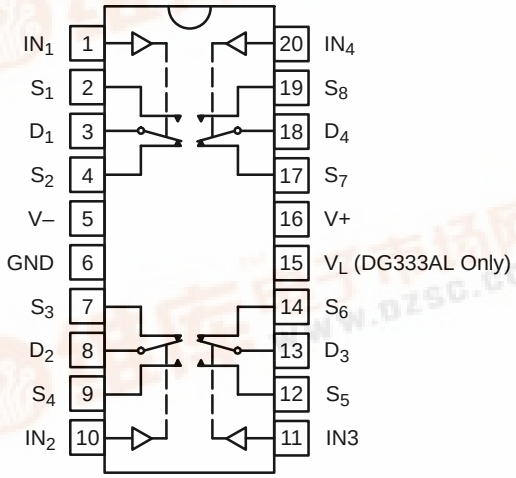
The DG333A/333AL consist of four independently controlled single-pole double-throw analog switches. These monolithic switch is designed to control analog signals with a high degree of accuracy. The DG333A/333AL minimize measurement errors by offering low on-resistance (25-Ω typ), low leakage (20-pA typ) and low charge injection performance. The DG333AL features micro-power operation (<1-μW typ). This is ideal for battery operated systems. Pin 15 is not connected on the DG333A.

An improved charge injection compensation design minimizes switching transients. These switches can handle up to ±22-V signals and have an improved continuous current of 30 mA.

The DG333A/333AL is fabricated in Vishay Siliconix's proprietary HVSG-2 CMOS process, resulting in higher speed and lower power consumption. An epitaxial layer prevents latchup. Each switch conducts equally well in both directions when on. When off, they block voltages up to the power-supply levels.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line and Wide-Body SOIC



Top View

TRUTH TABLE

Logic	SW1, 4, 5, 8 Normally Open	SW2, 3, 6, 7 Normally Closed
0	Off	On
1	On	Off

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
–40 to 85°C	20-Pin Plastic DIP	DG333ADJ
		DG333ALDJ
	20-Pin Wide-Body SOIC	DG333ADW
		DG333ALDW

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ . . . . . 44 V
GND . . . . . 30 V
V+ to GND . . . . . 30 V
Digital Inputs[a] V_S, V_D . . . . . (V–) –2 V to (V+) +2 V
or 30 mA, whichever occurs first
Current, Any Terminal . . . . . 30 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) . . . . . 100 mA

Storage Temperature . . . . . –65 to 125°C
Power Dissipation (Package)b
20-Pin Plastic DIP[c] . . . . . 890 mW
20-Pin Wide SOIC[d] . . . . . 800 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 12 mW/°C above 75°C
d. Derate 10 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

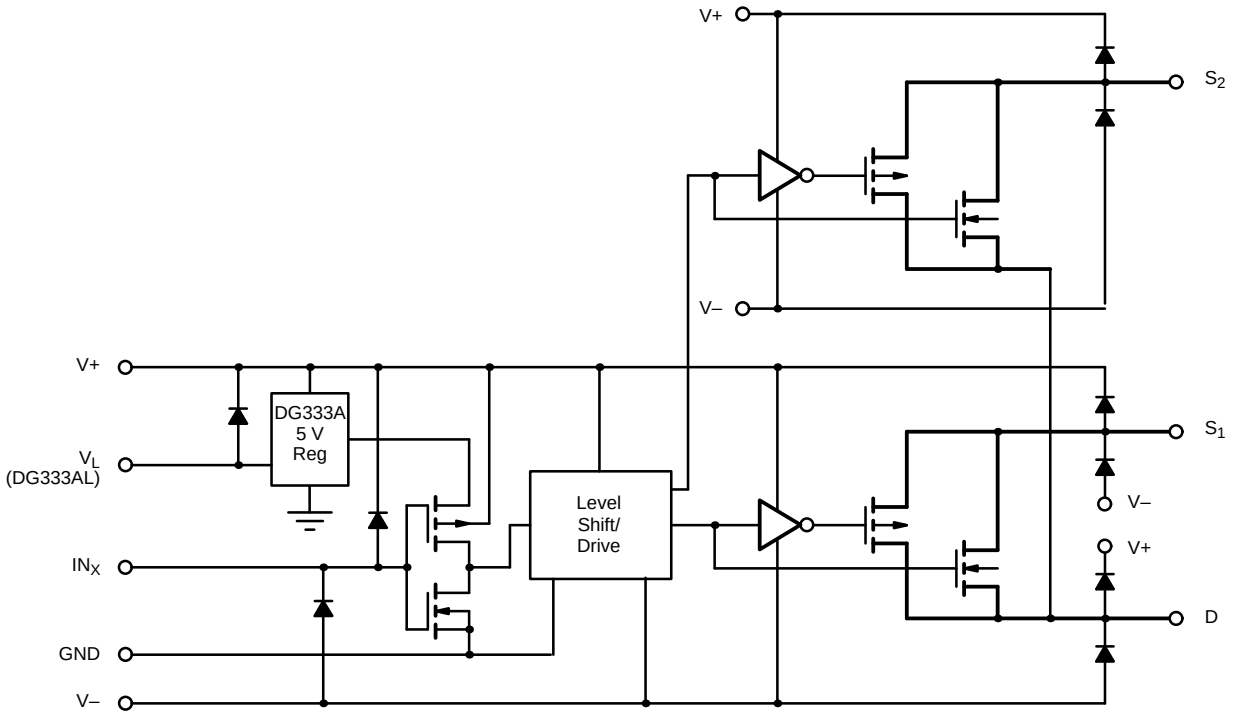


FIGURE 1.

SPECIFICATIONS

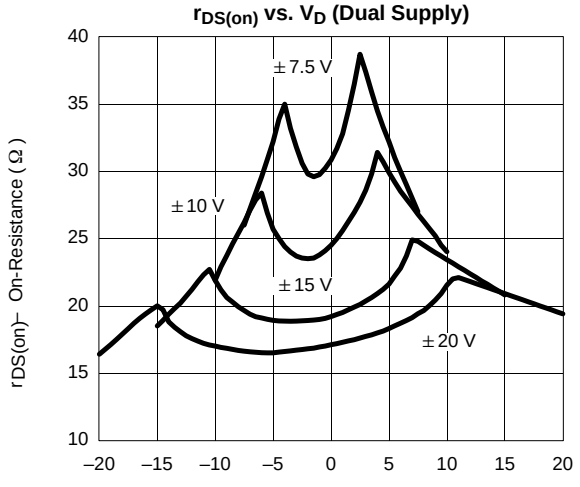
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_{IN} = 2.4 V, 0.8 V[e]	Limits D Suffix –40 to 85°C Temp[a]	Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	V–		V+	V
Channel On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = ±10 V	Room Full		25	45 90	Ω
On-Resistance Flatness		I_S = –10 mA, V_D = ±5 V V+ = 16.5 V, V– = –16.5 V	Room Full			3 5	
$r_{DS(on)}$ Match Between Channels[f]	$\Delta r_{DS(on)}$	I_S = –10 mA, V_D = ±10 V	Room Full			2 4	
Source Off Leakage Current	$I_{S(off)}$	V_D = ±15.5 V, V_S = ∓15.5 V V+ = 16.5V, V– = –16.5 V	Room Hot	–0.25 –20		0.25 20	nA
Channel On Leakage Current	$I_{D(on)}$	V_D = ±15.5 V, $V_{S(open)}$ = ∓15.5 V V+ = 16.5V, V– = –16.5 V	Room Hot	–0.75 –60		0.75 60	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	
Input Current	I_{INH} or I_{INL}	V_{INH} or V_{INL}	Full	–1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	See Switching Time Test Circuit Figure 2	Room			175	ns
Turn-Off Time	t_{OFF}		Room			145	
Break-Before-Make Time Delay	t_D	See Figure 3	Room	5			
Charge Injection[d]	Q	C_L= 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room			10	pC
Off Isolation	OIRR	R_L = 75 Ω, C_L = 5 pF V_D = 2.3 V_{RMS}, f = 1 MHz	Room		72		dB
Channel-to-Channel Crosstalk	X_{TALK}		Room		80		
Off Capacitance	C_{OFF}	f = 1 MHz, V_S = 0 V	Room		8		pF
Channel On Capacitance	C_{ON}		Room		12		
Power Supplies							
Positive Supply Current	I+	DG333A: V_{IN} = 0 or 5 V	Room			200	µA
Negative Supply Current	I–		Room	–1			
Positive Supply Current	I+	DG333AL: V_{IN} = 0 or 5 V, V_L = 5 V	Room			1	
Logic Supply Current	I_L		Room			1	
Negative Supply Current	I–		Room	–1			
Supply Voltage Range	V+/V–		Full	±4		±22	V

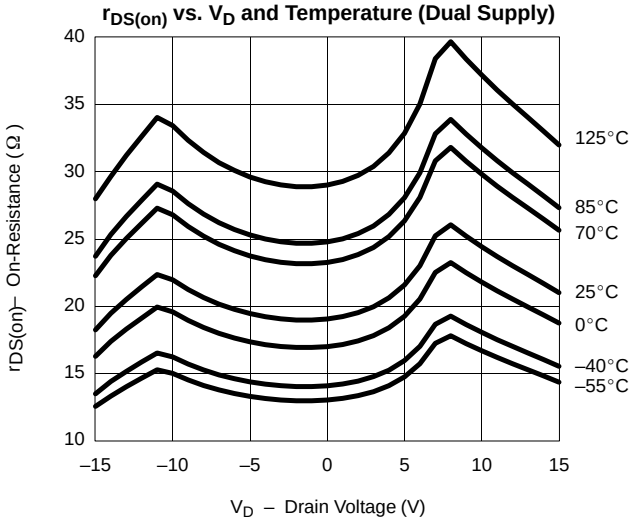
SPECIFICATIONS (UNIPOLAR SUPPLIES)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V– = –0 V T_A = 25°C	Limits D Suffix –40 to 85°C Temp[a]	Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	V–		V+	V
Channel On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = 10, 1 V	Room		35	75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_D = 11 V, $V_{S(open)}$ = 1 V	Room			0.25	nA
Channel On Leakage Current	$I_{D(on)}$	V_D = 11 V, $V_{S(open)}$ = 0 V V_D = 1 V, $V_{S(open)}$ = V+	Room			0.75	nA
Dynamic Characteristics							
Turn-On Time	t_{ON}	See Switching Times Test Circuit Figure 2	Room		90		ns
Turn-Off Time	t_{OFF}		Room		45		ns
Break-Before-Make Time Delay	t_D	See Figure 3	Room	5	10		ns
Power Supplies							
Positive Supply Current	I+	DG333A: V_{IN} = 0 or 5 V	Room			200	µA
			Room			1	µA
Positive Supply Current	I+	DG333AL: V_{IN} = 0 or 5 V, V_L = 5 V	Room			1	µA
Logic Supply Current	I_L		Room			1	µA
Positive Supply Range	V+		Room	5		40	V

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.
f. On-resistance match and flatness are guaranteed only for bipolar supply operation.

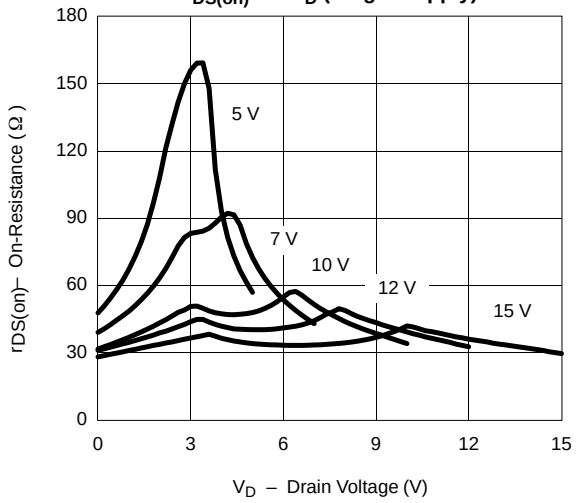
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



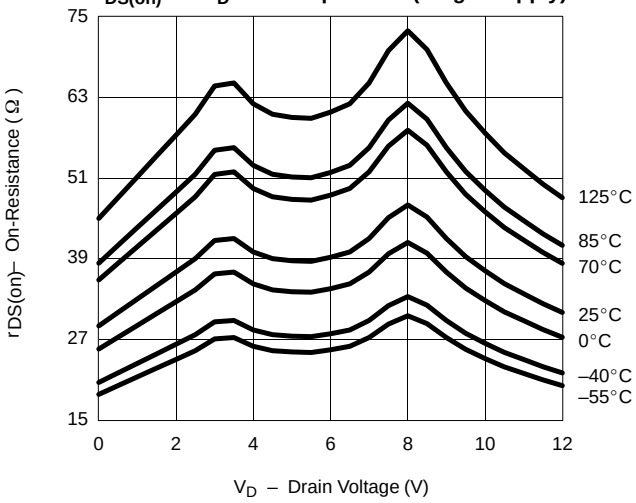


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

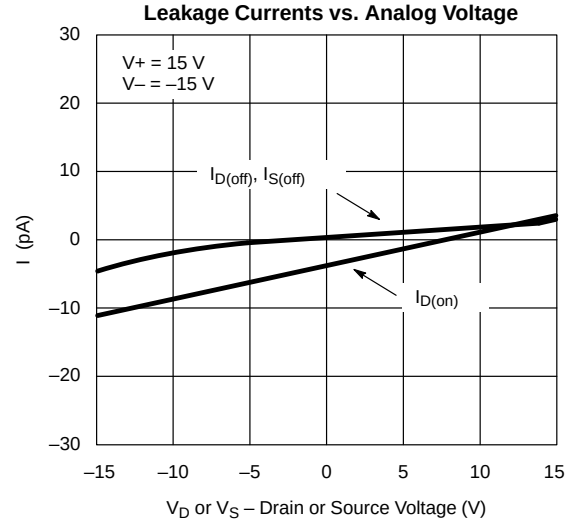
$r_{DS(on)}$ vs. V_D (Single Supply)



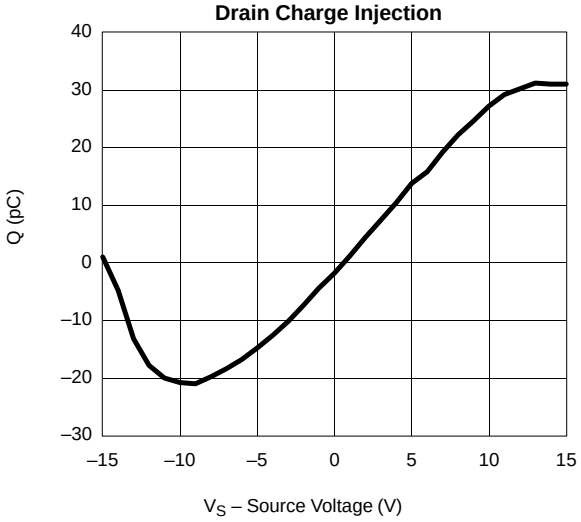
$r_{DS(on)}$ vs. V_D and Temperature (Single Supply)



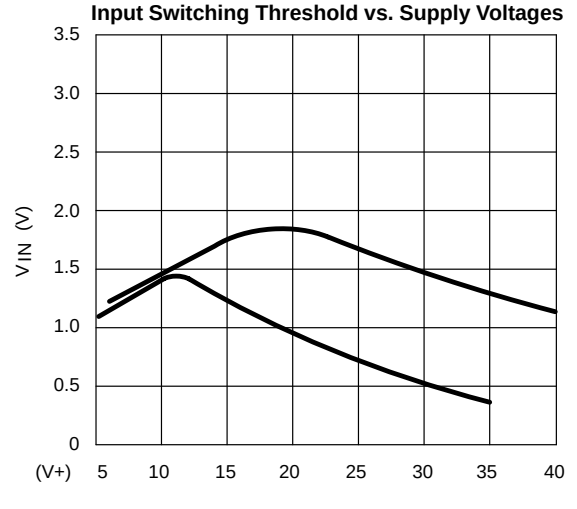
Leakage Currents vs. Analog Voltage



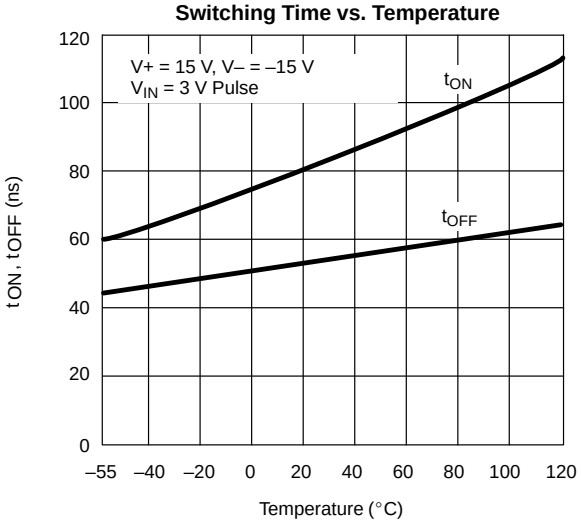
Drain Charge Injection



Input Switching Threshold vs. Supply Voltages

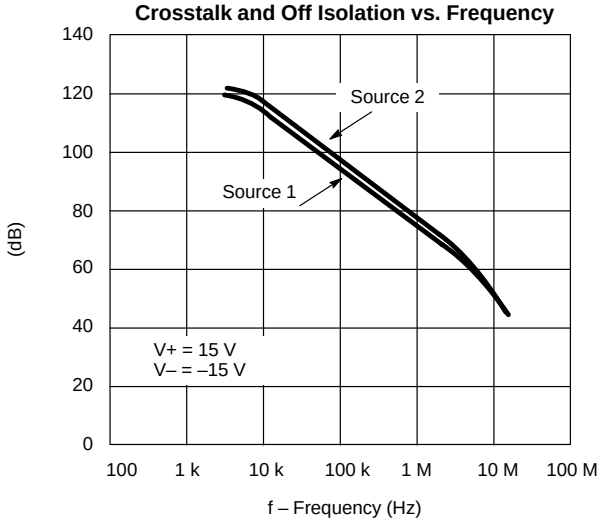


Switching Time vs. Temperature

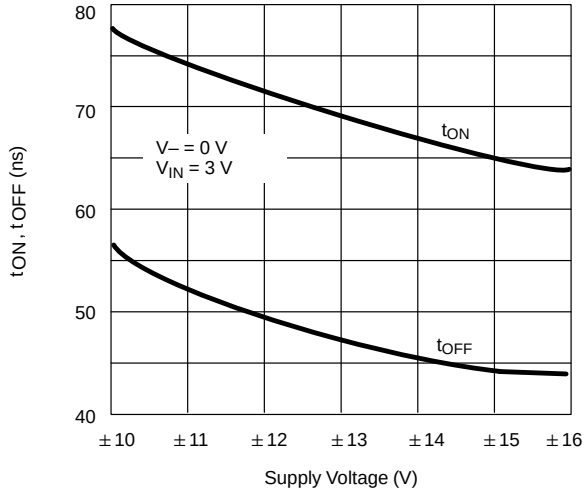


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

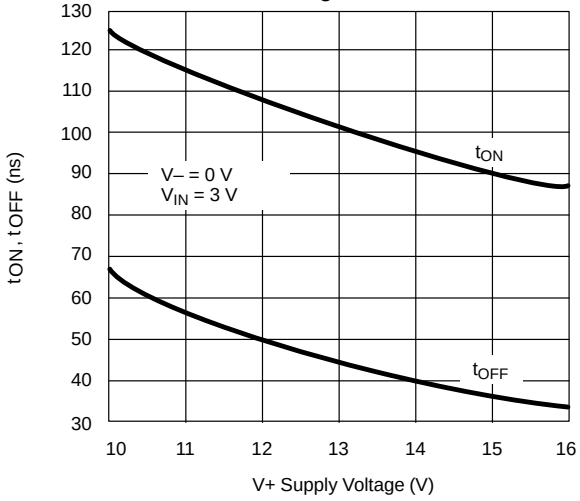
Crosstalk and Off Isolation vs. Frequency



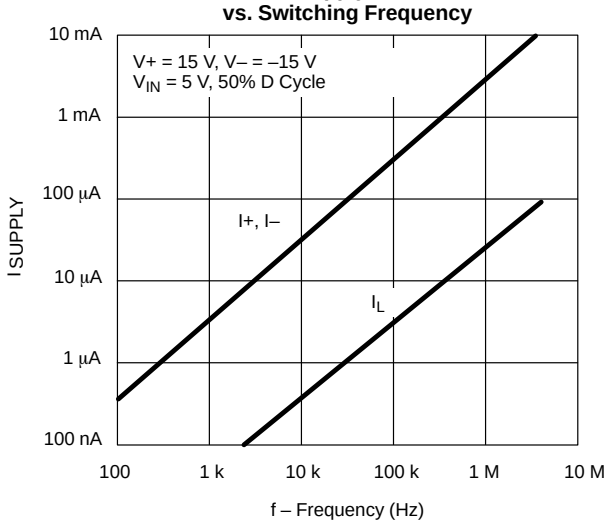
Switching Time vs. Supply Voltages



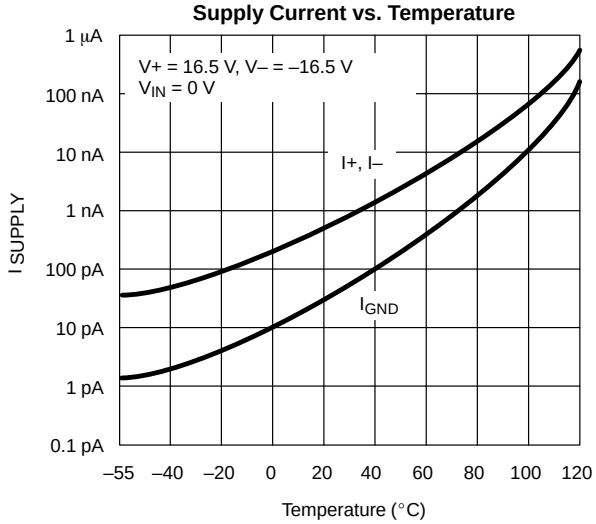
Switching Time vs. V+



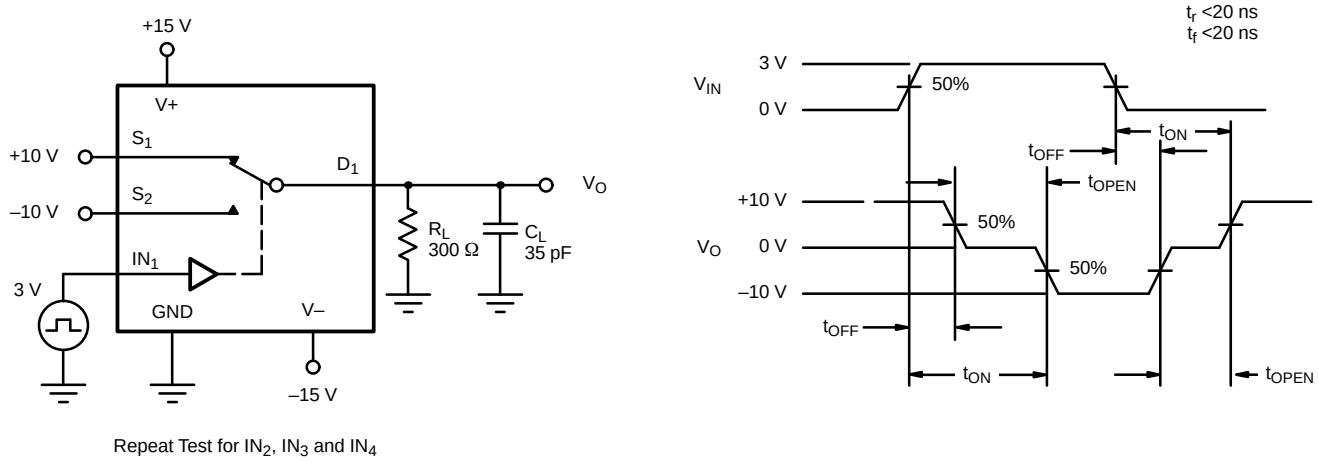
Power Supply Currents vs. Switching Frequency



Supply Current vs. Temperature

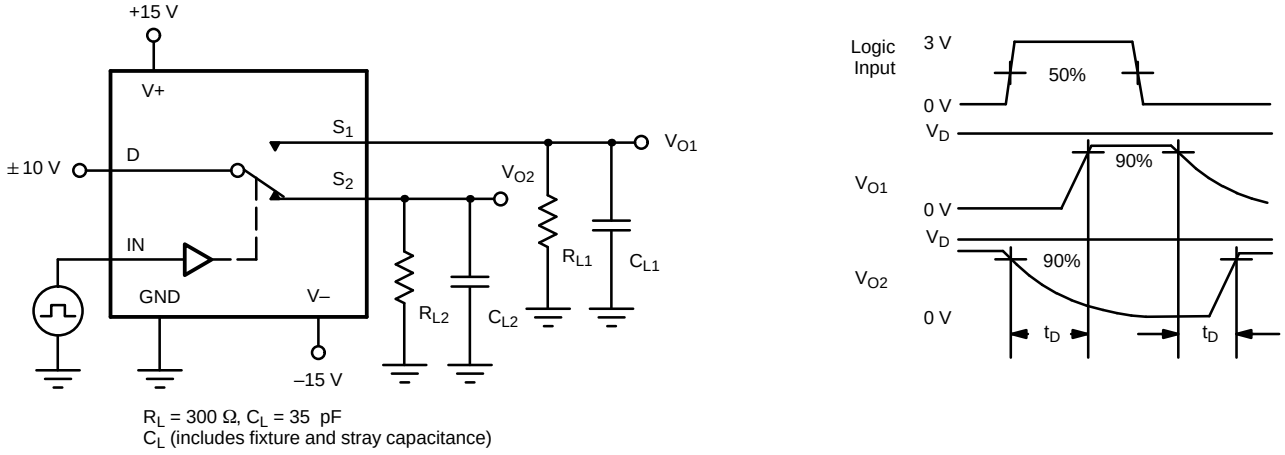


TEST CIRCUITS



Repeat Test for IN_2, IN_3 and IN_4

FIGURE 2. Switching Times



R_L = 300 Ω, C_L = 35 pF
C_L (includes fixture and stray capacitance)

FIGURE 3. Break-Before-Make

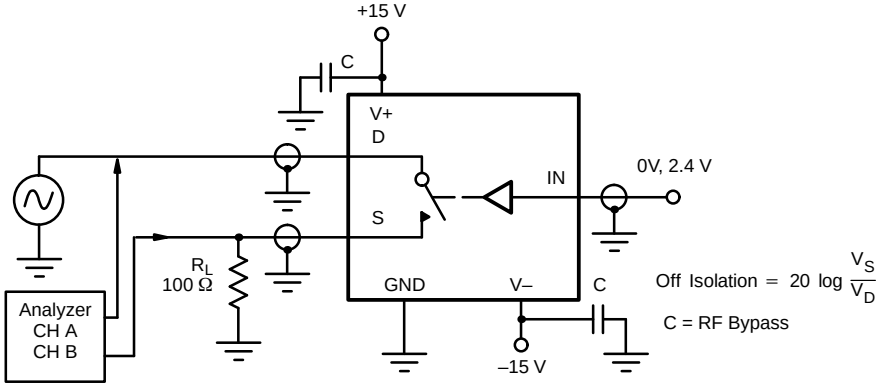


FIGURE 4. Off Isolation

TEST CIRCUITS

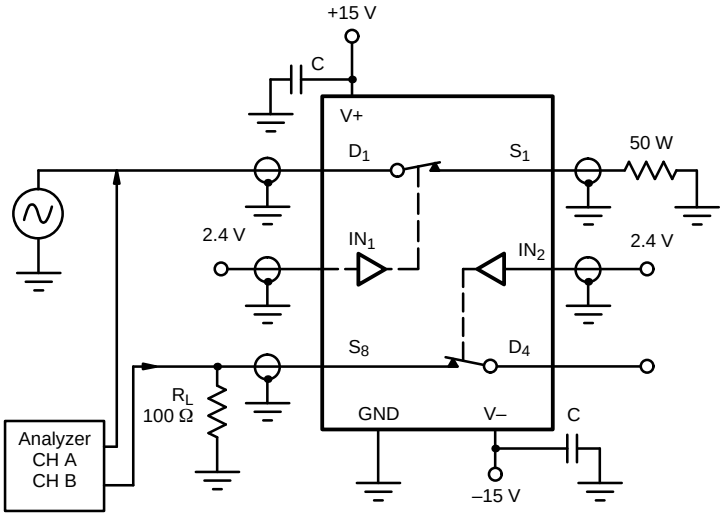


FIGURE 5. Crosstalk

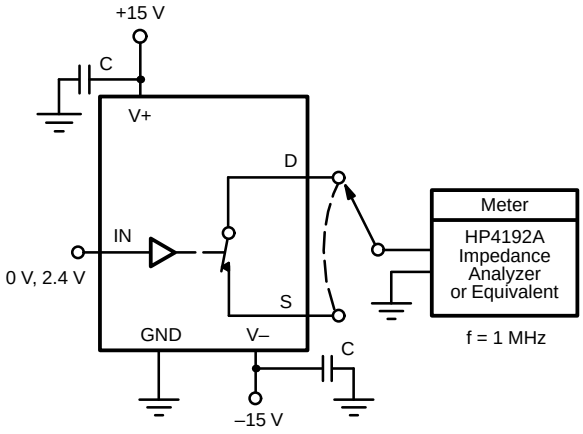


FIGURE 6. Capacitances

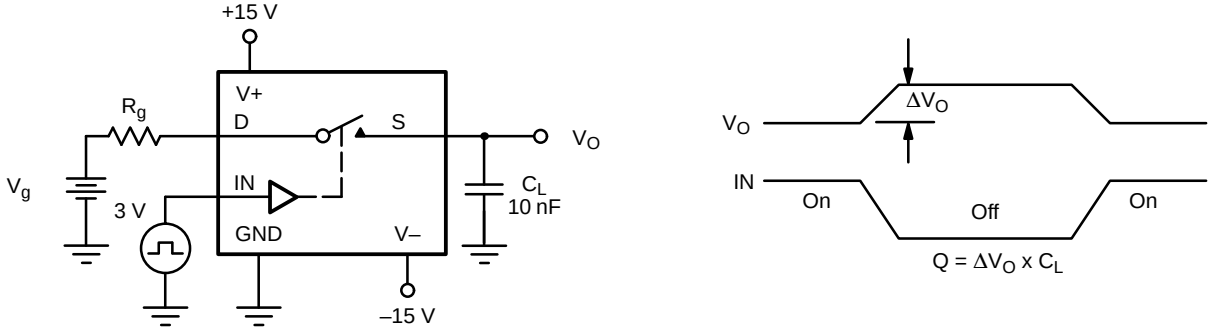


FIGURE 7. Charge Injection

APPLICATIONS

Band-Pass Switched Capacitor Filter

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG333A/333AL allow for higher clock rates and consequently higher filter operating frequencies. Figure 8 shows two capacitors being switched. The DG333A/333AL is capable of switching four capacitors.

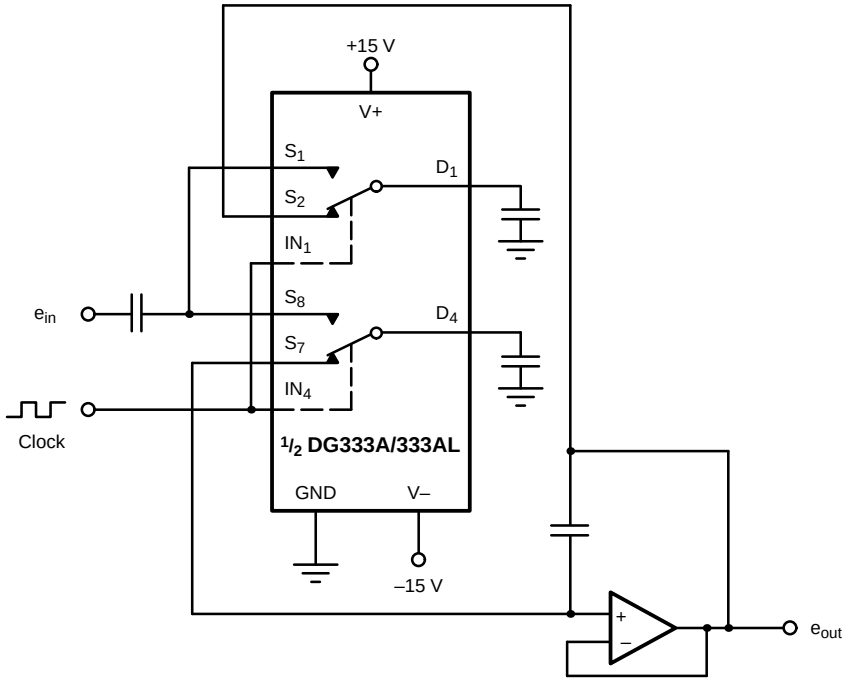


FIGURE 8. Band-Pass Switched Capacitor Filter