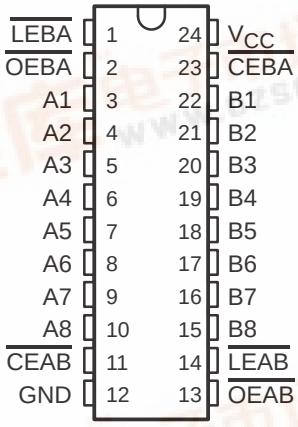
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (JT)**

DB, DW, OR NT PACKAGE
(TOP VIEW)



description

The SN74ABT543A octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT543A is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74ABT543A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

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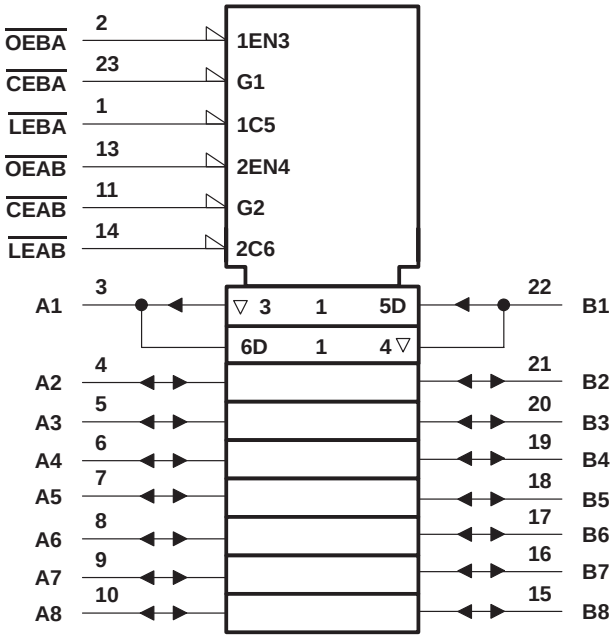
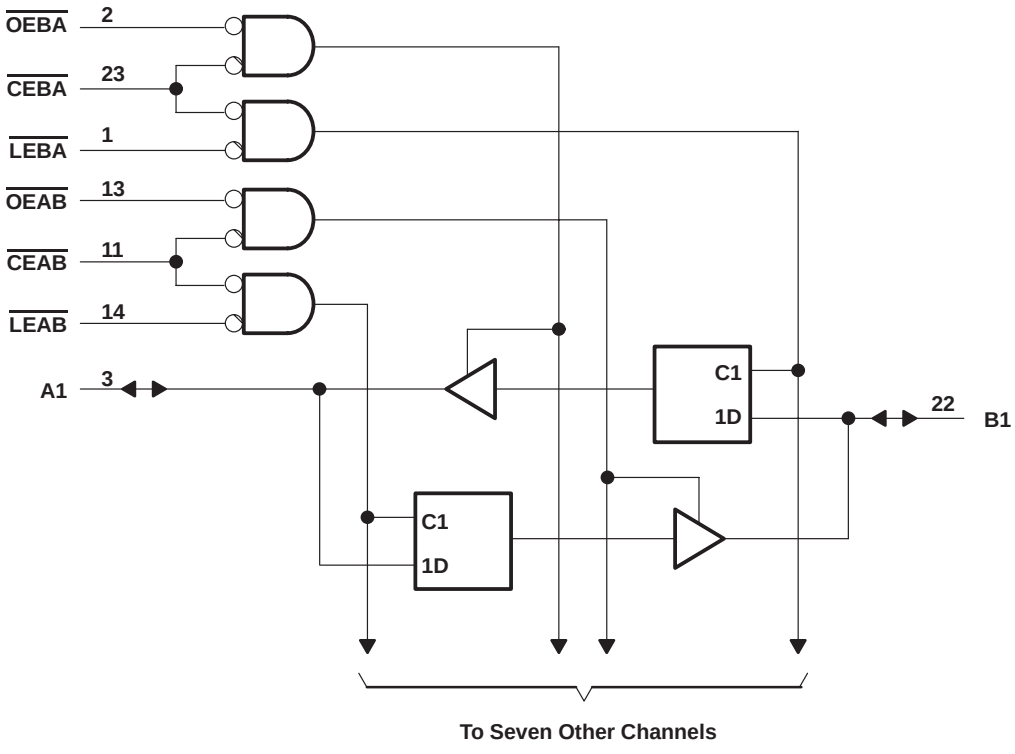
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air): DB package . . . . . 0.7 W
DW package . . . . . 1 W
NT package . . . . . 1.3 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP†	MAX			
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA		2					
		I_{OH} = –32 mA					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55			V
		I_{OL} = 64 mA						0.55	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND	Control inputs			±1		±1	µA
			A or B ports			±100		±100	
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50	µA
I_{OFF}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100		±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		1	250		250	µA
			Outputs low		24	34		34	mA
			Outputs disabled		0.5	250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		4				pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		7				pF

† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

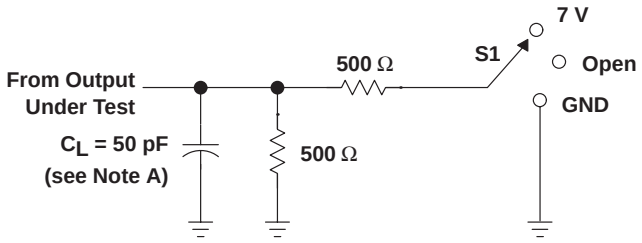
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			3.5		3.5		ns
t_{su}	Setup time	Data before LEAB or LEBA↑	High	2.5		2.5		ns
			Low	3		3		
		Data before CEAB or CEBA↑	High	2.5		2.5		
			Low	2.5		2.5		
t_h	Hold time	Data after $\overline{LEAB}$ or $\overline{LEBA}$↑		1		1		ns
		Data after $\overline{CEAB}$ or $\overline{CEBA}$↑		1		1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

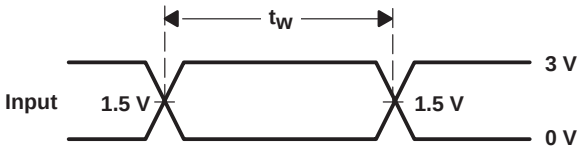
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.6	3.3	4.4	1.6	5	ns
t_{PHL}			1.6	4.1	5.1	1.6	6	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	1.6	3.9	5.1	1.6	6.2	ns
t_{PHL}			1.6	4.4	5.4	1.6	6.3	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	1.4	3.1	4.1	1.4	5	ns
t_{PZL}			2	3.9	4.9	2	5.7	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.5	4.2	5.8	2.5	6.7	ns
t_{PLZ}			2.5	4.8	6.1	2.5	7	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	1.4	3.4	4.4	1.4	5.4	ns
t_{PZL}			2	4.1	5.2	2	6.1	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.2	4.7	6.1	3.2	7	ns
t_{PLZ}			2.5	5	6.7	2.5	7.3	

PARAMETER MEASUREMENT INFORMATION

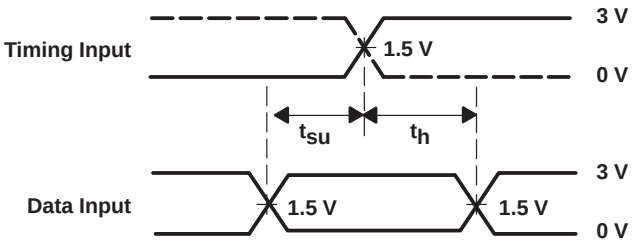


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

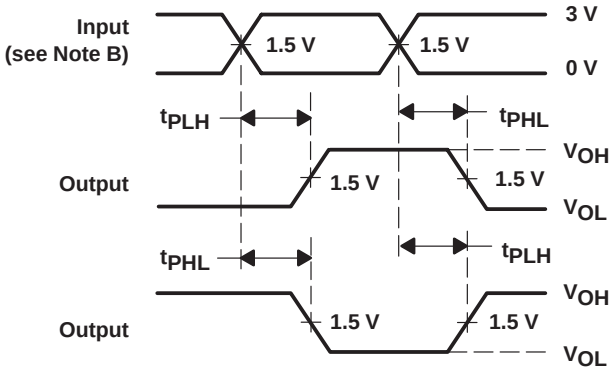
LOAD CIRCUIT FOR OUTPUTS



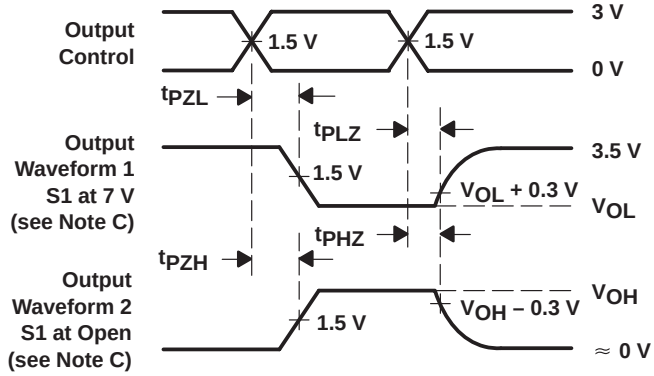
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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