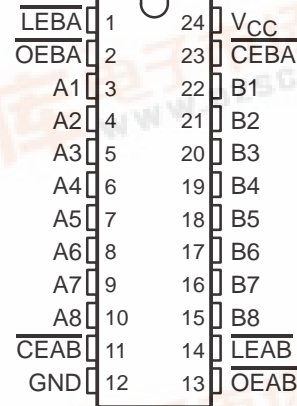


# SN74LVC543A OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)**  
< 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)**  
> 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE  
(TOP VIEW)



## description

This octal registered transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC543A contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ( $\overline{LEAB}$  or  $\overline{LEBA}$ ) and output-enable ( $\overline{OEAB}$  or  $\overline{OEBA}$ ) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ( $\overline{CEAB}$ ) input must be low to enter data from A or to output data from B. If  $\overline{CEAB}$  is low and  $\overline{LEAB}$  is low, the A-to-B latches are transparent; a subsequent low-to-high transition of  $\overline{LEAB}$  places the A latches in the storage mode. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow for B to A is similar to that of A to B, but uses  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC543A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

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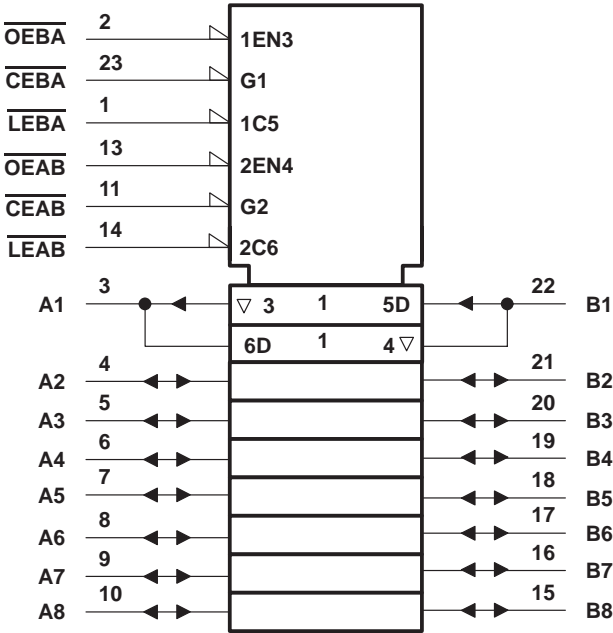
FUNCTION TABLE†

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B <sub>0</sub> ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$ , and  $\overline{\text{OEBA}}$ .

‡ Output level before the indicated steady-state input conditions were established

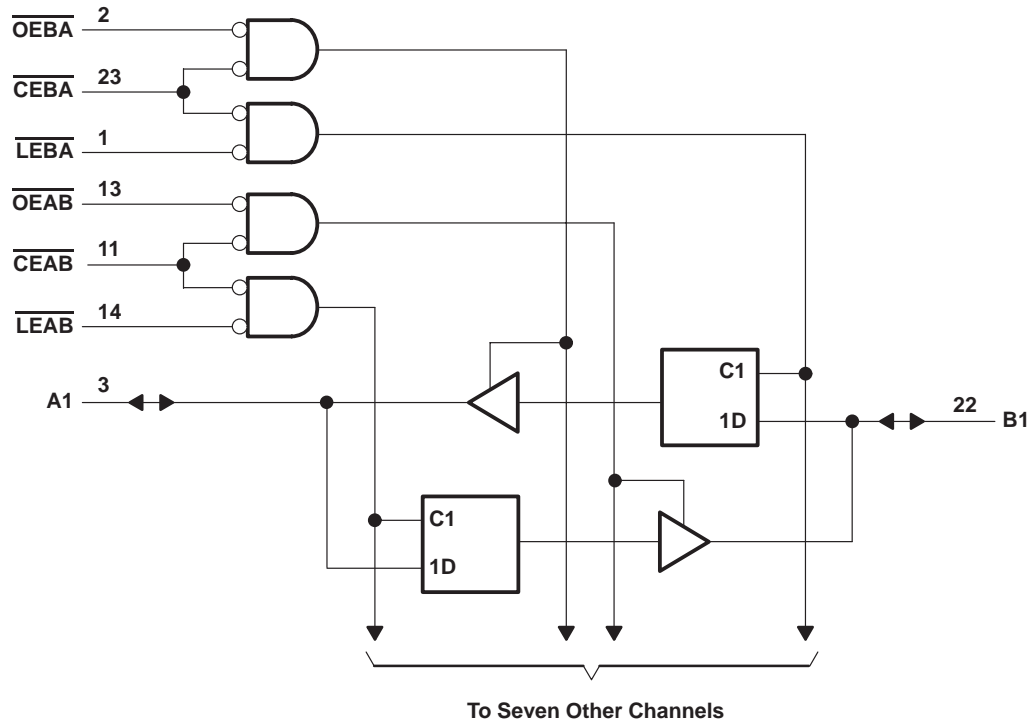
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 6.5 V
Input voltage range, $V_I$ : (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±50 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package	104°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

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#### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65×V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35×V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage	0	5.5	V	
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3 state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	−4		mA
		V <sub>CC</sub> = 2.3 V	−8		
		V <sub>CC</sub> = 2.7 V	−12		
		V <sub>CC</sub> = 3 V	−24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4		mA
		V <sub>CC</sub> = 2.3 V	8		
		V <sub>CC</sub> = 2.7 V	12		
		V <sub>CC</sub> = 3 V	24		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V	
T <sub>A</sub>	Operating free-air temperature	−40	85	°C	

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = –100 µA	1.65 V to 3.6 V	V <sub>CC</sub> –0.2			V
		I <sub>OH</sub> = –4 mA	1.65 V	1.2			
		I <sub>OH</sub> = –8 mA	2.3 V	1.7			
		I <sub>OH</sub> = –12 mA	2.7 V	2.2			
			3 V	2.4			
		I <sub>OH</sub> = –24 mA	3 V	2.2			
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V	0.2			V
		I <sub>OL</sub> = 4 mA	1.65 V	0.45			
		I <sub>OL</sub> = 8 mA	2.3 V	0.7			
		I <sub>OL</sub> = 12 mA	2.7 V	0.4			
		I <sub>OL</sub> = 24 mA	3 V	0.55			
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V	±5			µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	±10			µA
I <sub>OZ</sub> ‡		V <sub>O</sub> = 0 to 5.5 V	3.6 V	±10			µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	10			µA
		3.6 V ≤ V <sub>I</sub> ≤ 5.5 V§		10			
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500			µA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	4.5			pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7.5			pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

§ This applies in the disabled state only.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	¶		¶		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before $\overline{\text{LE}}\uparrow$ or $\overline{\text{CE}}\uparrow$	¶		¶		1.6		1.6		ns
t <sub>h</sub>	Hold time, data after $\overline{\text{LE}}\uparrow$ or $\overline{\text{CE}}\uparrow$	¶		¶		2.1		2.1		ns

¶ This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	B or A	†	†	†	†	8		1	7	ns
	$\overline{LE}$		†	†	†	†	9.5		1.2	8.5	
$t_{en}$	$\overline{OE}$	A or B	†	†	†	†	9.2		1.3	7.7	ns
	$\overline{CE}$		†	†	†	†	9.3		1.3	8	
$t_{dis}$	$\overline{OE}$	A or B	†	†	†	†	7.5		1	7	ns
	$\overline{CE}$		†	†	†	†	7.5		1	7	

† This information was not available at the time of publication.

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$	UNIT
				TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	$f = 10\text{ MHz}$	†	†	49	pF
		Outputs disabled		†	†	6	

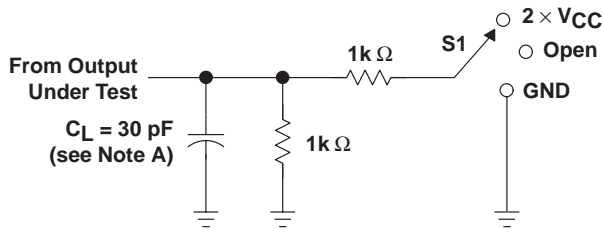
† This information was not available at the time of publication.

# SN74LVC543A OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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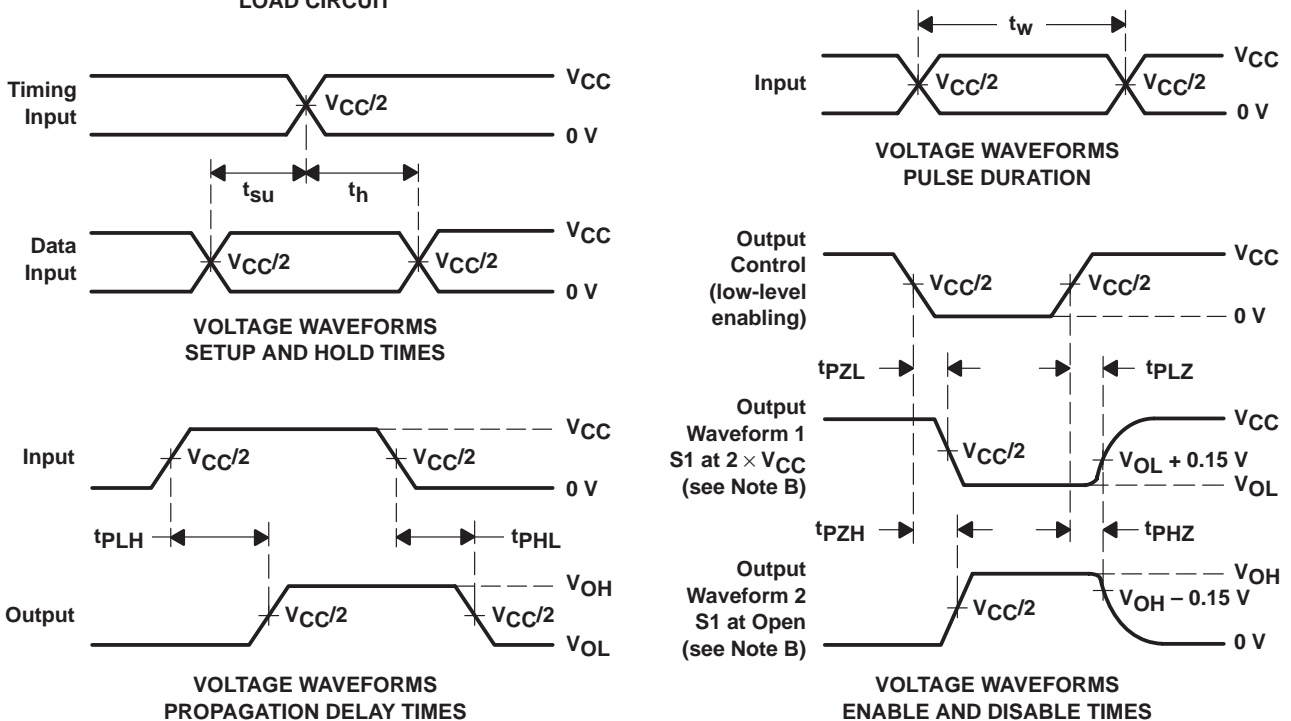
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

# SN74LVC543A

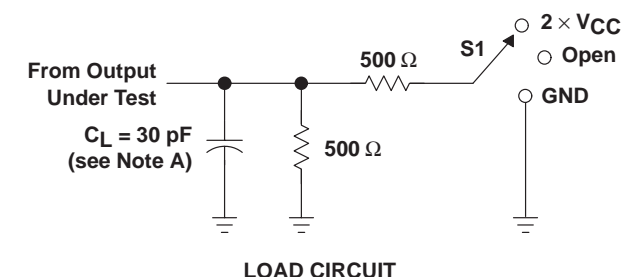
## OCTAL REGISTERED TRANSCEIVER

### WITH 3-STATE OUTPUTS

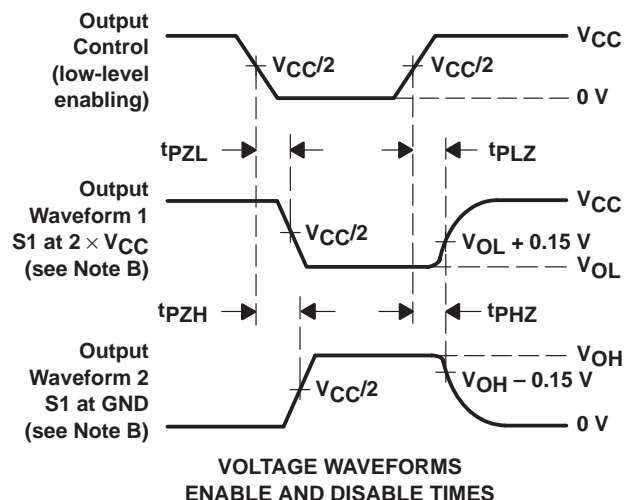
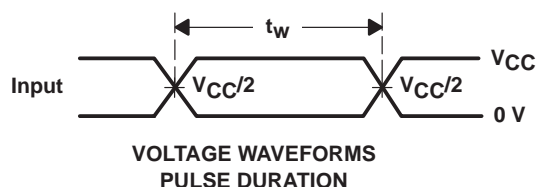
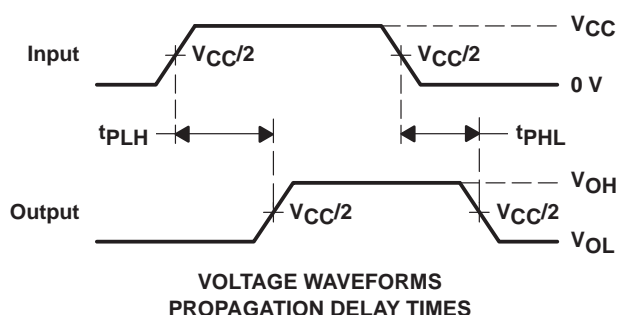
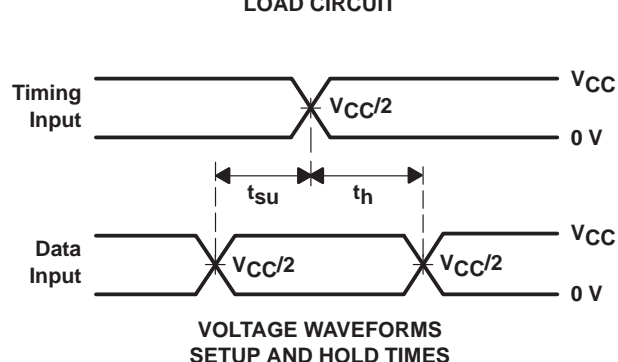
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#### PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

# SN74LVC543A

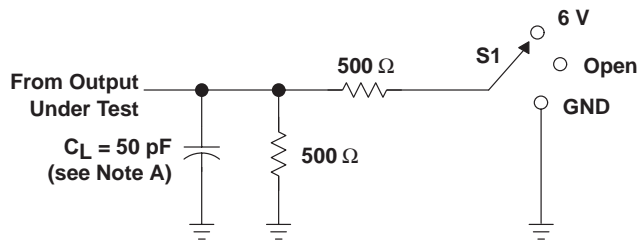
## OCTAL REGISTERED TRANSCEIVER

### WITH 3-STATE OUTPUTS

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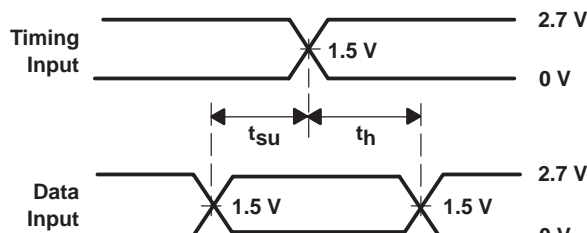
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

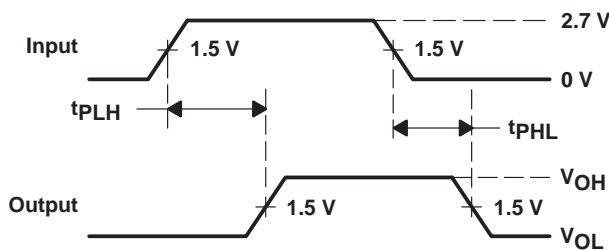


LOAD CIRCUIT

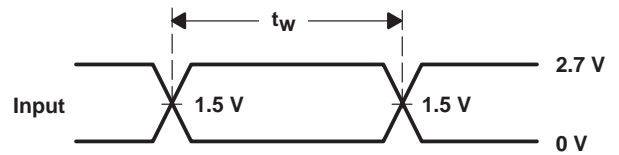
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



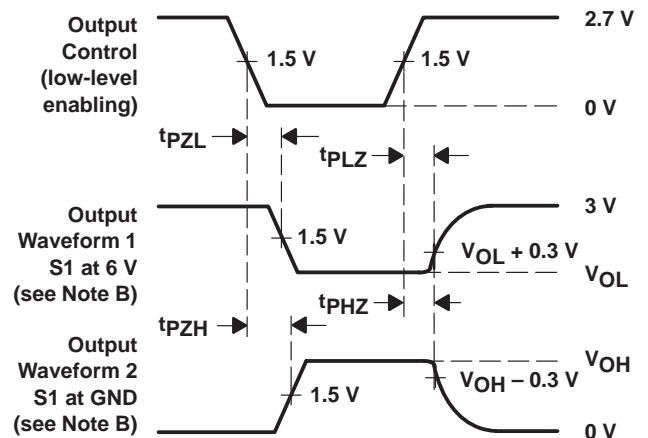
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

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