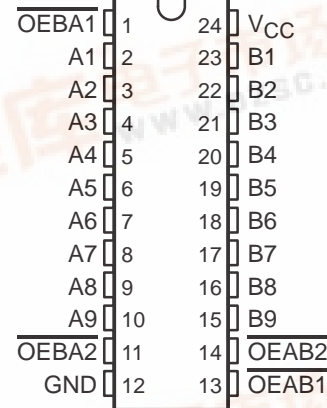


# SN74LVC863A

## 9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200\text{ pF}$ ,  $R = 0$ )
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE  
(TOP VIEW)

### description

This 9-bit bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC863A is designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ) inputs.

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC863A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

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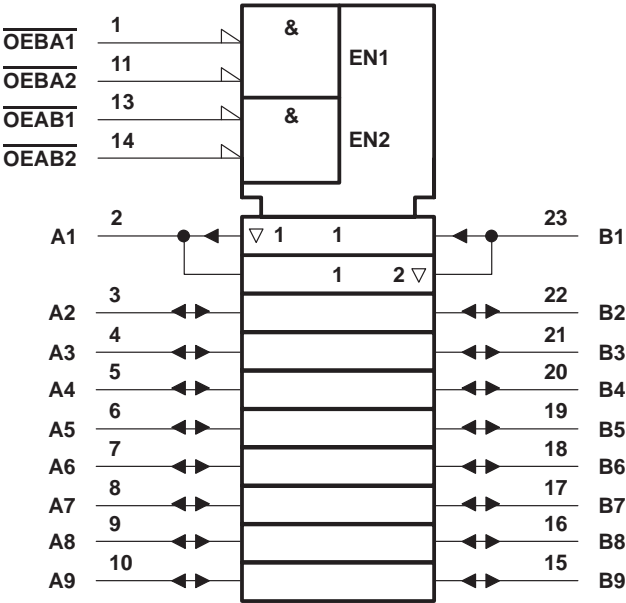
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9-BIT BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS				OPERATION
OEAB1	OEAB2	OEBA1	OEBA2	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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Logic diagram of a 2-to-4 decoder circuit. The circuit uses two 2-input AND gates and two inverters. The inputs are OEBA1 (pin 1), OEBA2 (pin 11), OEAB1 (pin 13), and OEAB2 (pin 14). The outputs are A1 (pin 2) and B1 (pin 23). The circuit is part of a larger system with eight other channels.

NOTES:

1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

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## 9-BIT BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage	0	5.5		V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3 state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		−4	mA
		V <sub>CC</sub> = 2.3 V		−8	
		V <sub>CC</sub> = 2.7 V		−12	
		V <sub>CC</sub> = 3 V		−24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 2.7 V		12	
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate	0	10		ns/V
T <sub>A</sub>	Operating free-air temperature	−40	85		°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**9-BIT BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT	
V <sub>OH</sub>		I <sub>OH</sub> = −100 μA	1.65 V to 3.6 V	V <sub>CC</sub> −0.2			V	
		I <sub>OH</sub> = −4 mA	1.65 V	1.2				
		I <sub>OH</sub> = −8 mA	2.3 V	1.7				
		I <sub>OH</sub> = −12 mA	2.7 V	2.2				
			3 V	2.4				
		I <sub>OH</sub> = −24 mA	3 V	2.2				
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V	
		I <sub>OL</sub> = 4 mA	1.65 V			0.45		
		I <sub>OL</sub> = 8 mA	2.3 V			0.7		
		I <sub>OL</sub> = 12 mA	2.7 V			0.4		
		I <sub>OL</sub> = 24 mA	3 V			0.55		
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	μA	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μA	
I <sub>OZ</sub> ‡		V <sub>O</sub> = 0 to 5.5 V		3.6 V			±10	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			10	μA	
		3.6 V ≤ V <sub>I</sub> ≤ 5.5 V§				10		
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		2.7 V to 3.6 V		500	μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		5	pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		7	pF	

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

§ This applies in the disabled state only.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	¶	¶	¶	¶	6.8		1.7	6.1	ns
t <sub>en</sub>	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	A or B	¶	¶	¶	¶	8.3		1.2	7.2	ns
t <sub>dis</sub>	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	A or B	¶	¶	¶	¶	7		2	6.3	ns

¶ This information was not available at the time of publication.

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	V <sub>CC</sub> = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	¶	¶	27	pF
		Outputs disabled		¶	¶	5	

¶ This information was not available at the time of publication.

# SN74LVC863A

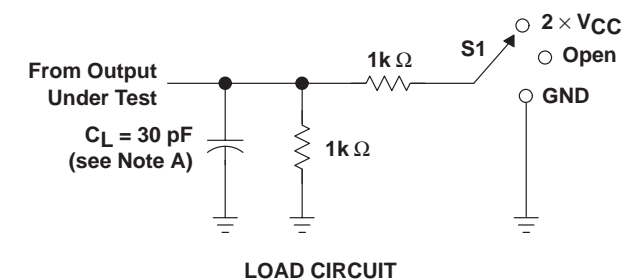
## 9-BIT BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

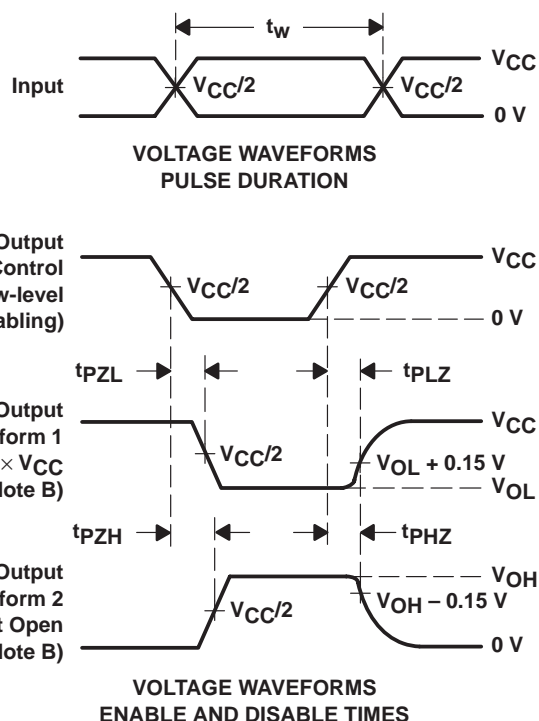
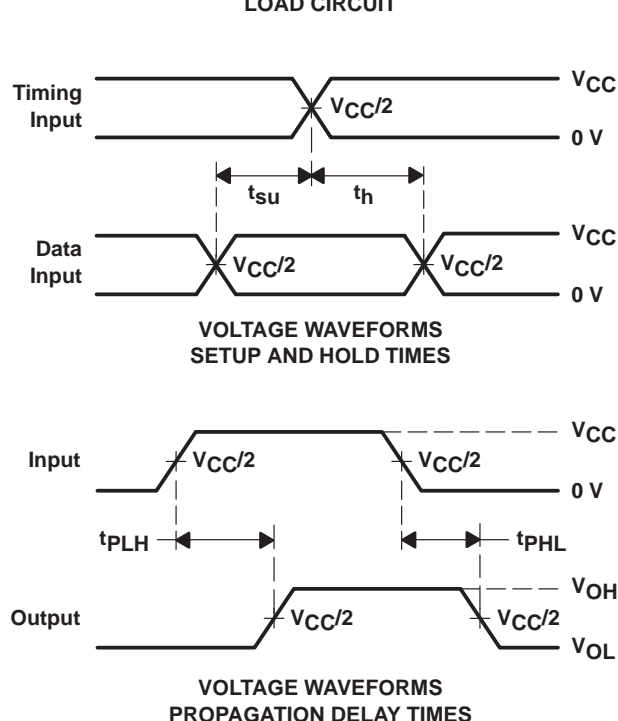
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#### PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

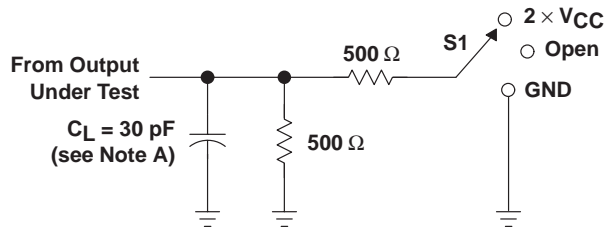
Figure 1. Load Circuit and Voltage Waveforms

# SN74LVC863A 9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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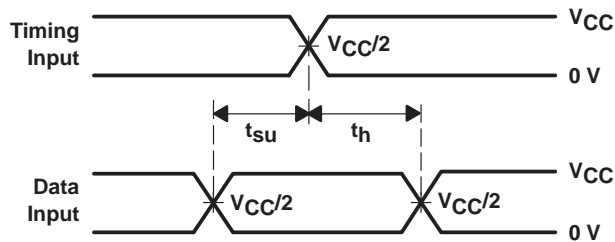
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

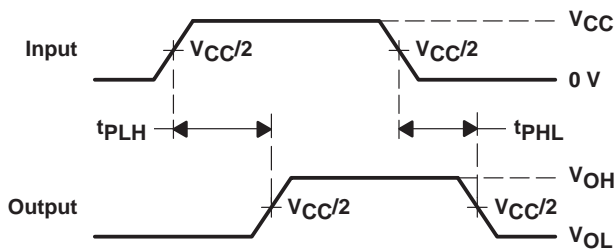


LOAD CIRCUIT

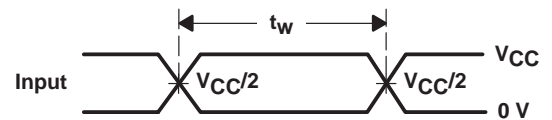
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PHZ}$	GND



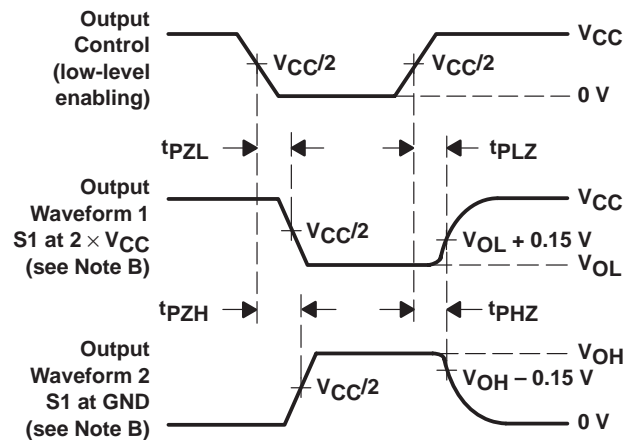
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

# SN74LVC863A

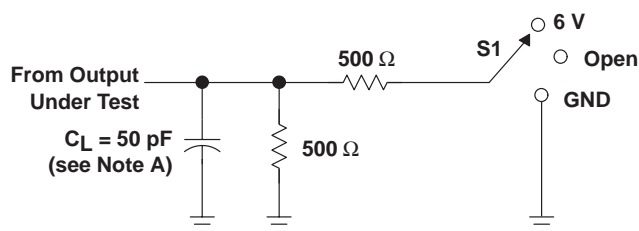
## 9-BIT BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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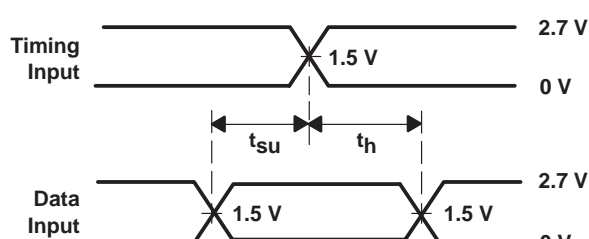
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V} \pm 0.3 \text{ V}$

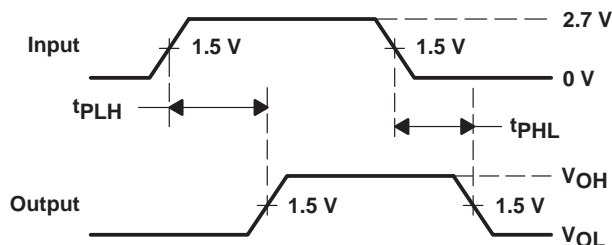


LOAD CIRCUIT

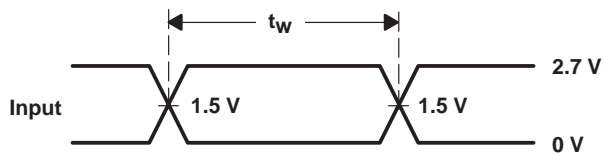
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



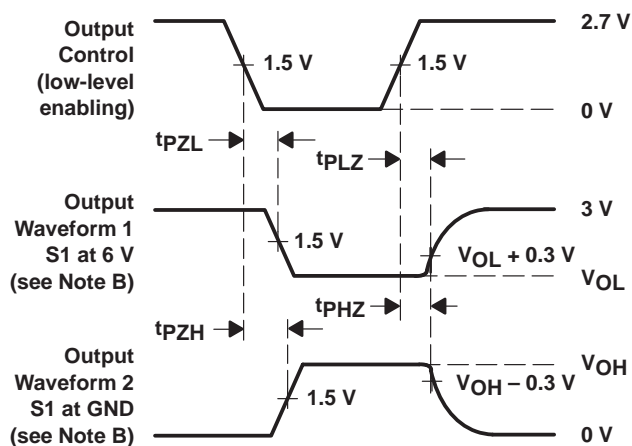
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

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  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms



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