

# SN54ALS563A, SN74ALS563B OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS163 – D2661, DECEMBER 1982 – REVISED JANUARY 1989

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus Structured Pinout**
- **Package Options include Plastic Small Outline Package, Ceramic Chip Carriers and Standard Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

## description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

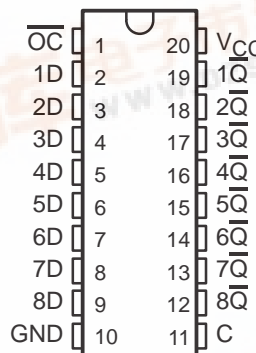
The eight latches are transparent D-type latches. While the enable (C) is high the Q outputs will follow the complements of data (D) inputs. When the enable is taken low the output will be latched at the inverses of the levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

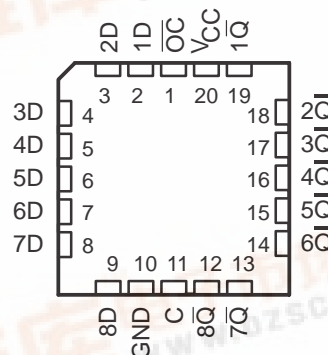
The output control (OC) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS563A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS563B is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS563A . . . J PACKAGE  
SN74ALS563B . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS563A . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each latch)

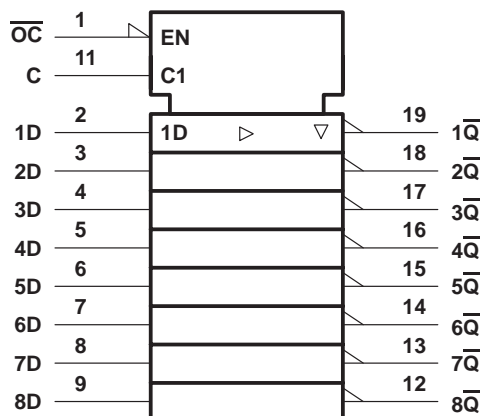
INPUTS			OUTPUT Q
OC	ENABLE C	D	
L	H	H	L
L	H	H	H
L	L	X	Q <sub>0</sub>
H	X	X	Z

# SN54ALS563A, SN74ALS563B

## OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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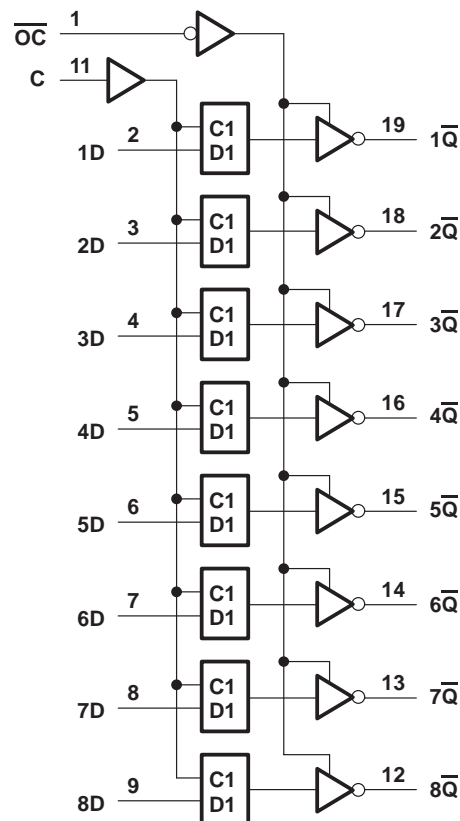
### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range: SN54ALS563A	–55°C to 125°C
SN74ALS563B	0°C to 70°C
Storage temperature range	–65°C to 150°C

### recommended operating conditions

		SN54ALS563A			SN74ALS563B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–1			–2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$t_w$	Pulse duration, C high	15			15			ns
$t_{su}$	Setup time, data before C↓	10			10			ns
$t_h$	Hold time, data after C↓	10			10			ns
$T_A$	Operating free-air temperature	–55		125	0		70	°C

# SN54ALS563A, SN74ALS563B

## OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS563A			SN74ALS563B			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = -1\text{ mA}$	2.4	3.3					
	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -2.6\text{ mA}$				2.4	3.2		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 12\text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 24\text{ mA}$					0.35	0.5	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			20			20	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.4\text{ V}$			-20			-20	$\mu\text{A}$
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			-0.1			-0.1	mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-30		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high		10	17	10		17
		Outputs low		16	26	16		26
		Outputs disabled		17	29	17		29

† All typical Values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

### switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = 25°C	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§				UNIT
			'ALS563	SN54ALS563A		SN74ALS563B		
			TYP	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Q	10	3	21	3	18	ns
t <sub>PHL</sub>			8	3	15	3	14	
t <sub>PLH</sub>	C	Q	8	8	29	6	22	ns
t <sub>PHL</sub>			14	8	22	6	21	
t <sub>PZH</sub>	OC	Q	8	4	21	3	18	ns
t <sub>PZL</sub>			10	4	21	4	18	
t <sub>PHZ</sub>	OC	Q	5	2	12	1	10	ns
t <sub>PLZ</sub>			7	3	18	1	15	

§ For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of the *ALS/AS Logic Data Book*, 1986.

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