

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC193AP, TC74HC193AF, TC74HC193AFN

SYNCHRONOUS UP/DOWN BINARY COUNTER

The TC74HC193A are high speed CMOS SYNCHRONOUS 4-BIT UP/DOWN COUNTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

They have a clear input (CLR), a load input ($\overline{LOAD}$), load data inputs (A ~ D), two clock inputs (COUNT UP, COUNT DOWN), four count data outputs (QA ~ QD), and other outputs ($\overline{CARRY}$, $\overline{BORROW}$).

CLEAR is active high and forces QA thru QD outputs low independent of the other inputs.

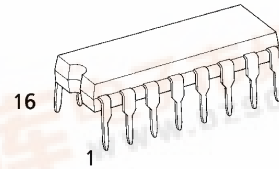
$\overline{CARRY}$ and $\overline{BORROW}$ outputs are provided in order to make a cascade connection without external circuitry.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

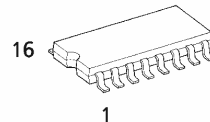
FEATURES:

- High Speed..... $f_{MAX} = 54\text{MHz}$ (typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}$ (Min.)
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range... V_{CC} (opr.) = $2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS193

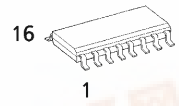
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

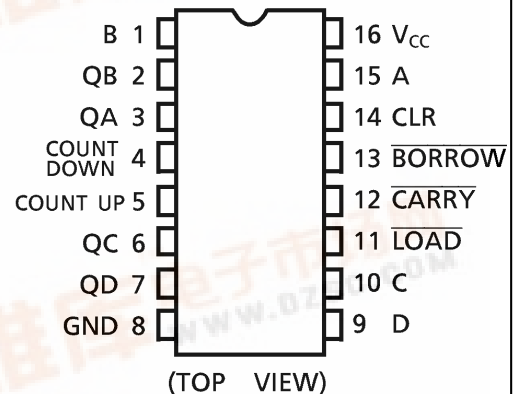


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

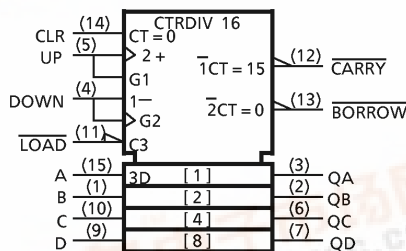


FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

PIN ASSIGNMENT



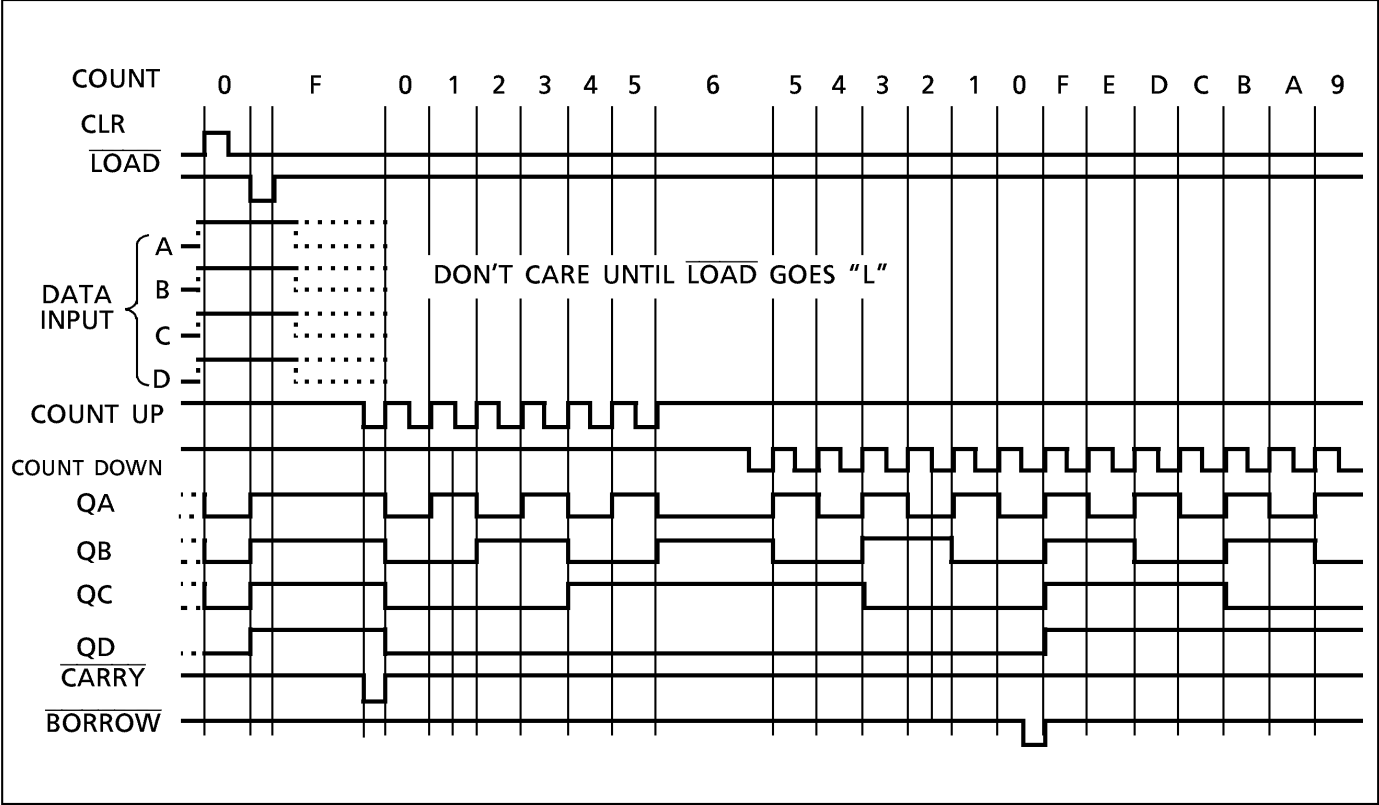
IEC LOGIC SYMBOL



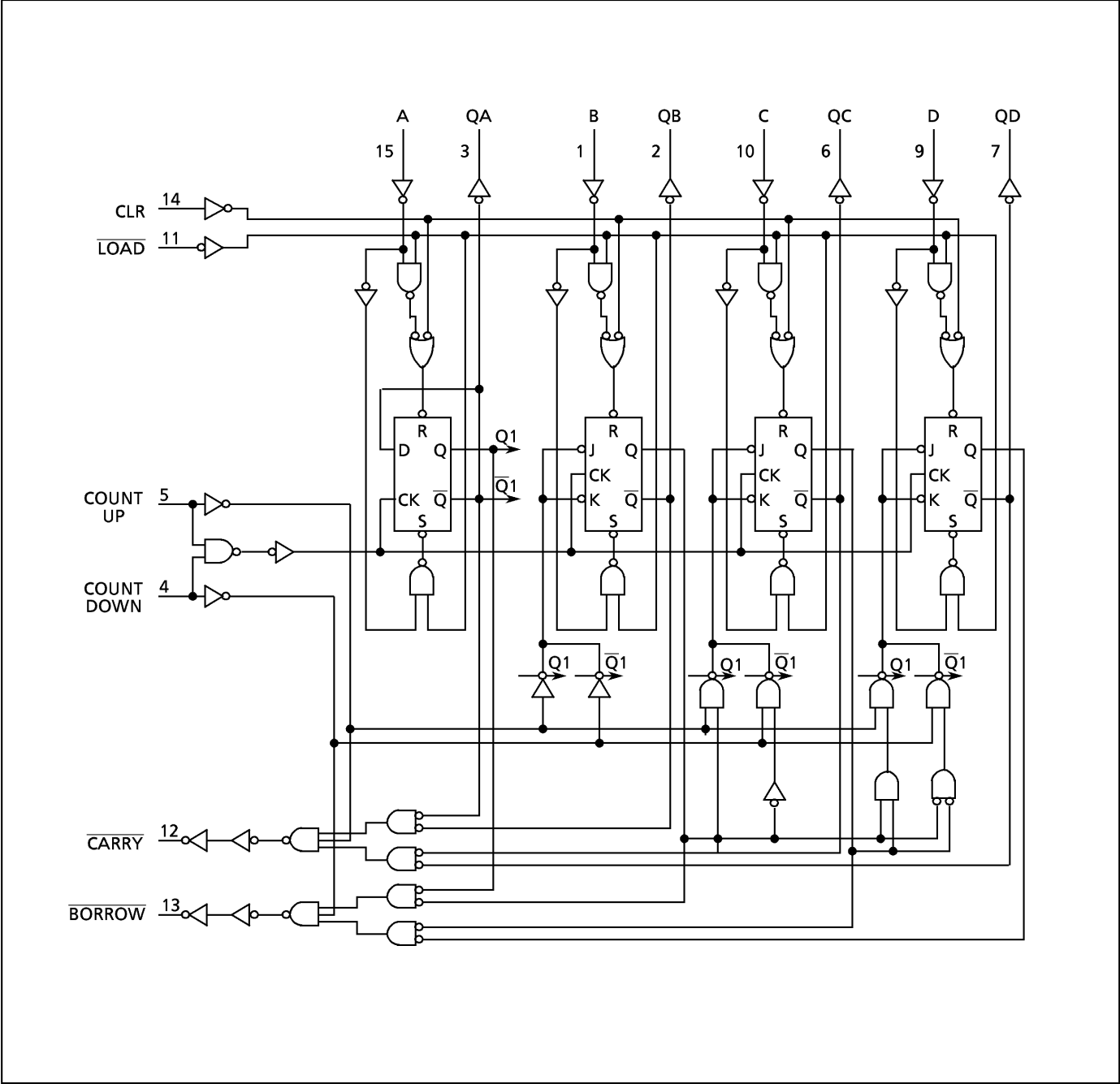
TRUTH TABLE

INPUTS				FUNCTION
COUNT UP	COUNT DOWN	$\overline{LOAD}$	CLR	
	H	H	L	COUNT UP
	H	H	L	NO COUNT
H		H	L	COUNT DOWN
H		H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
			4.5 6.0	— —	— —	— —	— —	— —	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
			4.5 6.0	— —	— —	— —	— —	— —	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$		$T_a = -40 \sim 85^\circ\text{C}$	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Pulse Width (LOAD)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time (CLR)	$t_{W(H)}$		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Set-up Time (DATA — LOAD)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time (DATA — LOAD)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time (LOAD)	t_{rem}		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	10	
Minimum Removal Time (CLR)	t_{rem}		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	10	
Clock Frequency	f		2.0	—	5	4	MHz
			4.5	—	25	20	
			6.0	—	29	24	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	6	12	ns
Propagation Delay Time (UP, DOWN—Q)	t_{PLH} t_{PHL}		—	16	33	
Propagation Delay Time (UP— $\overline{\text{CARRY}}$)	t_{PLH} t_{PHL}		—	10	22	
Propagation Delay Time (DOWN— $\overline{\text{BORROW}}$)	t_{PLH} t_{PHL}		—	10	22	
Propagation Delay Time ($\overline{\text{LOAD}}$ —Q)	t_{PLH} t_{PHL}		—	21	38	
Propagation Delay Time ($\overline{\text{LOAD}}$ — $\overline{\text{CARRY}}$)	t_{PLH} t_{PHL}		—	25	44	
Propagation Delay Time ($\overline{\text{LOAD}}$ — $\overline{\text{BORROW}}$)	t_{PLH} t_{PHL}		—	26	44	
Propagation Delay Time (DATA IN—Q)	t_{PLH} t_{PHL}		—	21	33	
Propagation Delay Time (DATA IN— $\overline{\text{CARRY}}$)	t_{PLH} t_{PHL}		—	29	44	
Propagation Delay Time (DATA IN— $\overline{\text{BORROW}}$)	t_{PLH} t_{PHL}		—	26	44	
Propagation Delay Time (CLR—Q)	t_{PHL}		—	25	39	
Propagation Delay Time (CLR— $\overline{\text{CARRY}}$)	t_{PLH}		—	30	44	
Propagation Delay Time (CLR— $\overline{\text{BORROW}}$)	t_{PHL}		—	30	44	
Maximum Clock Frequency	f_{MAX}		27	52	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation Delay Time (UP, DOWN—Q)	t_{pLH} t_{pHL}		2.0	—	65	190	—	240
			4.5	—	20	38	—	48
			6.0	—	16	32	—	41
Propagation Delay Time (UP—CARRY)	t_{pLH} t_{pHL}		2.0	—	40	130	—	165
			4.5	—	13	26	—	33
			6.0	—	11	22	—	28
Propagation Delay Time (DOWN—BORROW)	t_{pLH} t_{pHL}		2.0	—	40	130	—	165
			4.5	—	13	26	—	33
			6.0	—	11	22	—	28
Propagation Delay Time (LOAD—Q)	t_{pLH} t_{pHL}		2.0	—	85	220	—	275
			4.5	—	25	44	—	55
			6.0	—	20	37	—	47
Propagation Delay Time (LOAD—CARRY)	t_{pLH} t_{pHL}		2.0	—	110	250	—	315
			4.5	—	30	50	—	63
			6.0	—	25	43	—	54
Propagation Delay Time (LOAD—BORROW)	t_{pLH} t_{pHL}		2.0	—	110	250	—	315
			4.5	—	30	50	—	63
			6.0	—	25	43	—	54
Propagation Delay Time (DATA IN—Q)	t_{pLH} t_{pHL}		2.0	—	80	190	—	240
			4.5	—	25	38	—	48
			6.0	—	20	32	—	41
Propagation Delay Time (DATA IN—CARRY)	t_{pLH} t_{pHL}		2.0	—	120	250	—	315
			4.5	—	34	50	—	63
			6.0	—	28	43	—	54
Propagation Delay Time (DATA IN—BORROW)	t_{pLH} t_{pHL}		2.0	—	110	250	—	315
			4.5	—	31	50	—	63
			6.0	—	25	43	—	54
Propagation Delay Time (CLR—Q)	t_{pHL}		2.0	—	100	225	—	280
			4.5	—	30	45	—	56
			6.0	—	25	38	—	48
Propagation Delay Time (CLR—CARRY)	t_{pLH}		2.0	—	120	250	—	315
			4.5	—	35	50	—	63
			6.0	—	29	43	—	54
Propagation Delay Time (CLR—BORROW)	t_{pHL}		2.0	—	120	250	—	315
			4.5	—	35	50	—	63
			6.0	—	29	43	—	54
Maximum Clock Frequency	f_{MAX}		2.0	5	12	—	4	—
			4.5	25	48	—	20	—
			6.0	29	55	—	24	—
Input Capacitance	C_{IN}			—	5	10	—	10
Power Dissipation Capacitance	$C_{PD} (1)$			—	67	—	—	—

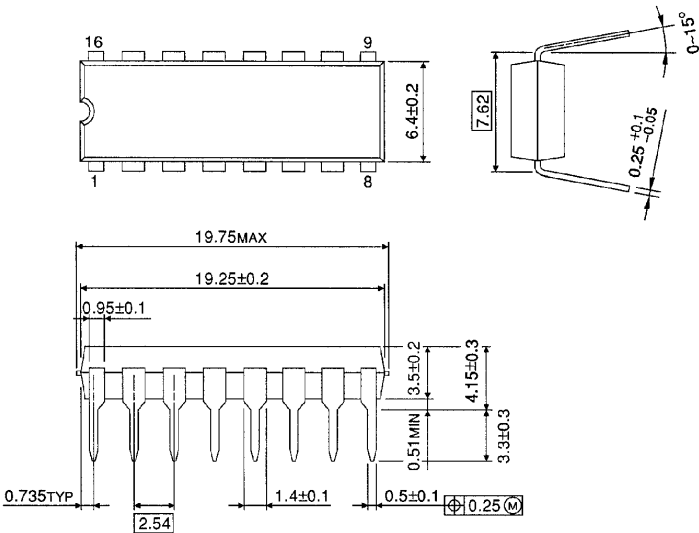
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC} (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

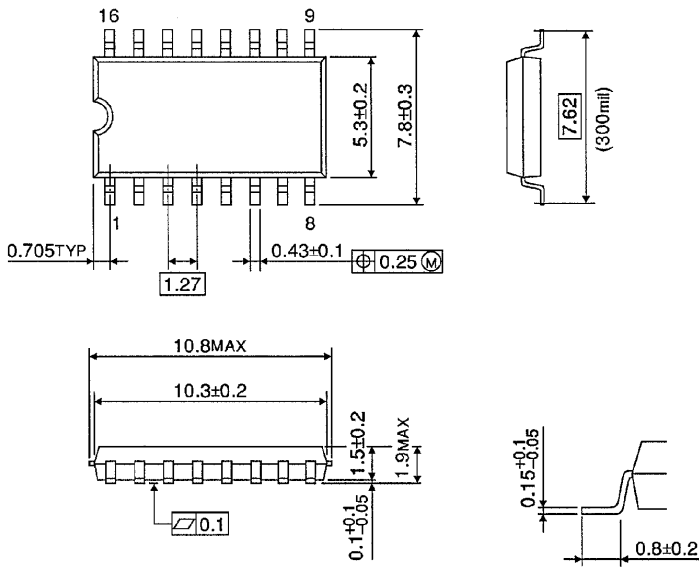
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

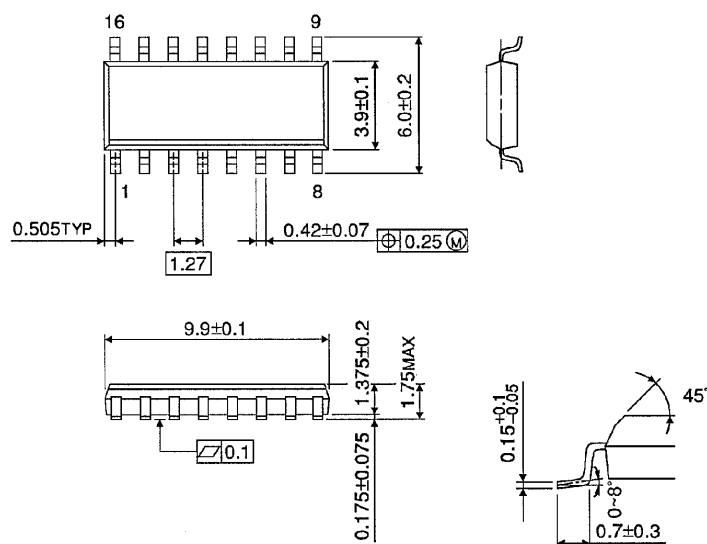


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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