

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC273AP, TC74HC273AF, TC74HC273AFW

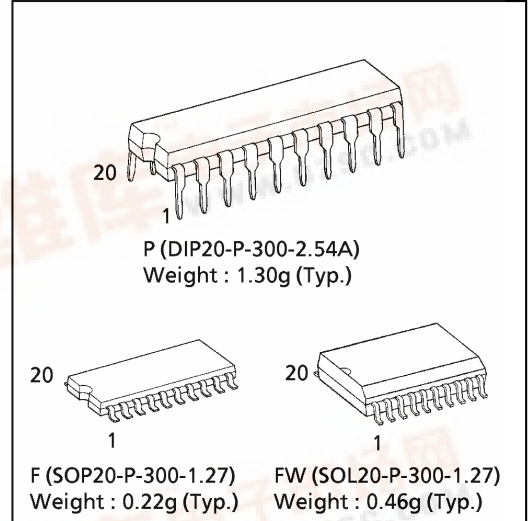
OCTAL D-TYPE FLIP FLOP WITH CLEAR

(Note) The JEDEC SOP (FW) is not available in Japan.

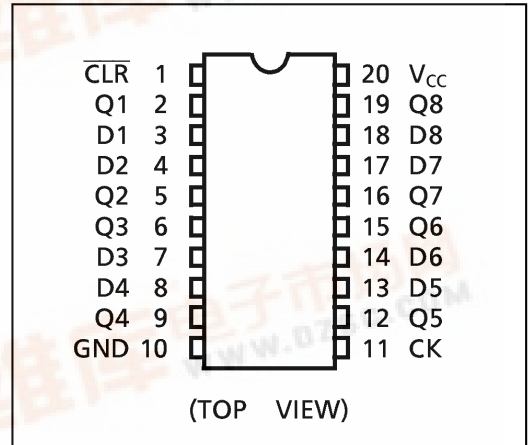
The TC74HC273A is a high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse. When the $\overline{\text{CLR}}$ input is held "L", the Q outputs are at a low logic level independent of the other inputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $f_{\text{MAX}} = 67\text{MHz}(\text{typ.})$
at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}} (\text{Min.})$
- Output Drive Capability 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{\text{OH}}| = I_{\text{OL}} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS273



PIN ASSIGNMENT

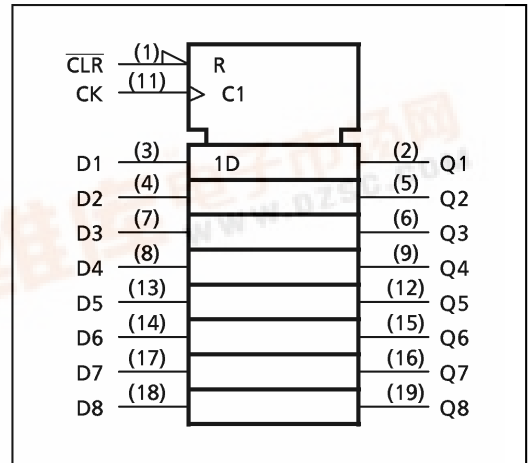


TRUTH TABLE

| INPUTS | | | OUTPUTS | FUNCTION |
|-------------------------|---|--------------|---------|-----------|
| $\overline{\text{CLR}}$ | D | CK | Q | |
| L | X | X | L | CLEAR |
| H | L | \uparrow | L | — |
| H | H | \uparrow | H | — |
| H | X | \downarrow | Q_n | No change |

X : Don't Care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|-----------------------------|-----------|------------------------|------|
| Supply Voltage Range | V_{CC} | -0.5~7 | V |
| DC Input Voltage | V_{IN} | -0.5~ $V_{CC} + 0.5$ | V |
| DC Output Voltage | V_{OUT} | -0.5~ $V_{CC} + 0.5$ | V |
| Input Diode Current | I_{IK} | ± 20 | mA |
| Output Diode Current | I_{OK} | ± 20 | mA |
| DC Output Current | I_{OUT} | ± 25 | mA |
| DC V_{CC} /Ground Current | I_{CC} | ± 50 | mA |
| Power Dissipation | P_D | 500 (DIP)* / 180 (SOP) | mW |
| Storage Temperature | T_{stg} | -65~150 | °C |

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | VALUE | UNIT |
|--------------------------|------------|--|------|
| Supply Voltage | V_{CC} | 2~6 | V |
| Input Voltage | V_{IN} | 0~ V_{CC} | V |
| Output Voltage | V_{OUT} | 0~ V_{CC} | V |
| Operating Temperature | T_{opr} | -40~85 | °C |
| Input Rise and Fall Time | t_r, t_f | 0~ 1000 ($V_{CC} = 2.0\text{V}$) 0~ 500 ($V_{CC} = 4.5\text{V}$) 0~ 400 ($V_{CC} = 6.0\text{V}$) | ns |

DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | V_{CC} (V) | $T_a = 25^{\circ}\text{C}$ | | | $T_a = -40 \sim 85^{\circ}\text{C}$ | | UNIT | |
|-----------------------------|----------|--|--|----------------------------|------|-------|-------------------------------------|-------|---------------|---|
| | | | | MIN. | TYP. | MAX. | MIN. | MAX. | | |
| High - Level Input Voltage | V_{IH} | | 2.0 | 1.50 | — | — | 1.50 | — | V | |
| | | | 4.5 | 3.15 | — | — | 3.15 | — | | |
| | | | 6.0 | 4.20 | — | — | 4.20 | — | | |
| Low - Level Input Voltage | V_{IL} | | 2.0 | — | — | 0.50 | — | 0.50 | V | |
| | | | 4.5 | — | — | 1.35 | — | 1.35 | | |
| | | | 6.0 | — | — | 1.80 | — | 1.80 | | |
| High - Level Output Voltage | V_{OH} | $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -20\mu\text{A}$ | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | $I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$ | 4.5 | 4.18 | 4.31 | — | 4.13 | — | |
| | | | | 6.0 | 5.68 | 5.80 | — | 5.63 | — | |
| Low - Level Output Voltage | V_{OL} | $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 20\mu\text{A}$ | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL} = 4 \text{ mA}$ $I_{OL} = 5.2 \text{ mA}$ | 4.5 | — | 0.17 | 0.26 | — | 0.33 | |
| | | | | 6.0 | — | 0.18 | 0.26 | — | 0.33 | |
| Input Leakage Current | I_{IN} | $V_{IN} = V_{CC} \text{ or } \text{GND}$ | 6.0 | — | — | ± 0.1 | — | ± 1.0 | μA | |
| Quiescent Supply Current | I_{CC} | $V_{IN} = V_{CC} \text{ or } \text{GND}$ | 6.0 | — | — | 4.0 | — | 40.0 | | |

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

| PARAMETER | SYMBOL | TEST CONDITION | V _{CC} (V) | Ta = 25°C | | Ta = -40~85°C | UNIT |
|--|--------------------------|----------------|---------------------|-----------|-------|---------------|------|
| | | | | TYP. | LIMIT | LIMIT | |
| Minimum Pulse Width (CK) | $t_{W(L)}$ $t_{W(H)}$ | | 2.0 | — | 75 | 95 | ns |
| | | | 4.5 | — | 15 | 19 | |
| | | | 6.0 | — | 13 | 16 | |
| Minimum Pulse Width (\overline{CLR}) | $t_{W(L)}$ | | 2.0 | — | 75 | 95 | |
| | | | 4.5 | — | 15 | 19 | |
| | | | 6.0 | — | 13 | 16 | |
| Minimum Set-up Time | t_s | | 2.0 | — | 75 | 95 | |
| | | | 4.5 | — | 15 | 19 | |
| | | | 6.0 | — | 13 | 16 | |
| Minimum Hold Time | t_h | | 2.0 | — | 0 | 0 | |
| | | | 4.5 | — | 0 | 0 | |
| | | | 6.0 | — | 0 | 0 | |
| Minimum Removal Time (\overline{CLR}) | t_{rem} | | 2.0 | — | 50 | 65 | |
| | | | 4.5 | — | 10 | 13 | |
| | | | 6.0 | — | 9 | 11 | |
| Clock Frequency | f | | 2.0 | — | 6 | 5 | MHz |
| | | | 4.5 | — | 30 | 24 | |
| | | | 6.0 | — | 35 | 28 | |

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f = 6ns$)

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--|------------------------|----------------|------|------|------|------|
| Output Transition Time | t_{TLH} t_{THL} | | — | 4 | 8 | ns |
| Propagation Delay Time (CK-Q) | t_{pLH} t_{pHL} | | — | 15 | 25 | |
| Propagation Delay Time (\overline{CLR} -Q) | t_{pLH} t_{pHL} | | — | 16 | 27 | |
| Maximum Clock Frequency | f_{MAX} | | 40 | 67 | — | MHz |

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f = 6ns$)

| PARAMETER | SYMBOL | TEST CONDITION | V _{CC} (V) | Ta = 25°C | | | Ta = -40~85°C | | UNIT |
|--|------------------------|----------------|---------------------|-----------|------|------|---------------|------|------|
| | | | | MIN. | TYP. | MAX. | MIN. | MAX. | |
| Output Transition Time | t_{TLH} t_{THL} | | 2.0 | — | 25 | 75 | — | 95 | ns |
| | | | 4.5 | — | 7 | 15 | — | 19 | |
| | | | 6.0 | — | 6 | 13 | — | 16 | |
| Propagation Delay Time (CK-Q) | t_{pLH} t_{pHL} | | 2.0 | — | 54 | 145 | — | 180 | |
| | | | 4.5 | — | 18 | 29 | — | 36 | |
| | | | 6.0 | — | 15 | 25 | — | 31 | |
| Propagation Delay Time (\overline{CLR} -Q) | t_{pLH} t_{pHL} | | 2.0 | — | 60 | 160 | — | 200 | |
| | | | 4.5 | — | 20 | 32 | — | 40 | |
| | | | 6.0 | — | 17 | 27 | — | 34 | |
| Maximum Clock Frequency | f_{MAX} | | 2.0 | 6 | 18 | — | 5 | — | |
| | | | 4.5 | 30 | 56 | — | 24 | — | |
| | | | 6.0 | 35 | 66 | — | 28 | — | |
| Input Capacitance | C _{IN} | | | — | 5 | 10 | — | 10 | pF |
| Power Dissipation Capacitance | C _{PD} (1) | | | — | 43 | — | — | — | |

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

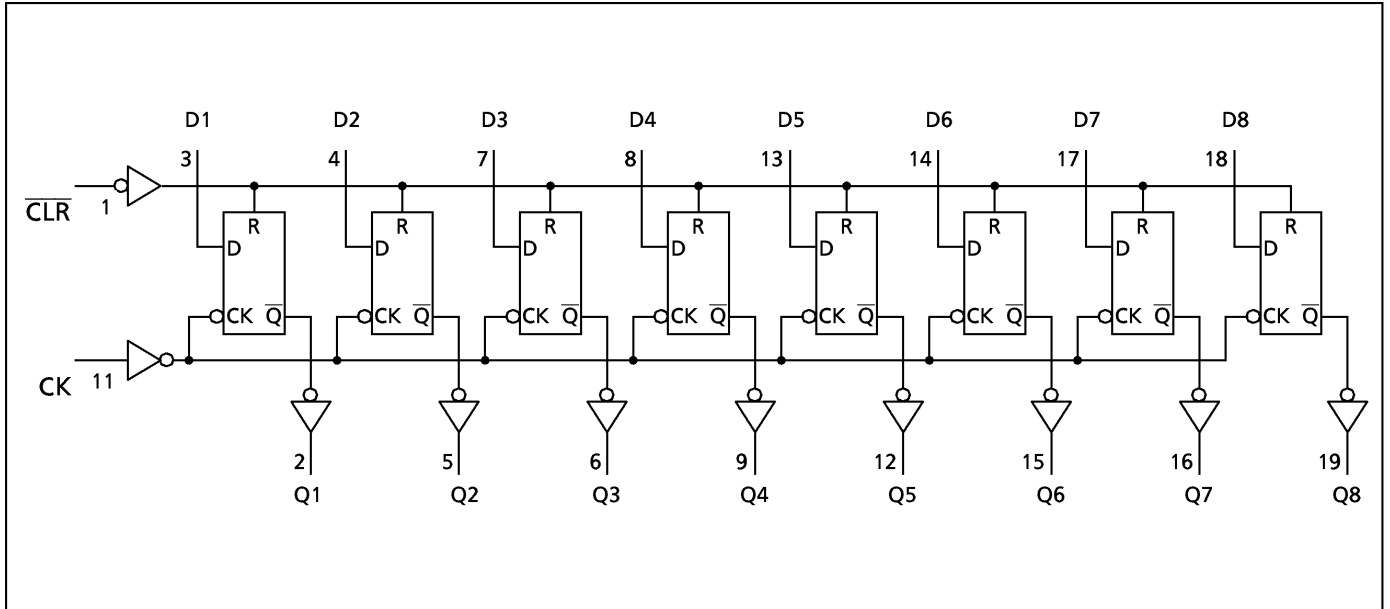
Average operating current can be obtained by the equation :

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per Flip Flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation :

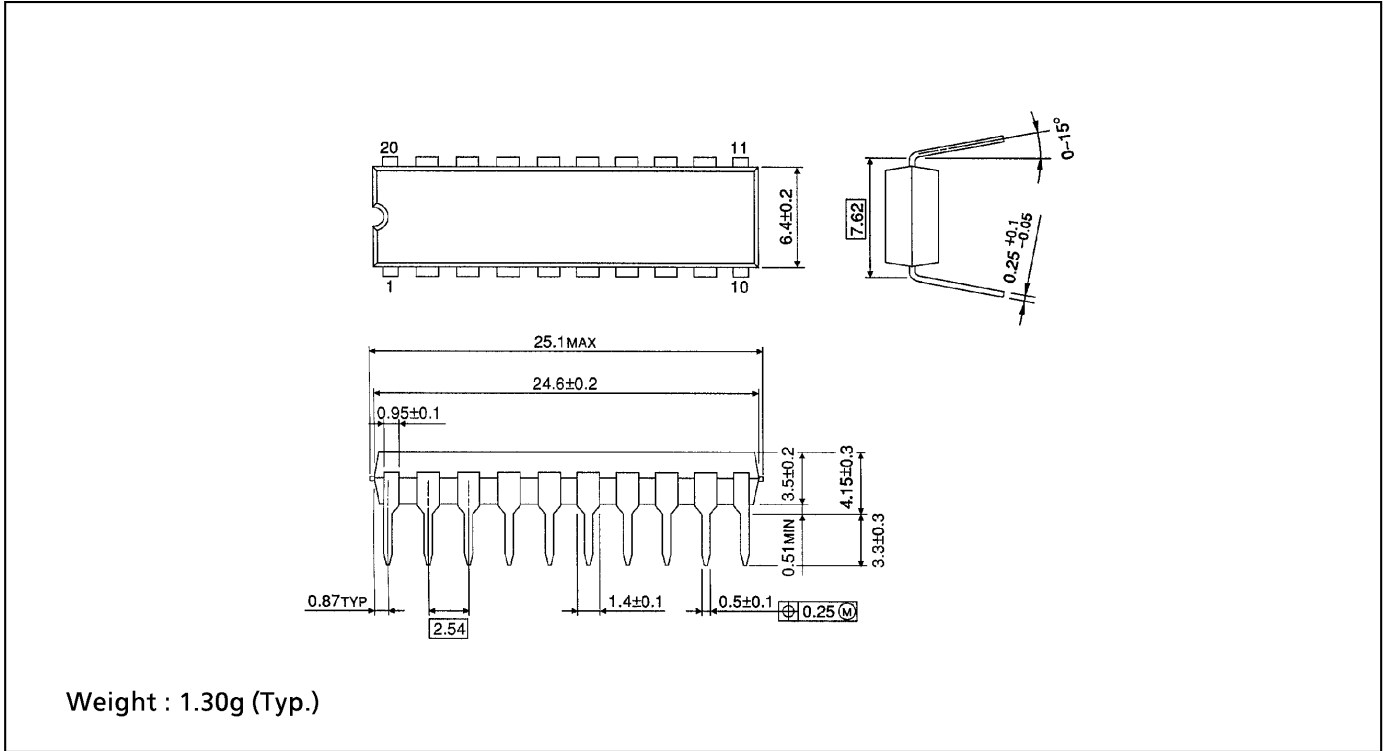
$$C_{PD} \text{ (total)} = 32 + 11 \cdot n$$

SYSTEM DIAGRAM



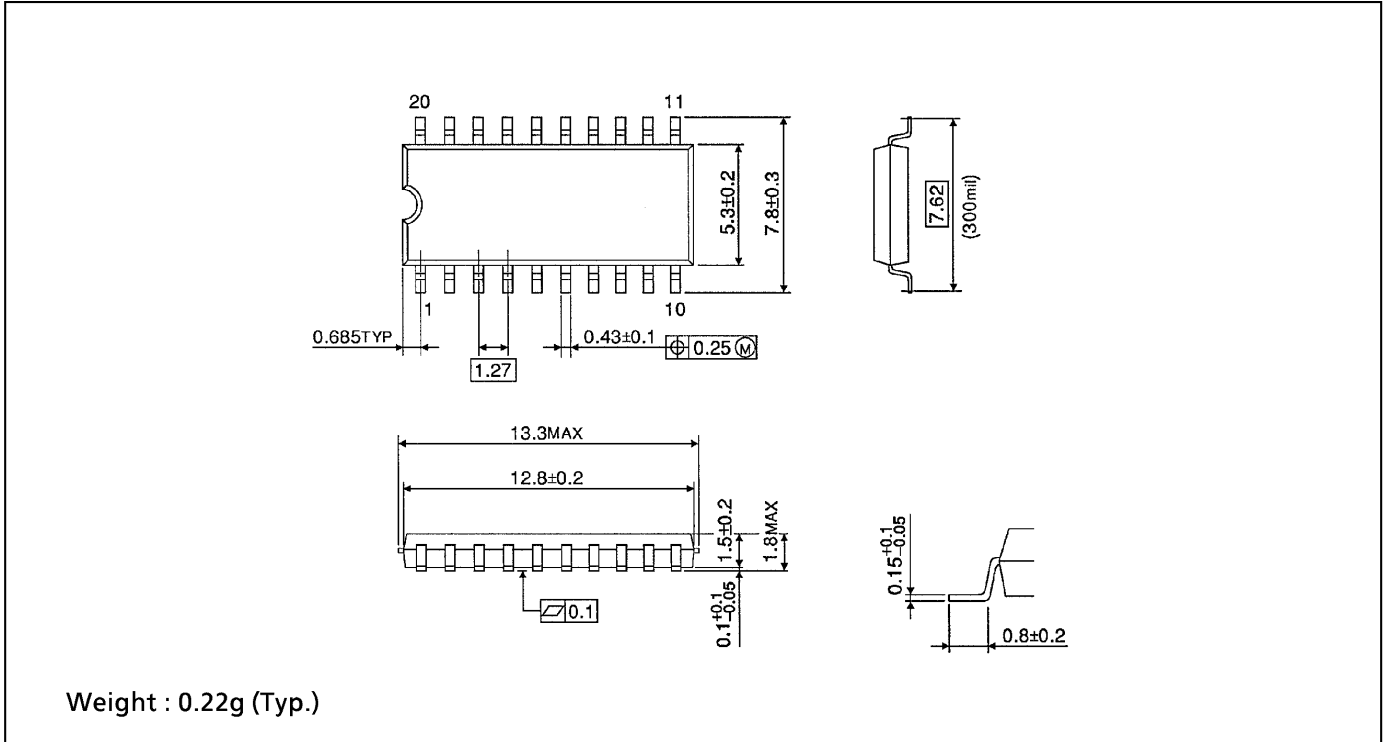
DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)

Unit in mm



SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

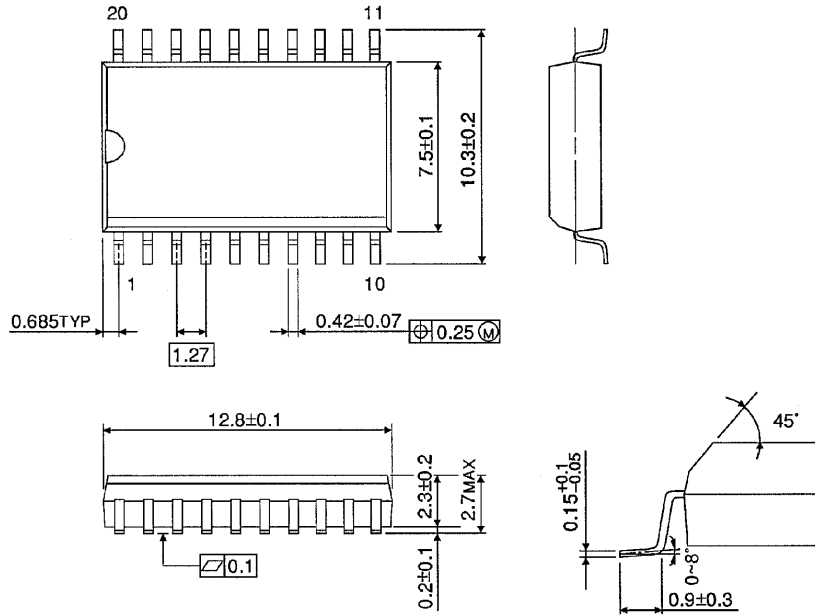
Unit in mm



SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

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