PRELIMINARY

AMD

Am79C983A

Integrated Multiport Repeater 2 (IMR2™)

DISTINCTIVE CHARACTERISTICS

- **Repeater functionality compliant with IEEE 802.3 Repeater Unit specifications**
- **Hardware implementation of Management Information Base (MIB) with all of the counters, attributes, actions, and notifications specified by IEEE 802.3 Section 19 *(Layer Management)***
- **Twelve pseudo AUI (PAUI™) ports to support multiple media types via direct connection to external transceivers**
- **One IEEE-compliant AUI port**
- **One reversible AUI (RAUI™) port that can be programmed as a second AUI port or used to connect directly to a media access controller (MAC)**
- **Direct interface with the AMD Am79C988A QuIET™ (Quad Integrated Ethernet Transceiver) to support 10BASE-T repeater designs**
- **Port switching support to allow individual ports to be switched between multiple Ethernet backplanes under software control**
- **Remote Monitoring (RMON) Register Bank to provide direct support for etherStatsEntry and etherStatsHistory object groups of the RMON MIB (IETF RFC1757)**
- **Packet Report Port to provide packet information for deriving objects in the Host, HostTopN, and Matrix groups of the RMON MIB (IETF RFC1578)**
- **Two user-selectable expansion bus modes: IMR/IMR+ compatible mode and asynchronous mode**
- **Simple 8-bit microprocessor interface**
- **Full LED support**
- **132-pin PQFP CMOS device with a single 5-V supply**

GENERAL DESCRIPTION

The Am79C983A Integrated Multiport Repeater 2 (IMR2) chip is a VLSI integrated circuit that provides a system-level solution to designing intelligent (managed) multiport repeaters. When the IMR2 device is combined with the Quad Integrated Ethernet Transceiver (QuIET) device, it provides a cost-effective solution to designing 10BASE-T managed repeaters. The IMR2 device integrates the repeater functions specified by Section 9 (*Repeater Unit*) and Section19 (*Layer Management for 10 Mb/s Baseband Repeaters*) of the IEEE 802.3 standard.

The Am79C983A IMR2 device provides 1 standard Attachment Unit Interface (AUI) port, 12 Pseudo Attachment Unit Interface (PAUI) ports, and 1 Reversible AUI (RAUI) port for direct connection to a media access controller (MAC). The pseudo AUI ports can be connected to external transceivers to support multiple media types, including 10BASE2, 10BASE-T, and 10BASE-FL/FOIRL. The pseudo AUI ports can be turned off individually (without external circuitry) to allow the switching of transceiver ports between IMR2 devices. This capability allows multiple IMR2 devices to be connected to a single set of transceivers, thus allowing straightforward implementations of port switching applications.

The IMR2 device also provides a Hardware Implemented Management Information Base (HIMIB™), which is a super set of the functions provided by the Am79C987 HIMIB device. All of the necessary counters, attributes, actions, and notifications specified by Section 19 of the IEEE 802.3 standard are included in the IMR2 device. To facilitate the design of managed repeaters, the IMR2 device implements a simple 8-bit microprocessor interface.

Support for an RMON MIB, as specified by the Internet Engineering Task Force (IETF) RFC 1757, is provided. Direct support is from an RMON Register Bank. Additional support is provided by the Packet Report Port, which supplies information that can be used in conjunction with a microprocessor to derive various RMON MIB attributes. With systems using multiple IMR2 de-

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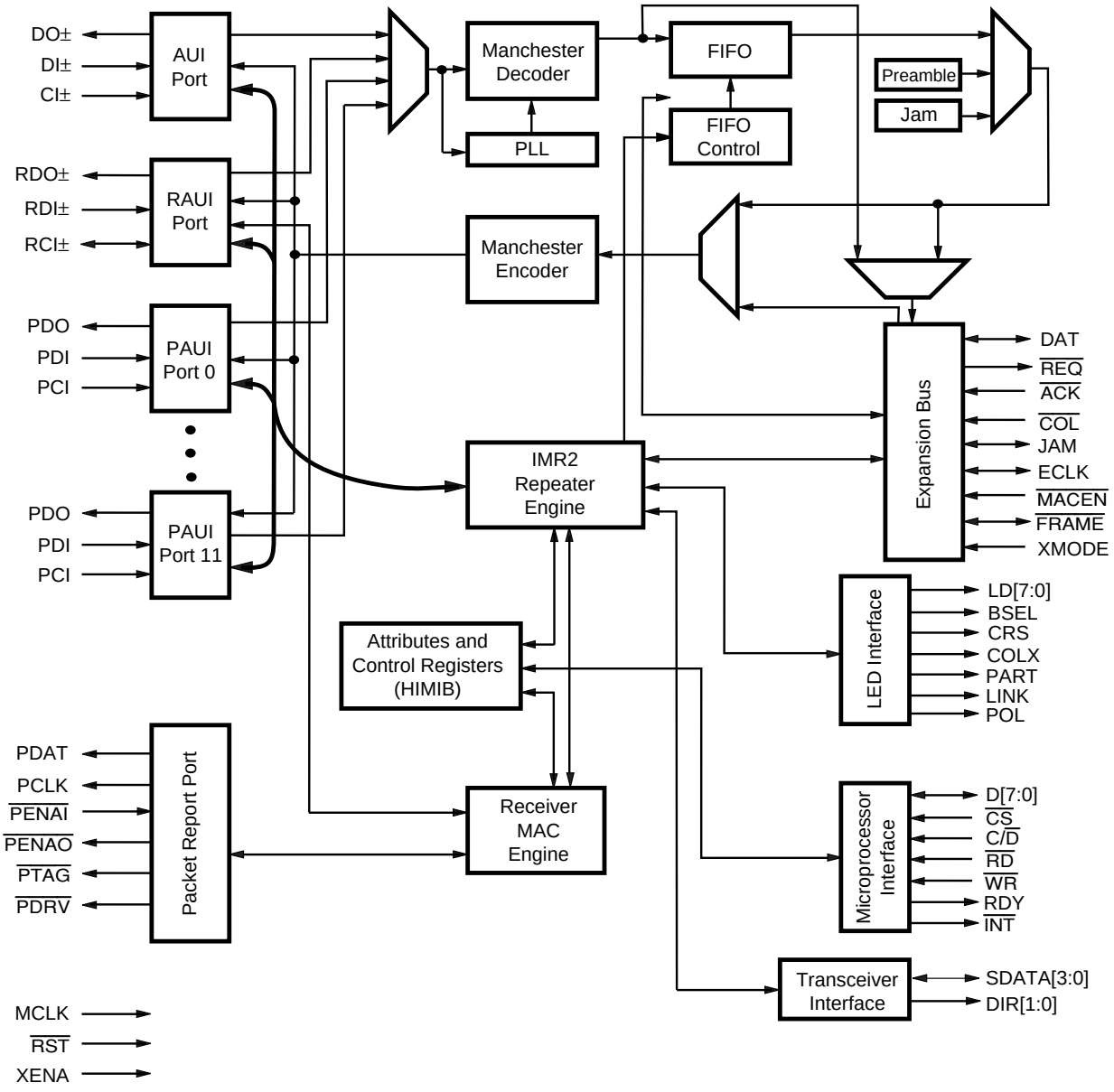
vices, the information is passed to a designated IMR2 device that transfers the information to a MAC.

For application examples on building fully-managed repeaters using the IMR2 and QuIET devices, refer to AMD's *IMR2 Technical Manual* (PID 19898A).

BLOCK DIAGRAM



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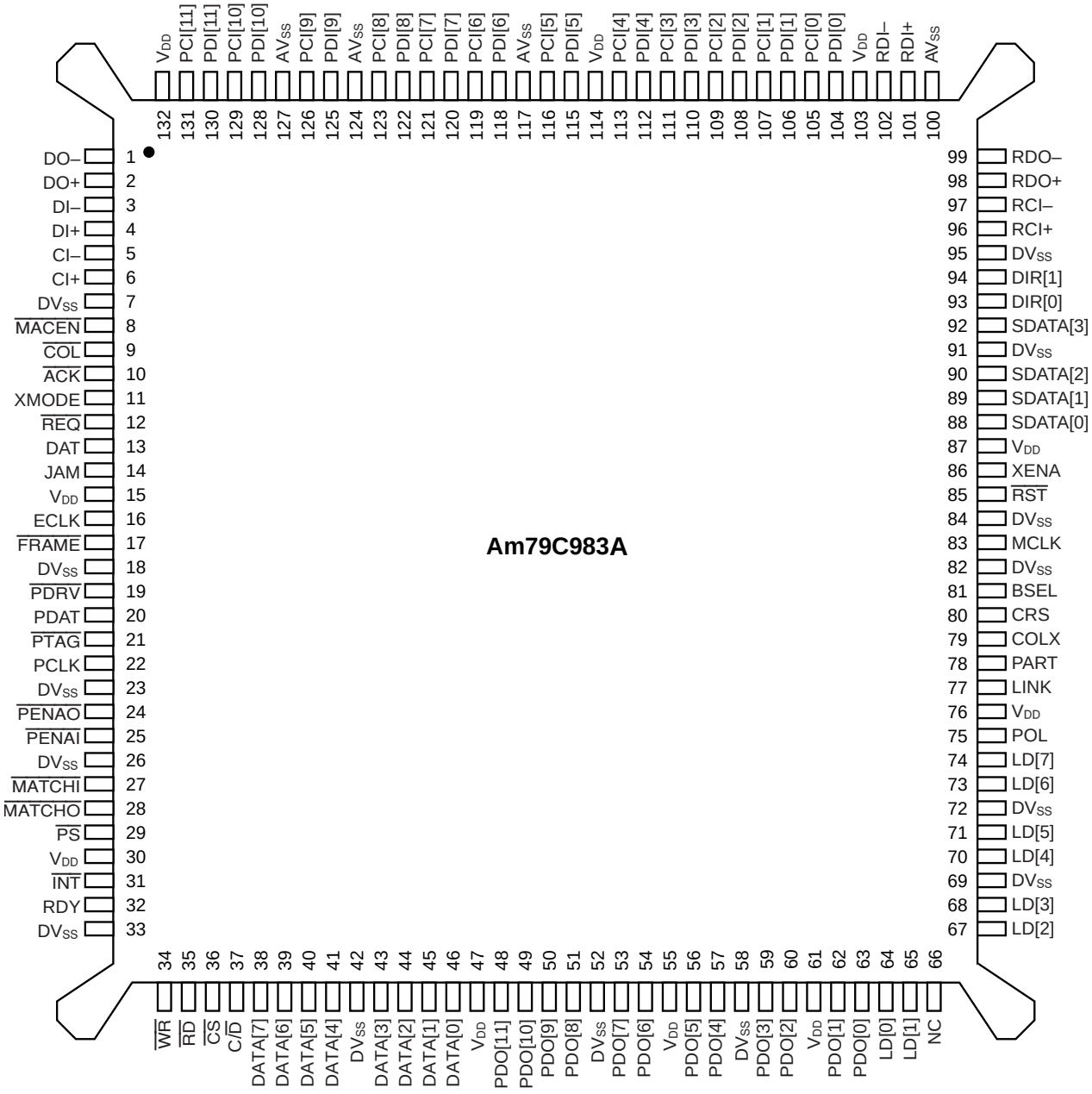
RELATED AMD PRODUCTS

Part No.	Description
Am79C981	Integrated Multiport Repeater+ (IMR+™)
Am79C982	*b*asic Integrated Multiport Repeater (*b*IMR™)
Am79C987	Hardware Implemented Management Information Base (HIMIB™)
Am79C988A	Quad Integrated Ethernet Transceiver (QuIET™)
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7996	IEEE 802.3/Ethernet/Cheapernet Transceiver
Am79C90	CMOS Local Area Network Controller for Ethernet (C-LANCE)
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am79C100	Twisted Pair Ethernet Transceiver Plus (TPEX+)
Am79C900	Integrated Local Area Communications Controller (ILACC™)
Am79C940	Media Access Controller for Ethernet (MACE™)
Am79C960	PCnet™-ISA Single-Chip Ethernet Controller (for ISA bus)
Am79C961	PCnet™-ISA+ Single-Chip Ethernet Controller for ISA (with Microsoft® Plug n' Play® Support)
Am79C961A	PCnet™-ISA II Full Duplex Single-Chip Ethernet Controller for ISA
Am79C965	PCnet™-32 Single-Chip 32-Bit Ethernet Controller
Am79C970	PCnet™-PCI Single-Chip Ethernet Controller (for PCI bus)
Am79C970A	PCnet™-PCI II Full Duplex Single-Chip Ethernet Controller (for PCI bus)
Am79C974	PCnet™-SCSI Combination Ethernet and SCSI Controller for PCI Systems

CONNECTION DIAGRAM

PQFP



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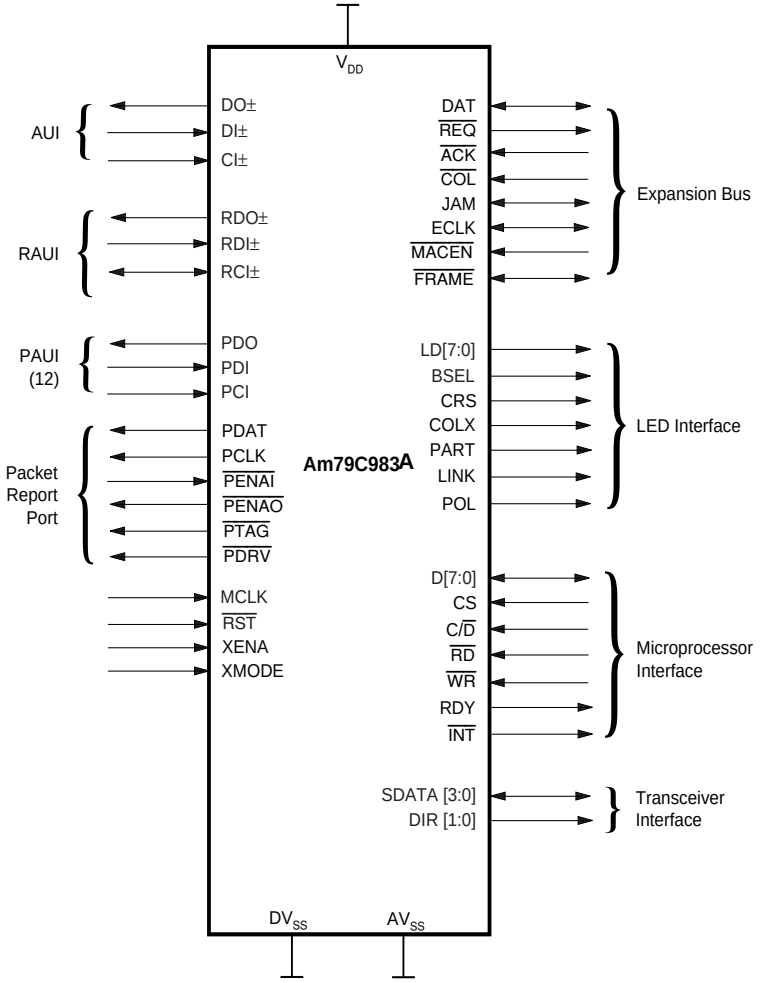
LOGIC SYMBOL



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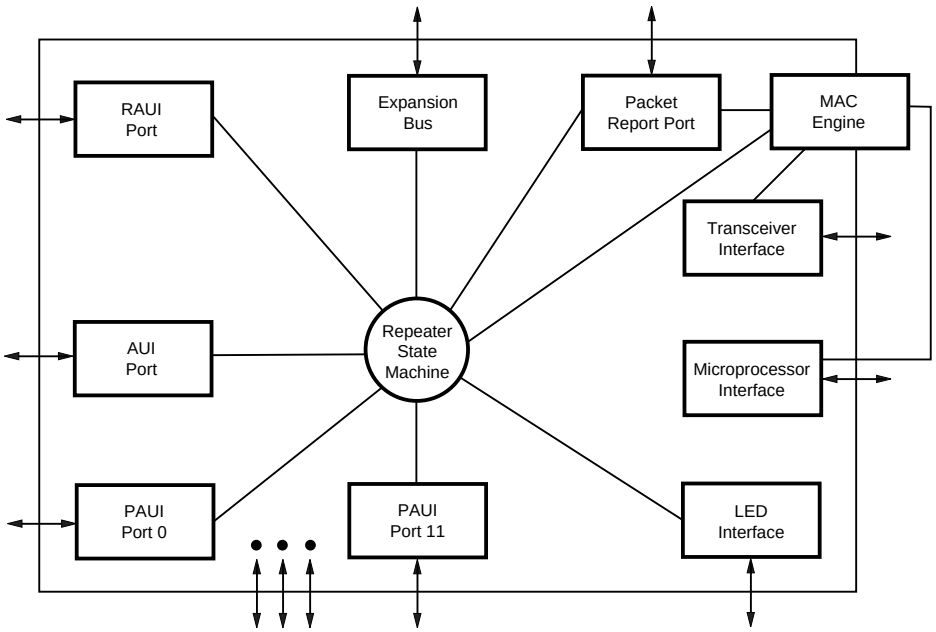
LOGIC DIAGRAM



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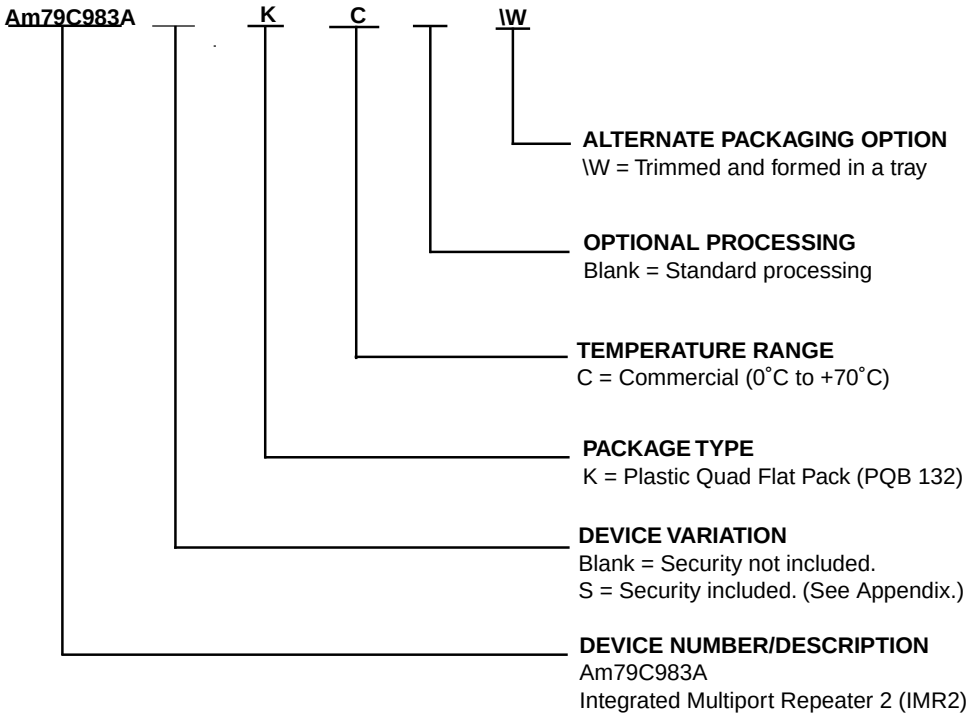
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am79C983A	KC, KC\W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

TABLE OF CONTENTS

PIN DESIGNATIONS

Listed by Pin Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	DO-	34	$\overline{WR}$	67	LD[2]	100	AVSS
2	DO+	35	$\overline{RD}$	68	LD[3]	101	RDI+
3	DI-	36	$\overline{CS}$	69	DVSS	102	RDI-
4	DI+	37	C/$\overline{D}$	70	LD[4]	103	VDD
5	CI-	38	D[7]	71	LD[5]	104	PDI[0]
6	CI+	39	D[6]	72	DVSS	105	PCI[0]
7	DVSS	40	D[5]	73	LD[6]	106	PDI[1]
8	$\overline{MACEN}$	41	D[4]	74	LD[7]	107	PCI[1]
9	$\overline{COL}$	42	DVSS	75	POL	108	PDI[2]
10	$\overline{ACK}$	43	D[3]	76	VDD	109	PCI[2]
11	XMODE	44	D[2]	77	LINK	110	PDI[3]
12	$\overline{REQ}$	45	D[1]	78	PART	111	PCI[3]
13	DAT	46	D[0]	79	COLX	112	PDI[4]
14	JAM	47	VDD	80	CRS	113	PCI[4]
15	VDD	48	PDO[11]	81	BSEL	114	VDD
16	ECLK	49	PDO[10]	82	DVSS	115	PDI[5]
17	$\overline{FRAME}$	50	PDO[9]	83	MCLK	116	PCI[5]
18	DVSS	51	PDO[8]	84	DVSS	117	AVSS
19	$\overline{PDRV}$	52	DVSS	85	$\overline{RST}$	118	PDI[6]
20	PDAT	53	PDO[7]	86	XENA	119	PCI[6]
21	$\overline{PTAG}$	54	PDO[6]	87	VDD	120	PDI[7]
22	PCLK	55	VDD	88	SDATA[0]	121	PCI[7]
23	DVSS	56	PDO[5]	89	SDATA[1]	122	PDI[8]
24	$\overline{PENAO}$	57	PDO[4]	90	SDATA[2]	123	PCI[8]
25	$\overline{PENAI}$	58	DVSS	91	DVSS	124	AVSS
26	DVSS	59	PDO[3]	92	SDATA[3]	125	PDI[9]
27	$\overline{MATCHI}$	60	PDO[2]	93	DIR[0]	126	PCI[9]
28	$\overline{MATCHO}$	61	VDD	94	DIR[1]	127	AVSS
29	$\overline{PS}$	62	PDO[1]	95	DVSS	128	PDI[10]
30	VDD	63	PDO[0]	96	RCI+	129	PCI[10]
31	$\overline{INT}$	64	LD[0]	97	RCI-	130	PDI[11]
32	RDY	65	LD[1]	98	RDO+	131	PCI[11]
33	DVSS	66	NC	99	RDO-	132	VDD

PIN DESCRIPTION

Pseudo AUI Pins

PDO_{0-11}
Pseudo AUI Data Output
Output/High Impedance

PDO is a single-ended output driver. PDO can be placed into a high impedance state, allowing multiple IMR2 devices to connect to a single QuIET device (port switching). The output data is Manchester encoded.

PDI_{0-11}
Pseudo AUI Receive Data Input
Input

The input data is Manchester encoded.

PCI_{0-11}
Pseudo AUI Collision Input
Input

PAUI port collision data receiver. A 10-MHz square wave indicates a collision has been detected on that port.

RAUI Port Pins

RDO+, RDO-
Reversible AUI Data Output
Output

RDO is a differential, Manchester output driver.

RDI+, RDI-
Reversible AUI Data Input
Input

RDI is a differential, Manchester receiver.

RCI+, RCI-
Reversible AUI Collision Input
Input/Output

RCI is a differential I/O. As an input, RCI receives a collision indication. As an output, RCI generates a 10-MHz square wave when a collision is sensed.

$\overline{PS}$
Output

This pin is reserved for factory use.

AUI Pins

DO+, DO-
AUI Data Output
Output

AUI port differential driver. Manchester encoded data.

DI+, DI-
AUI Data Input
Input

AUI port differential receiver. Manchester encoded data.

CI+, CI-
AUI Collision Input
Input

AUI port collision differential receiver.

Expansion Bus Pins

DAT
Data
Input/Output/High Impedance

The IMR2 device drives the DAT line with NRZ data when both $\overline{REQ}$ and $\overline{ACK}$ pins are asserted. DAT is an input if only the $\overline{ACK}$ signal is asserted. If $\overline{REQ}$ and $\overline{ACK}$ are not asserted, DAT enters a high impedance state. During collision when JAM is HIGH, DAT is used to signal a multiport (DAT=0) or single port (DAT=1) condition.

JAM
Jam
Input/Output/High Impedance

This pin is an output if the device is the only active IMR2 device. An IMR2 device is defined as active when it has one or more ports receiving or colliding, is in the state where it is still transmitting data from the internal FIFO, or is extending a packet to the minimum 96-bit times. If active, the IMR2 device drives the JAM pin HIGH to indicate that it is in a Collision state when both $\overline{REQ}$ and $\overline{ACK}$ pins are asserted. JAM is an input if only the $\overline{ACK}$ signal is asserted. If $\overline{REQ}$ and $\overline{ACK}$ are not asserted, JAM enters a high impedance state.

$\overline{REQ}$
Request
Output, Active LOW

This pin is driven LOW when the IMR2 device senses activity. An IMR2 device is defined as ACTIVE when it has one or more ports receiving or colliding, is in the state where it is still transmitting data from the internal FIFO, or is extending a packet to the minimum 96-bit times. The assertion of this signal signifies that the IMR2 device requires the DAT and JAM lines to transfer repeated data and collision status information to other IMR2 devices.

$\overline{ACK}$
Acknowledge
Input, Active LOW

When this signal is asserted by an external arbiter, it signals to the requesting IMR2 device that it may drive the DAT and JAM pins. It signals to other IMR2 devices the presence of valid collision status on the JAM line and valid data on the DAT line.

$\overline{\text{COL}}$
Collision
Input, Active LOW

When this pin is asserted by an external arbiter, it signifies that more than one IMR2 device is active and that each IMR2 device should generate the Collision Jam Sequence independently.

ECLK
Bus Clock
Input/Output

Data transitions on the expansion bus on DAT are synchronized to this clock. ECLK is a 10-MHz output clock when DAT is transmitting and a 10-MHz input clock when DAT is receiving. ECLK is only used when the expansion bus is operated in the asynchronous mode. ECLK should be terminated to ground with a 1 kΩ resistor. ECLK should be ignored in the synchronous mode.

$\overline{\text{MACEN}}$
MAC Enable
Input, Active LOW

When this pin is asserted, data on the expansion bus is included in MIB statistics. This is typically used when a MAC is driving the expansion bus.

$\overline{\text{MATCHO}}$

This pin should be tied to +5 V through a 1 kΩ ±10% resistor.

$\overline{\text{MATCHI}}$

This pin should be tied to +5 V through a 1 kΩ ±10% resistor.

$\overline{\text{FRAME}}$
Packet Framing Signal
Input/Output, Active LOW

$\overline{\text{FRAME}}$ defines the beginning and end of a packet. $\overline{\text{FRAME}}$ indicates valid data on the DAT pin when the expansion bus is in the asynchronous mode. $\overline{\text{FRAME}}$ is an output on the IMR2 device when it is transmitting over the expansion bus. It is an input on all other IMR2 devices.

XMODE
Expansion Bus Mode
Input

XMODE determines the mode of the expansion bus. XMODE should not be changed after $\overline{\text{RST}}$. Although changing XMODE after $\overline{\text{RST}}$ will change the expansion bus mode, the operation is unpredictable. Therefore, it is recommended that XMODE be tied either HIGH or LOW, depending on the desired expansion bus mode.

XMODE	Mode
1	Asynchronous
0	Synchronous (IMR/IMR+)

XENA
Port Enable
Input

XENA sets the default mode of the ports. It is used when $\overline{\text{RST}}$ transitions from LOW to HIGH.

XENA	Default
1	All ports are enabled.
0	All ports are disabled. The output drivers are in a high impedance state.

Note: *XENA only controls the default state. Once reset is completed, the enabling and disabling of ports is under software control. It is recommended that XENA be tied either HIGH or LOW, depending on the desired default state.*

Packet Report Port

PDAT
Packet Report
Output, High Impedance

PDAT outputs the beginning portion of a packet followed by packet status information. The size of the beginning portion is user programmable. If a second packet arrives before PDAT finishes transmitting status information, the second packet and corresponding status information are not transmitted over PDAT. The packet is aborted on collision.

$\overline{\text{PENAI}}$
Packet Report Enable Input
Input, Active LOW

$\overline{\text{PENAI}}$ senses when another device is transmitting over PDAT.

$\overline{\text{PENAO}}$
Packet Report Enable Output
Output, Active LOW, Open Drain

$\overline{\text{PENAO}}$ is TRUE when the IMR2 device is transmitting data over PDAT. If a second packet arrives before PDAT is finished transmitting status information, $\overline{\text{PENAO}}$ remains active for the second packet.

$\overline{\text{PDRV}}$
Packet Drive
Output, Active LOW

$\overline{\text{PDRV}}$ is TRUE when the IMR2 device is transmitting data over PDAT. If a second packet arrives before PDAT is finished transmitting status, $\overline{\text{PDRV}}$ goes FALSE after the status is transmitted.

PCLK
Packet Report Clock
Output, High Impedance

PCLK is a 10-MHz clock. PDAT transitions are synchronized to PCLK.

$\overline{\text{PTAG}}$
Packet Tag
Output, HIGH Impedance, Active LOW

$\overline{\text{PTAG}}$ indicates when the status frame is being transmitted over PDAT. It is asserted when the status frame is transmitted.

Microprocessor Interface

D[7:0]
Microprocessor Data
Input/Output

These pins are inputs when either $\overline{\text{CS}}$ or $\overline{\text{WR}}$ are LOW. They are outputs when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are LOW. Otherwise, these pins are high impedance.

$\overline{\text{CS}}$
Chip Select
Input, Active LOW

This pin enables the IMR2 device to read from or write to the microprocessor data bus.

C/$\overline{\text{D}}$
Control/Data
Input

This pin is used to select either a control register or a data register in the IMR2 device and is normally connected to the least significant bit of the address bus.

$\overline{\text{RD}}$
Read Strobe
Input, Active LOW

Initiates read operation.

$\overline{\text{WR}}$
Write Strobe
Input, Active LOW

Initiates write operation.

RDY
Ready
Output, Active HIGH, Open Drain

RDY is driven LOW at the start of every READ or WRITE cycle. RDY is released when the IMR2 device is ready to complete the transaction.

$\overline{\text{INT}}$
Interrupt
Output, Active LOW, Open Drain

The Interrupt pin is driven LOW when any of the unmasked (enabled) interrupts occur.

LED Interface

LD[7:0]
LED Drivers
Output

LD is the status output and is transmitted as 2 bytes. The byte number (high or low) is determined by BSEL.

BSEL
Byte Select
Output

When BSEL is LOW, LD[7:0] is transmitting the status of the first eight PAUI ports (ports P_7 through P_0). When BSEL is HIGH, LD[7:0] is transmitting the status of the rest of the PAUI ports (ports P_{11} through P_8), the AUI port, the RAUI port, and the expansion bus.

CRS
Carrier Sense Strobe
Output

When CRS is HIGH, LD [7:0] has carrier sense status.

COLX
Collision Status
Output

When COLX is HIGH, LD [7:0] has collision status.

PART
Partitioning Status
Output

When PART is HIGH, LD [7:0] has partitioning status.

LINK
Link Status
Output

When LINK is HIGH, LD [7:0] has link status.

POL
Polarity Status
Output

When POL is HIGH, LD [7:0] has polarity status.

Miscellaneous Pins

$\overline{\text{RST}}$
Reset
Input

When $\overline{\text{RST}}$ is LOW, the IMR2 device resets to its default state.

MCLK
Master Clock
Input

MCLK is a 20-MHz clock input.

Transceiver Device Interface

SDATA [3:0]
Serial Data
Input/Output

SDATA carries command and status data between the IMR2 device and the QuIET device (or other connected transceiver).

Pin	Transceiver Ports
SDATA [0]	PAUI [3:0]
SDATA [1]	PAUI [7:4]
SDATA [2]	PAUI [11:8]
SDATA [3]	Arbitrary ports

DIR
Direction
Output

DIR sets the direction of data on SDATA[3:0] The settings are as follows:

DIR[1:0]	Function
00	Transceiver (QuIET device) drives SDATA with status and device ID.
01	SDATA is a high impedance output.
10	SDATA is a high impedance output.
11	IMR2 device drives SDATA with commands.

V_{DD}
Power Pin

These pins supply +5 V power.

AV_{SS}
Analog Ground
Ground Pin

These pins provide the ground reference for the analog portions of the IMR2 circuitry. These pins should be decoupled and kept separate from the digital ground plane.

DV_{SS}
Digital Ground
Ground Pin

These pins provide the ground reference for the digital portions of the IMR2 circuitry. These pins should be decoupled and kept separate from the analog power plane.

FUNCTIONAL DESCRIPTION

Overview

The Am79C983A Integrated Multiport Repeater 2 device provides a system-level solution to designing IEEE 802.3 managed repeaters. It includes 12 pseudo AUI (PAUI) ports for single-ended connections to external transceivers. The IMR2 device interfaces directly with AMD's Am79C988A Quad Integrated Ethernet Transceiver (QuIET) device for 10BASE-T implementations. The PAUI ports can be turned off individually to enable port switching applications. In addition, the IMR2 device has a standard AUI port and a reversible AUI (RAUI) port for a direct connection to a MAC.

The IMR2 device provides a Hardware Implemented Management Information Base (HIMIB) which contains all of the necessary counters, attributes, actions, and notifications specified by Section 19 of the IEEE 802.3 standard. Support for an RMON MIB, as specified by the Internet Engineering Task Force (IETF) RFC 1757, is also provided. Direct support is from an RMON Register Bank. Additional support is provided by the Packet Report Port, which supplies packet information that can be used in conjunction with a microprocessor to derive various RMON MIB attributes.

Basic Repeater Functions

The IMR2 repeater functions are summarized below. An overview of IMR2 management functions is presented under *Basic Management Functions*.

Repeater Function

If any single network port of a repeater system senses the start of a valid packet on its receive lines, the IMR2 device will retransmit the received data to all other enabled network ports unless a collision is detected. The repeated data will also be presented on the DAT line of the expansion bus to facilitate designs utilizing multiple IMR2 devices. The IMR2 device fully complies with Section 9.5.1 of the IEEE 802.3 specifications.

Signal Regeneration

When retransmitting a packet, the IMR2 device ensures that the outgoing packet complies with the IEEE 802.3 specification in terms of preamble structure. Data packets repeated by the IMR2 device will contain a minimum of 56 preamble bits before the Start of Frame Delimiter.

The IMR2 device, by virtue of its internal Phase Lock Loop and Manchester Encoder/Decoder, will ensure correct regeneration of the repeated signal at its PAUI and AUI outputs. If the outputs of the IMR2 device are connected to QuIET device transceivers, the 10BASE-T outputs of the QuIET devices will meet the IEEE 802.3 signal symmetry requirements. If other types of transceivers are used, the signal characteristics will depend, in part, on the transceiver.

Jabber Lockup Protection

The IMR2 chip implements a built-in jabber protection scheme to ensure that the network is not disabled due to transmission of excessively long data packets. This protection scheme will automatically interrupt the transmitter circuits of the IMR2 device for 96-bit times, if the IMR2 device has been transmitting continuously for more than 65,536 bit times. This is referred to as MAU Jabber Lockup Protection (MJLP). The MJLP status for the IMR2 chip can be read from the Repeater Status Register.

Collision Handling

The IMR2 chip will detect and respond to collision conditions as specified in the IEEE 802.3 specification. A multiple IMR2 device repeater implementation also complies with the specification because of the inter-IMR2 chip status communication provided by the expansion port. Specifically, a repeater based on one or more IMR2 devices will handle correctly the transmit collision and one-port-left collision conditions as specified in Section 9 of the IEEE 802.3 specification.

Fragment Extension

If the total packet length received by the IMR2 device is less than 96 bits, including preamble, the IMR2 chip will extend the repeated packet length to 96 bits by appending a Jam sequence to the original fragment. Note that in a few cases, it is possible for the IMR2 device to generate a sequence 97 bits in length when the expansion bus is operated in the asynchronous mode.

Auto Partitioning/Reconnection

Any of the IMR2 ports can be partitioned under excessive duration or frequency of collision conditions. Once a port is partitioned, the IMR2 device will continue to transmit data packets to a partitioned port, but will not respond (as a repeater) to activity on the partitioned port's receiver. The IMR2 chip will monitor the port and reconnect it once certain criteria indicating port "wellness" are met. The criteria for reconnection are specified by the IEEE 802.3 standard. In addition to the standard reconnection algorithm, the IMR2 device implements an alternative reconnection algorithm which provides a more robust partitioning function. Each port is partitioned and/ or reconnected separately and independently of other network ports.

Either one of the following conditions occurring on any enabled IMR2 device network port will cause the port to partition:

a. An SQE signal active for more than 2048 bit times.

b. A collision condition occurs during each of 32 consecutive attempts to transmit to that port.

Once a network port is partitioned, the IMR2 device will reconnect that port if the following is met:

a. Standard reconnection algorithm—A data packet longer than 512-bit times (nominal) is transmitted or received by the partitioned port without a collision.

b. Alternate reconnection algorithm—A data packet longer than 512-bit times (nominal) is transmitted by the partitioned port without a collision.

Basic Management Functions

Repeater Management

The IMR2 management functions are a super-set of the those provided by the AMD's IMR+/HIMIB device chipset. The IMR2 device contains the complete set of repeater and port functions as defined in ANSI/IEEE 802.3, *Repeater Management Standard*, (Section 19). All mandatory and optional capabilities are supported. These include the Basic Control, Performance Monitoring, and Address Tracking packages. Additionally, Node Address Mapping, MAU Management specific functions, and intrusion protection functions are included. Support is also provided for the RMON MIB RFC 1757.

All information is stored in registers which can be accessed through the Microprocessor Interface (Node Processor Port). The register location is defined by a register bank and an address within that register bank. Address and data of the registers are multiplexed using the C/$\overline{D}$ pin. The register address is selected by writing to the Node Processor Port with C/$\overline{D}$ HIGH. The register data is selected by writing or reading to the Node Processor Port with C/$\overline{D}$ LOW.

Many of the registers are larger than 1 byte. For these registers, consecutive accesses to register data (equal to the number of bytes in the register) are required. The order is LSByte to MSByte. For a write operation, if the address changes before all the bytes are written, the register is not changed to the new value.

The Status Register is accessed by reading the Node Processor Port with the C/$\overline{D}$ pin HIGH. This reduces the number of operations necessary to access the Status Register.

All bit fields are ordered such that the left most bit is the most significant bit. Unused register banks, ports and register numbers are reserved and should not be accessed as this may cause device malfunction. When specifying the register bank or port number, the following format is used:

C Port Write

0	0	0	P4	P3	P2	P1	P0

MSB LSB

P4:0 represent the Register Bank or Port Number, organized as follows:

$P = P_4\,P_3\,P_2\,P_1\,P_0$

P	Port/Register Bank
0	Repeater Registers
1	Interrupt Registers
2	Interrupt Control Registers
3	Port Control Registers
4	Port Status Registers
5	RMON Registers
7	Packet Report Registers
16- 30	Port Attributes

The register to be accessed for reading or writing is specified by writing the following control byte to the C register:

C Port Write

1	1	1	R4	R3	R2	R1	R0

MSB LSB

$R = R_4\,R_3\,R_2\,R_1\,R_0$

Figure 1 shows the Management Register Map, and Table 1 shows register banks and register assignments within the register banks.

RMON

Remote monitoring (RMON) functions are designed to give the management system the capability to remotely monitor the hub for diagnostic purposes. The rules for RMON are described in the RMON MIB (as of this writing IETF RFC1578).

The IMR2 device provides direct support for both the statistics and history object groups. Indirect support is provided for the alarm, host, hostTopN, event, and matrix groups. Direct support is provided via the RMON register set and relevant attribute registers. Indirect support is provided through the Packet Report Port.

Packet Reports

The IMR2 device generates status information on every packet that it repeats. The data is transmitted over the Packet Report Port. The data format consists of the beginning of the packet followed by a packet tag and statistical data on the packet.

Preamble	DA	SA	T/L	Packet Data Var. Length	Port No., Tag & Status	New FCS

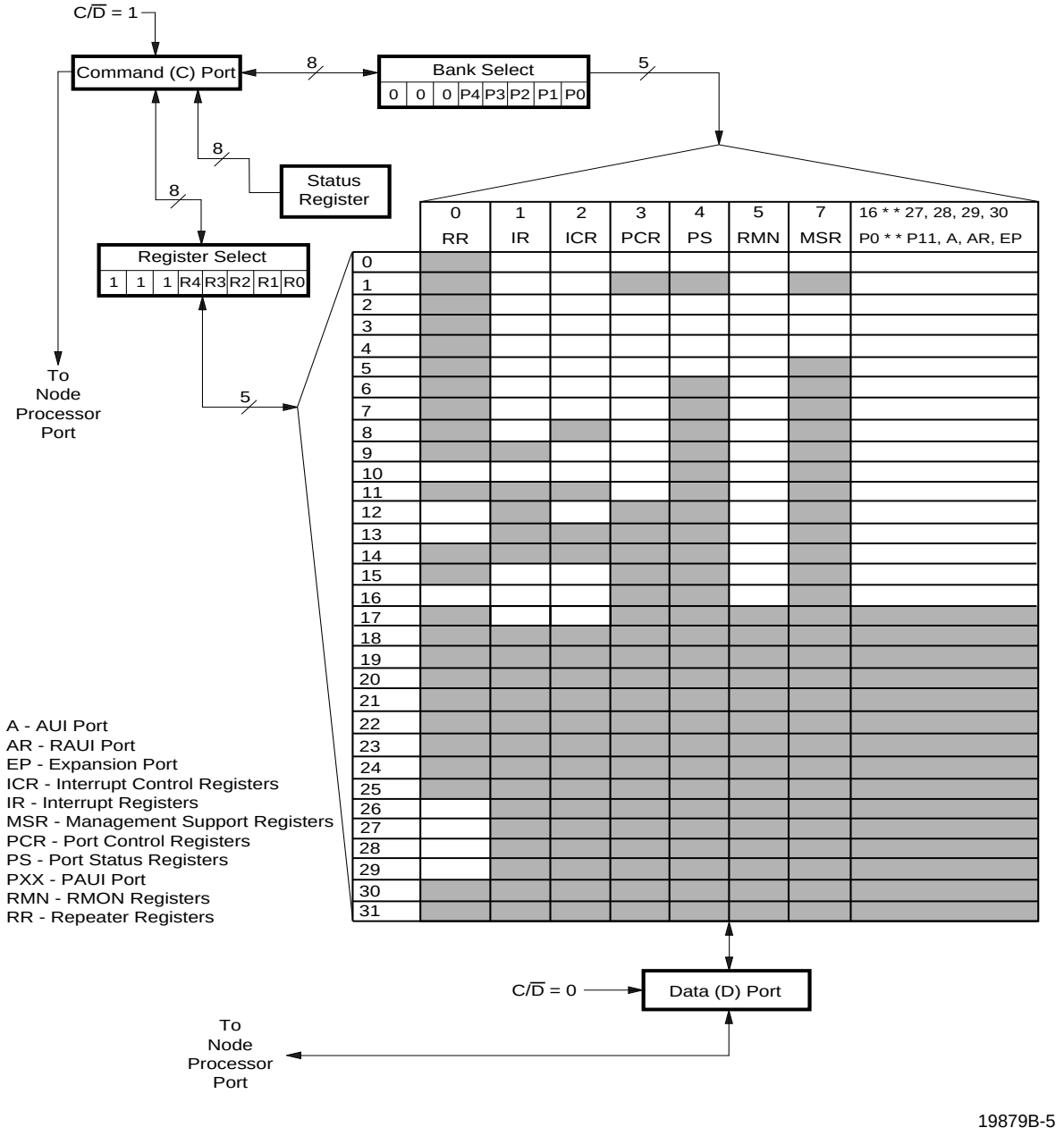


Figure 1. Management Register Map

Table 1. Management Registers

Reg. No.	Register Bank 0 Repeater Registers	Register Bank 1 Interrupt Registers	Register Bank 2 Interrupt Control Registers	Register Bank 3 Port Control Registers
0		Port Partition Status Change Interrupt	Partition Change Interrupt Enable	Alternative Partition Algorithm Enable
1		Runts with Good FCS Interrupt	Runts with Good FCS Interrupt Enable	
2		Link Status Change Interrupt	Link Status Change Interrupt Enable	Link Test Enable
3		Loopback Error Change Interrupt	Loopback Error Change Interrupt Enable	Link Pulse Transmit Enable
4		Polarity Change Interrupt	Polarity Change Interrupt Enable	Automatic Receiver Polarity Reversal Enable
5		SQE Test Error Change Interrupt	SQE Test Error Change Interrupt Enable	SQE Mask Enable
6		Source Address Changed Interrupt	Source Address Changed Interrupt Enable	Port Enable/Disable
7		Intruder Interrupt	Intruder Interrupt Enable	Port Mobility Control
8		Source Address Match Interrupt		Extended Distance Enable
9			Multicast Address Pass Enable	Last Source Address Automatic Intrusion Control
10	Source Address Match Register	Data Rate Mismatch Interrupt	Data Rate Mismatch Interrupt Enable	Pref. Source Address Automatic Intrusion Control
11				Last Source Address Lock Enable
12	Total Octets		Last Source Address Compare Enable	
13	Transmit Collisions			
14				
15		Transceiver Interface Status	Preferred Address Compare Enable	
16	Configuration Register	Transceiver Interface Changed Interrupt	Transceiver Interface Changed Interrupt Enable	
17		Jabber Interrupt	Jabber Interrupt Enable	
18				
19				
20				
21				
22				
23				
24				
25				
26	Repeater Status			
27	QuIET Device ID Register			
28	Repeater Device and Revision Register			
29	Device Configuration			
30				
31				

Table 1. Management Registers (Continued)

Reg. No.	Register Bank 4 Port Status Registers	Register Bank 5 RMON Registers	Register Bank 7 Management Support Registers	Register Bank 16-30 Port Attribute Registers
0	Partitioning Status of Ports	etherStatsOctets	Device ID	Readable Frames
1		etherStatsPkts		Readable Octets
2	Link Test Status of Ports	etherStatsBroadcastPkts	Sample Error Status	Frame Check Sequence Errors
3	Loopback Error Status	etherStatsMulticastPkts	Report Packet Size	Alignment Errors
4	Receive Polarity Status	etherStatsCRCAlignErrors	Statistics Control	Frames Too Long
5	SQE Test Status	etherStatsUndersizePkts		Short Events
6		etherStatsOversizePkts		Runts
7		etherStatsFragments		Collisions
8		etherStatsJabbers		Late Events
9		etherStatsCollisions		Very Long Events
10		etherStats64Octets		Data Rate Mismatches
11		etherStats65to127Octets		Auto Partition
12		etherStats128to255-Octets		Source Address Changes
13		etherStats256to511-Octets		Readable Broadcast Frames
14		etherStats512to1023-Octets		Last Source Address
15		etherStats1024to1518-Octets		Readable Multicast Frames
16		Activity		Preferred Source Address
17				
18				
19				
20				
21				
22				
23				
24				
25				
26				
27				
28				
29				
30				
31				

Detailed Functions

This section describes the detailed functional behavior of the IMR2 device. Where necessary, the behavior is defined in terms of state machines. Note that this is a conceptual definition and the actual implementation may be different.

Reset

Hardware Reset

The IMR2 device enters the reset state when the $\overline{RST}$ pin is driven LOW. The reset pin should be held LOW for a minimum of 150 µs after power-up or 4 µs otherwise. This allows the IMR2 device to reset the internal logic. During reset, the registers are set to their default values. The output signals are placed in their inactive state. That is, all analog outputs are placed in their idle state, all bidirectional signals are not driven, all active-HIGH signals are driven LOW, and all active-LOW signals are driven HIGH. The only exception is POL, which defaults to HIGH on reset. In a multiple IMR2 device repeater, the reset signal should be synchronized to MCLK when the expansion bus is operated in the synchronous mode.

Reset does not affect the RMON registers (Register Bank 5) or the Port Attribute Registers (Register Banks 16-30). These registers will power up at a random value. They can be preset while the IMR2 is in software reset or while the port is disabled via the microprocessor interface.

The mode of the expansion bus and the default state of the ports are set by XMODE and XENA during $\overline{RST}$. XMODE sets the expansion bus mode and XENA sets the port state. Note that XENA only controls the default state. Once reset is completed, the enabling and disabling of the ports is under software control. The settings are as follow:

XMODE	1	The expansion bus is in the asynchronous (IMR2) mode.
	0	The expansion bus is in the synchronous (IMR/IMR+) mode.
XENA	1	All ports are enabled.
	0	All PAUI ports are disabled. The output drivers are placed in a high impedance state.

Software Reset

The IMR2 device supports software reset with two bits on the Device Configuration Register: Repeater Reset (R - bit 7 on the register) and Management Reset (M - bit 6 on the register). Bit R resets the registers, repeater, and MAC engine. Setting Bit R is the functional equivalent of hardware reset, with the exception that the microprocessor interface is not reset and the ability to access 4 and 6 byte attribute registers is maintained. Bit M affects only the management and intrusion protection functions of the IMR2 device.

Bit R causes the IMR2 device to go into the default state. As with hardware reset, all analog outputs are placed in their idle state, all bidirectional signals are not driven, all active-HIGH signals are driven LOW, and all active-LOW signals are driven HIGH. The only exception is POL, which defaults to HIGH on reset. Registers are also set to their default state.

Setting Bit R also allows write access to the MIB registers and some other read-only registers. These registers are the Total Octets Register, the Transmit Collision Register, the entire RMON Register Bank, and the Port Attribute Register Banks. Note that the Last Source Address Register and the Preferred Source Address Register can also be written into when bit R is not set. Setting bit R will not affect any bit of the Device Configuration Register. Thus, the IMR2 device does not automatically exit software reset. Software reset must be exited by setting bit R to zero.

The function of bit M is a subset of the function of bit R. It affects the intrusion protection and MIB registers. Setting bit M causes the intrusion protection registers to go into the default state. As with bit R, the MIB registers can be written into. 2 lists the default state of the registers. If the M column has an M, the corresponding register is set to its default state when bit M is set.

Expansion Bus

The expansion bus has two modes of operation: the synchronous (IMR/IMR+ compatible) mode and the asynchronous mode. The modes are differentiated by the expansion bus clock. In the synchronous mode, the IMR2 devices (and any IMR/IMR+ devices) are all clocked by a single 20-MHz clock. The IMR2 device uses MCLK as the clock source.

In the asynchronous mode, IMR2 devices can be clocked (MCLK) by different sources. The single IMR2 device transmitting over the expansion bus provides the clock source for data. The clock pin in this mode is ECLK. ECLK clocks the data. All other expansion bus signals are asynchronous. The mode of expansion bus operation is selected during reset by XMODE.

The expansion bus can be configured for connection to a MAC. The pin $\overline{MACEN}$ selects the MAC mode. When $\overline{MACEN}$ is TRUE (LOW), the statistics on the data received by DAT are recorded in the management registers. The expansion bus is considered another port in the same sense as the PAUIs, the AUI, and the RAUI.

Synchronous Mode Operation

While operating in the synchronous mode, the expansion bus pins are Data (DAT), JAM, Request ($\overline{REQ}$), Acknowledge ($\overline{ACK}$), and Collision ($\overline{COL}$). DAT and JAM are bidirectional signals. $\overline{REQ}$ is an output. $\overline{ACK}$ and $\overline{COL}$ are inputs.

Table 2. Register Reset Default States

Register	Default	M
Configuration		M, R
Enable Interrupts	Masked	
Source Address Match Interrupt	Masked	
Repeater Status		
MJLP	No Error	R
Device Configuration		
Repeater Reset	Normal	
Management Reset	Normal	
RAUI Direction	Normal	
Loopback Test Mode	Normal	
Transceiver Loopback	Normal	
Partition Change Interrupt	None	R
Runts with Good FCS Interrupt	None	M, R
Link Change Interrupt	None	R
Loopback Change Interrupt	None	R
Polarity Changed Interrupt	None	R
SQE Test No Change Interrupt	None	R
Source Address Changed Interrupt	None	M, R
Intruder Interrupt	None	M, R
Source Address Match Interrupt	None	M, R
Data Rate Mismatch Interrupt	No Mismatch	R
Transceiver Interface Status	No Trans.	R
Transceiver Interface Change Interrupt	None	R
Jabber Interrupt	No Jabber	R
Partition Change Interrupt Enable	Masked	R
Runts with Good FCS Interrupt Enable	Masked	M,R
Link Changed Interrupt Enable	Masked	R
Loopback Changed Interrupt Enable	Masked	R
Polarity Changed Interrupts Enable	Masked	R
SQE Test Changed Interrupt Enable	Masked	R
Source Address Changed Interrupt Enable	Masked	M,R
Intruder Interrupt Enable	Masked	M, R
Multicast Address Pass Enable	Disabled	M, R
Data Rate Mismatch Interrupt Enable	Masked	R
Source Address Compare Enable	Disabled	M, R
Preferred Address Compare Enable	Disabled	M, R
Transceiver Interface Changed Interrupt Enable	Masked	R
Jabber Interrupt Enable	Masked	R
Alternative Partition	Disabled	R
Link Test Enable	Enabled	R
Link Pulse Enable	Enabled	R
Reverse Polarity Enable	Disabled	R
SQE Mask Enable	Disabled	R
Port Enable	Enabled	R
Port Mobility Control	XENA	R
Extended Distance Control Enable	Disabled	R
Source Address Automatic Intrusion Enable	Disabled	R
Preferred Address Automatic Intrusion Enable	Disabled	R
Last Source Address Lock Enable	Disabled	M, R
Partition Status	Connect	R
Link Status	Link Fail	R
Loopback Status	No Error	R
Polarity Status	Positive	R
SQE Test Status	No Error	R
Sample Counter Que	Four	M, R
Packet Report Packet Size	07FF‘	M, R
Statistics Control		
Stat Tag	Disable	M, R
FCS Tag	Disable	M, R

The IMR2 device expansion scheme allows the use of multiple IMR2 devices in a single-board repeater or in a modular multiport repeater with a backplane architecture. Data sent on the DAT line is in NRZ format and is synchronized to MCLK. Another bidirectional pin, JAM, is used to communicate internal IMR2 device status from the single active IMR2 device to other IMR2 devices in the system. This signal indicates whether the active IMR2 device is in a collision state.

Arbitration for control of the bussed signals, DAT and JAM, is provided by external circuitry. One output pin ($\overline{REQ}$) and two input pins ($\overline{ACK}$ and $\overline{COL}$) are used as arbitration signals. The IMR2 device asserts $\overline{REQ}$ to

indicate that it is active and is ready to drive the DAT and JAM signals. The external arbiter asserts $\overline{ACK}$ if one and only one IMR2 device has $\overline{REQ}$ asserted. This allows the corresponding IMR2 device to drive the DAT line with data to be repeated by all other IMR2 devices. If there is more than one IMR2 device asserting $\overline{REQ}$, the external arbiter should assert $\overline{COL}$, indicating multiple IMR2 devices are active.

The active IMR2 device drives the JAM line HIGH in order to signal other IMR2 devices that it has detected a collision across one or more of its ports and is generating a Jam Sequence. The DAT line is used during single IMR2 device collision (JAM asserted) to signal single-port collision (DAT HIGH) or multiport collision (DAT LOW). Other IMR2 devices synchronize their internal Collision Jam Sequence generators using JAM and DAT pins as inputs.

If more than one IMR2 device is active (multiple $\overline{REQ}$s asserted), the external arbiter should assert the $\overline{COL}$ line to signal this condition. In this case, all IMR2 devices in the repeater are forced into the multiport collision state and will generate Jam sequence independently while this condition lasts. As ports on separate IMR2 devices back off, the last IMR2 device with an active port regains control of the DAT and JAM signals and all other IMR2 devices will continue generating Jam sequence while the JAM signal is asserted.

In a typical single-board application, three IMR2 devices can be connected together without the use of external transceivers. The total number of IMR2 devices that can be used in a more complex architecture will depend on the drive capability, system timing limitations, and system design.

The external arbiter is required to generate two signals ($\overline{ACK}$ and $\overline{COL}$). The logic function for these signals in a three IMR2 device Repeater Unit is as follows:

ACK = REQ1 & !REQ2 & !REQ3 + !REQ1 & REQ2 & !REQ3 + !REQ1 & !REQ2 & REQ3

COL = !(ACK + !REQ1 & !REQ2 & !REQ3)

Asynchronous Mode Operation

The operation of the expansion bus in the asynchronous mode is similar to the operation in the synchronous mode. The primary difference is that the clock signal in the asynchronous mode is ECLK, which is sourced by the IMR2 device transmitting DAT. The signals JAM, $\overline{REQ}$, $\overline{ACK}$, and $\overline{COL}$ are all asynchronous.

DAT is synchronized to ECLK, which is a 10-MHz clock signal. When the IMR2 device asserts $\overline{REQ}$ and receives an $\overline{ACK}$, ECLK is an output. When the IMR2 device does not assert $\overline{REQ}$ and receives an $\overline{ACK}$, ECLK is an input.

In the asynchronous mode, it is probable that ECLK and the master clocks of the receiving IMR2 devices will be skewed in frequency. To help the IMR2 devices accommodate the frequency differences, the expansion bus transmits a framing signal ($\overline{FRAME}$). See Figure 2.

Because JAM is an asynchronous signal, there is no defined relationship between JAM and ECLK.

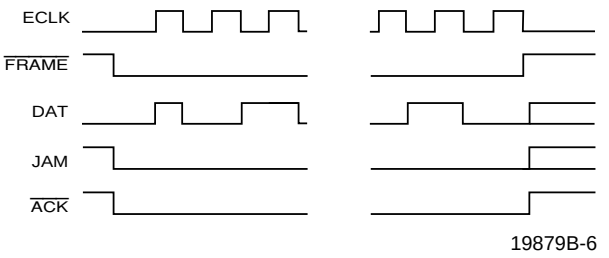


Figure 2. Asynchronous Mode Data Transfer

Packet Statistics

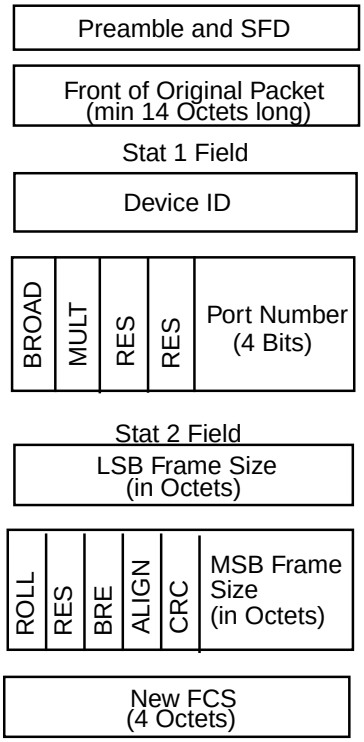
Packet Report Port

For each packet, the IMR2 device can compile a set of data about that packet. This data, which will now be referred to as the report packet, allows the system to derive objects in the Host, HostTopN, and Matrix groups of the RMON MIB (RFC 1757). The Report Packet is delivered by the Packet Report Port (PR).

The PR port transmits a portion of the packet along with data about that packet to a MAC. The format of the report packet is shown in 3. Sending only a portion of the packet is referred to as packet compression.

The degree to which the original packet is compressed is set by the Report Packet Size Register. The size is in bytes. If the register is set to 14 or less, the size of the packet passed is 14 bytes. If the register is set to 1536 or greater, the entire packet is passed. If the packet size is equal to or less than the value set in the Report Packet Size Register, the entire packet is passed.

If the destination address of the packet is the same as the address of the MAC connected to the PR Port, then it is desirable to have the entire packet transmitted to the MAC. Therefore, packet compression is automatically disabled when the destination address of the packet is a valid address for the expansion bus. However, the report tag is appended to the end of the packet. Note that the entire packet is also sent if the destination address is a broadcast address.



BROAD - Broadcast Address Match
MULT - Multicast Address Match
RES - Reserved. Set to Zero.
ROLL- Frame Size has exceeded 1535 bytes
BRE - Bit Rate Error
ALIGN - Framing Error
CRC - CRC Error

***Note**: The bit designation is LSB to the left and MSB to the right. The fields are transmitted LSB first.*

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Figure 3. Detailed Report Packet

The presence of a valid destination address is determined by comparing the destination address of the packet with the Last Source Address Register and the Preferred Source Address Register associated with the expansion bus. Comparison is enabled by setting the EP bit of the Last Source Address Compare Enable Register and/or the Preferred Source Address Compare Enable Register. Setting the EP bit of the Multicast Address Pass Enable Register inhibits compression when the address is a multicast address.

The PR port has six signals: PCLK, PDAT, $\overline{\text{PENAO}}$, $\overline{\text{PENAI}}$, $\overline{\text{PDRV}}$, and $\overline{\text{PTAG}}$. PCLK is a 10-MHz clock signal. PDAT transmits the packet data and is clocked by the rising edge of PCLK. $\overline{\text{PENAO}}$ is an active-LOW signal and indicates when the PR port is active. $\overline{\text{PENAI}}$ senses when a PR port of another IMR2 device is active and is an active-LOW signal. $\overline{\text{PDRV}}$ is used to enable an external buffer for PCLK and PDAT. $\overline{\text{PTAG}}$ indicates when the tag is being transmitted.

The signal format is shown in 4. PDAT first transmits the compressed or uncompressed packet. Then it transmits the first status field. This field has the format of the first statistics field shown in 4. At the end of the first statistics field, PCLK is stopped until the end of the packet. Then the second statistics field is transmitted over PDAT along with a new FCS.

Multiple IMR2 devices can be connected to a single MAC. If an IMR2 device becomes active while another device is transmitting statistics, the new packet will not be transmitted over the PR port.

RAUI Port

The RAUI Port is a configurable AUI port. It has the same signals that are associated with an AUI port: DO, DI, and CI. For the RAUI Port, these are named RDO, RDI, and RCI, respectively. The RAUI port can be configured in either normal or reverse mode. When configured in normal mode (default mode), the functionality is that of an AUI port on a MAC. When configured in reverse mode, the RAUI port provides the functionality of an AUI port on a MAU, with RCI acting as an output. This reverse configuration allows the RAUI Port to be connected directly to a MAC. However, the sense of RDO and RDI does not change with the configuration. Therefore, in the reverse configuration RDO should be connected to DI of the MAC and RDI should be connected to DO on the MAC.

Table 3. RAUI Port

Device Configuration Register Bit 5	RAUI Port Mode
0	Normal Mode
1	Reverse Mode (RCI is an Output)

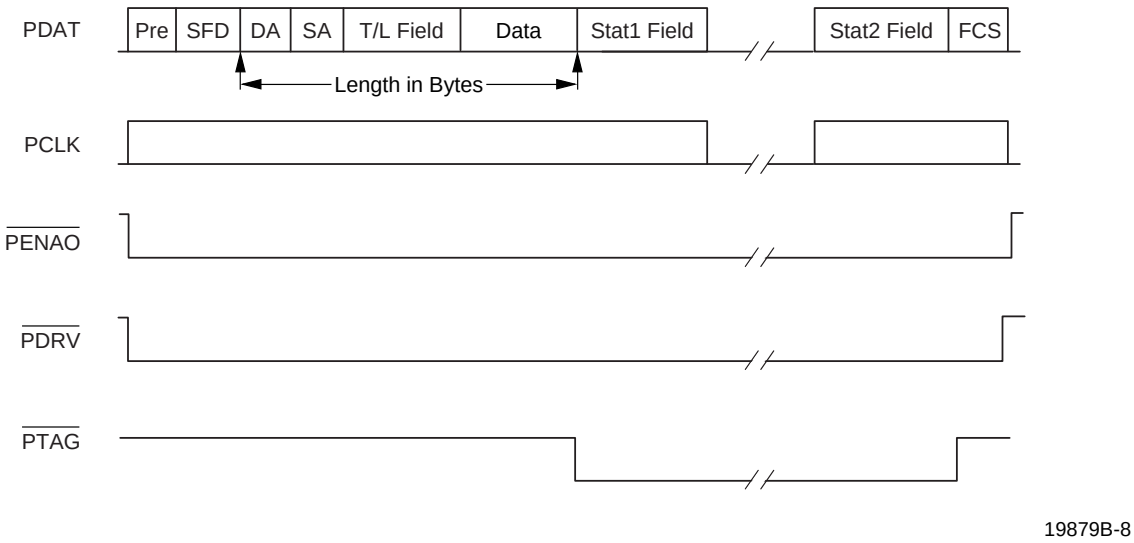


Figure 4. Packet Port Signals

Error Packet Statistics

Sample Error Status is an 8-byte 4-deep FIFO that contains statistical data on each packet having errors. The data is read in the following order:

Port Number	1 byte
Status	1 byte: FCS Error (LSB) Non-Integral Bytes Long Short Runt Data Rate Error Very Long Event (MSB)
Source Address	6 bytes

The FIFO is emptied by reading. If the FIFO is full, nothing more is recorded in Sample Error Status. If the control port is accessed, the reading starts at the beginning of the next location. If the data register is accessed after the location has been completely read, the beginning of the next location is automatically accessed.

Transceiver Interface

PAUI Ports

Packets are transferred between an IMR2 device and transceivers via twelve Pseudo AUI (PAUI) ports. The PAUI ports have the functionality of AUI ports, except that they are single-ended signals rather than differential.

QuIET Device Control and Status Data Interface

Control and status data are passed between the IMR2 device and QuIET devices via a serial data interface. Status data is on the SDATA[3:0] pins, and serial interface control is on the DIR[1:0] pins. SDATA is I/O. For interfacing with non-QuIET devices, both DIR[1] and DIR[0] are required. DIR[1:0] is used to select groups of four ports. For interfacing with QuIET devices, only DIR[1] is required.

DIR[1] controls the direction of data travel. Each SDATA pin corresponds to a QuIET device connected to a set of four specific IMR2 device ports.

Pin	Port
SDATA[0]	PAUI [3:0]
SDATA[1]	PAUI [7:4]
SDATA[2]	PAUI [11:8]

Typically, SDATA[3] is not used for a 12-port repeater. However, a QuIET device can be attached to the AUI port and the RAUI port (in normal mode) to make a 14-port repeater. The remaining two ports on the QuIET device can be connected to two ports on another IMR2 device. SDATA[3] provides the MAU management for all four ports on this QuIET device.

QuIET Device Control and Status Data Interface Operation

The interface has two modes of operation: QuIET device mode and Non-QuIET device mode. The QuIET device mode is automatically selected when a QuIET device is attached and used, and the Non-QuIET mode is selected when another type of transceiver is used. Note that it is possible for different sets of ports to use different types of transceivers.

In the QuIET device mode, DIR[1] has the following values:

DIR[1]	0	QuIET device drives SDATA with status and device ID.
	1	IMR2 device drives QuIET device with commands.

DIR[1] continually cycles. The state of DIR changes once every 50-bit times (1-bit time = 100 ns). When DIR[1] switches from 1 to 0, the QuIET device responds in the following format:

$01010A_0A_1A_2A_3B_0B_1B_2B_3C_0C_1C_2C_3D_0D_1D_2D_3S_0S_1S_2S_3$

01010	Preamble	
$A_0A_1A_2A_3$	Device ID (0000 for QuIET)	
$B_0B_1B_2B_3$	0	Link Fail
	1	Link Pass
$C_0C_1C_2C_3$	0	Received polarity is reversed.
	1	Received polarity is correct.
$D_0D_1D_2D_3$	0	No Jabber
	1	Jabber
S_n	Spares - Will be logic HIGH.	

Each character corresponds to a bit. Each bit is held for 2-bit times (200 ns). The IMR2 device uses the 01010 preamble to determine if the transceiver is a QuIET device. If any other sequence is received, the SDATA[n] pins behave as if a non-QuIET device transceiver is connected.

On the SDATA[n] pins that return the correct preamble, the IMR2 device transmits the following sequence when DIR[1] switches from 0 to 1.

$0E_0E_1E_2E_3F_0F_1F_2F_3G_0G_1G_2G_3H_0H_1H_2H_3S_0S_1S_2S_3S_4S_5S_6$

$E_0E_1E_2E_3$	Extended Distance	
	0	Disabled
	1	Enabled
$F_0F_1F_2F_3$	Link Test	
	0	Disabled
	1	Enabled
$G_0G_1G_2G_3$	Link Pulse Transmit	
	0	Disabled
	1	Enabled
$H_0H_1H_2H_3$	Reverse Received Polarity	
	0	Disabled
	1	Enabled
S_n	Spares - Will be logic HIGH.	

Control and Status for Non-QuIET Transceivers

On the SDATA[n] pins that do not return the correct preamble, the IMR2 device expects to see data corresponding to the polarity status of the port. The corresponding signals for each port on the transceiver should be connected to a 4-to-1 multiplexer with DIR utilized as the control lines. The multiplexer should behave as follows:

DIR[1:0]	Action
00	Select Transceiver 0.
01	Select Transceiver 1.
10	Select Transceiver 2.
11	Select Transceiver 3.

DIR[1:0] rotates through the $10 \rightarrow 00 \rightarrow 01 \rightarrow 11$ cycle regardless of the mode of SDATA[n]. The mode of each SDATA[n] pin can change with each cycle as transceivers are removed or inserted.

Visual Status Monitoring (LED) Support

The IMR2 device has a status port which can be connected to LEDs to facilitate visual monitoring of different repeater ports. Five port status attributes can be monitored: Carrier Sense (CRS), Collision (COLX), Partition (PART), Link Status (LINK), and Polarity (POL). The status of the ports is indicated on an 8-bit bus, LD[7:0], which is time multiplexed to show all five attributes for up to 16 ports. BSEL is the port select pin. When the select pin (BSEL) is LOW, LD[7:0] has the status of ports P7 through P0. When BSEL is HIGH, LD[3:0] has the status of P11 through P8, LD[4] has the status of the AUI port, and LD[5] has the status of the RAUI port. LD[7:6]is used to display the port status of a fourth QuIET device that optionally may be shared with another IMR2 device.

CRS, COLX, PART, LINK, and POL are the attribute select pins. When an attribute select pin is HIGH, LD[7:0] indicates the corresponding status attribute. The Status Monitoring port continually cycles as per 5. Each strobe is active for 64-bit times (6.4 μs). This allows a 10-percent duty cycle. The following table gives the value of LD[7:0] corresponding to the Attribute Select signal.

Signal	HIGH	LOW
CRS	Activity	No Activity
COLX	Collision	No Collision
PART	Connected	Partitioned
LINK	Good	None
POL	Correct	Reversed

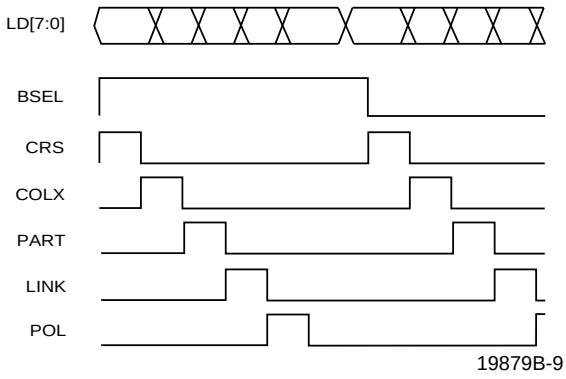


Figure 5. Visual Monitor Signals

CRS and COLX are the only valid attributes for the Expansion Bus. Therefore, when BSEL is HIGH, LD[6] has the Expansion Bus attribute for CRS and COLX.

Using AUI/RAUI for 10BASE-T Ports

The IMR2 device obtains Link and Polarity status from the serial data interface (SDATA [3:0]). When a single IMR2 device uses four QuIET devices, two of the ports on the fourth QuIET device connect to the AUI and RAUI ports of the IMR2. The two remaining ports on the fourth QuIET device connect to a second IMR2 device. Only the IMR2 device driving the serial interface to this QuIET device has Link and Polarity Status. Therefore, when BSEL is HIGH and either LINK or PART are HIGH, LD[7:6] contains Link Status or Polarity Status, respectively, of ports 2 and 3 of the fourth QuIET device.

If the AUI and RAUI ports are connected to a MAU (other than a QuIET device), LINK actually reports Loopback Error, where 1 indicates no loopback error and 0 indicates a Loopback Error. The state of POL will reflect the received polarity value on SDATA. The recommended implementation is shown in 6. The attribute select pins are connected to open-collector or open-drain inverters. The buffers connected to LD[7:0] have high-impedance outputs. They must source enough current to turn on the LEDs (typically 20 mA). CMOS devices that have a rail-to-rail output are recommended. Also, multiple open-collector inverters can be used in conjunction with multiple drives to overcome maximum current source/drain issues.

CRS and COLX signals are stretched to enhance visual recognition, i.e., they will remain active for some time even if the corresponding condition has expired. Once carrier sense is active, CRS will remain active for a minimum of 4 ms. Once a collision is detected, COLX will remain active for at least 4 ms.

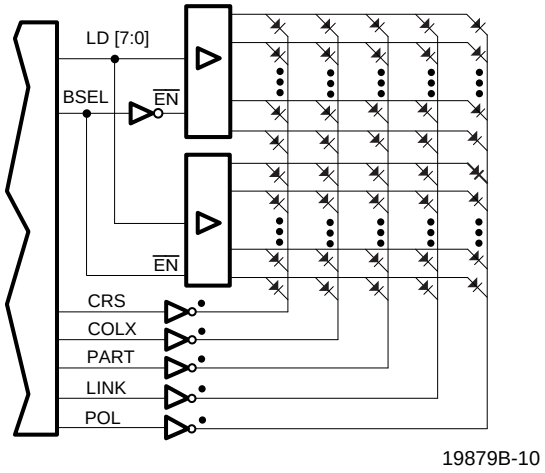


Figure 6. Visual Monitoring Application - Simplified Schematic

Intrusion Protection

The IMR2 device provides protection against intrusion, which is defined here as the unauthorized transmitting of packets onto the network.

Each port has two address registers associated with it: Last Source Address Register and Preferred Source Address Register. Unless it is locked, the Last Source Address Register contains the source address of the previous packet received by that port. The Preferred Source Address Register contains the source address that the system considers valid for that port. Both registers may be written.

If the valid address is known by the system, it may be written into both registers. If it is not known by the system, the Last Source Address Register is monitored by the system. After a packet is received by the port, the source address may be written into the Preferred Source Address Register by the system.

The Last Source Address Register may be locked. If the Last Source Address Register is locked, a mismatch between the packet's source address and the Last Source Address Register will not result in a change in the Last Source Address Register. The only way the register can be changed is by accessing it through the node processor interface. The control register for this is the Last Source Address Lock Register.

The IMR2 device provides two applicable interrupts: Source Address Changed Interrupt and Intruder Interrupt. Both interrupts can be masked on a port-by-port basis. Source Address Changed Interrupt compares the incoming packet's source address against two registers: Last Source Address Register and the Preferred Source Address Register. The interrupt is set when the source address of the incoming packet does not match both registers. Intruder Interrupt compares

the incoming packet's source address with the Preferred Source Address Register. The interrupt is set when there is a mismatch.

If the Automatic Intrusion Control register bit is set, the port is disabled if there is no match between the source address and either valid source address for that port. Valid addresses are determined from the corresponding Preferred Source Address Automatic Intrusion Control Register and Last Source Address Automatic Intrusion Control Register. The selection of these registers as valid addresses is made by the Last Source Address Compare Enable Register and the Preferred Source Address Compare Enable Register. The port is disabled after the FCS field and only if the packet is a valid packet. Once the port is disabled, it can only be enabled by the management software.

Timer Values

Descriptions and values for the various timers are as follows:

Tw1	Wait Timer for the end of transmit recovery time	10 bit times
Tw2	Wait Timer for the end of carrier recovery time	3 bit times
Tw3	Wait Timer for length of continuous output	65,536 bit times
Tw4	Wait Timer for time to disable output for Jabber Lockup Protection	96 bit times
Tw5	Wait Timer for length of packet without collision	452 to 523 bit times
Tw6	Wait Timer for excessive length of collision	2048 bit times
CC-Limit	Number of consecutive collisions which must occur before a segment (port) is partitioned	32 collisions

Microprocessor Interface

The IMR2 device implements a simple interface designed to be used by a variety of available microprocessors. The bus interface is asynchronous and can be easily adapted for different hardware interfaces.

The interface protocol is as follows:

1. Assert $\overline{CS}$ (LOW) and C/$\overline{D}$ (HIGH to access control and LOW to access data).
2. Assert $\overline{RD}$ (LOW) to start a read cycle or $\overline{WR}$ (LOW) to start a write cycle.
3. The IMR2 device forces RDY LOW in response to the leading edge of either of $\overline{RD}$ or $\overline{WR}$.

Note: *$\overline{CS}$ is internally gated with $\overline{RD}$ and $\overline{WR}$, such that $\overline{CS}$ may be permanently grounded if it is not required. A read or write cycle is started when $\overline{CS}$ and either data strobe are asserted (LOW).*

Write Cycle:

1. Data is to be placed on the Data (D[7:0]) pins prior to trailing edge of $\overline{WR}$.
2. The IMR2 device releases RDY (pulled HIGH externally), indicating that it is ready to accept the data.
3. $\overline{WR}$ strobe is de-asserted (HIGH) in response to RDY. The IMR2 device latches data internally on the rising edge of $\overline{WR}$.
4. The processor can stop driving Data pins after the rising edge of the $\overline{WR}$.

Many of the registers are two or more bytes long. In these cases, the registers are read or written into by accessing the microprocessor port with C/$\overline{D}$ LOW the same number of times as the byte size of the register.

Read Cycle:

1. The IMR2 device drives Data pins.
2. The IMR2 device releases RDY (pulled HIGH), indicating valid data.
3. De-assert $\overline{RD}$ (HIGH) in response to RDY HIGH.
4. The IMR2 device stops driving Data pins after the trailing edge of $\overline{RD}$.

The interrupt pin ($\overline{INT}$) is an open drain output. It is OFF (high impedance) upon reset, when all interrupts are disabled (masked), or when all internal sources of the interrupts are cleared. It is ON (LOW) when any of the enabled interrupts occur. Reading all the internal registers that caused the interrupt clears the internal source of the interrupt, and sets $\overline{INT}$ OFF.

Management Functions

All management functions are accessible through the microprocessor interface. The functions are divided into register banks which are subdivided into attribute registers. A register bank is selected by writing a byte with the format $000P_4P_3P_2P_1P_0$ into the C port, where P_4 through P_0 corresponds to the register bank. The desired attribute register within the selected register bank is selected by writing $111R_4R_3R_2R_1R_0$ into the C port, where R_4 through R_0 corresponds to the attribute register. Data can then be read from or written to the D port.

For registers whose contents are cleared upon reading, reading the first byte will clear the entire register. When writing to registers, all bytes must be written consecutively. If all register bytes are not written, the original contents of the register are left unchanged.

Most of the registers contain status or control information on the individual ports. These registers are each two bytes long. Each bit corresponds to an individual port. Active statistics will be maintained on the data received by DAT only if the EP bit of the Port Enable Register is set and $\overline{MACEN}$ is TRUE.

Unless otherwise indicated, the discussion of registers that are concerned with status or control on the IMR2 device will have the following format.

IMR2 Device Registers

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP/0	RAUI	AUI	P11	P10	P9	P8

Where:

P*n* refers to a PAUI port.

AUI refers to the AUI port

RAUI refers to the RAUI port

EP refers to the Expansion Bus

Unless otherwise indicated, the discussion of registers that are concerned with status or control on QuIET devices connected to the IMR2 device will have the following format.

QuIET Device Registers

D Port Read/Write

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8

Where:

TPn refers to a TP port on a QuIET device.

SPn refers to a QuIET device port connected to the AUI port or PAUI port on this device or to any port on another IMR2 device.

Note: The port on the QuIET device may be connected to a port on another IMR2 device.

Status Register

The Status Register can be accessed at any time by reading the Command Register.

The 8-bit quantity read has the following format:

C Port Read

I	E	S	X	B	M	P	L

I Interrupt. This bit reflects the state of the $\overline{INT}$ output pin. If this bit is set to 1, then this IMR2 device is driving the $\overline{INT}$ pin. Note that $\overline{INT}$ is an open drain output and that multiple devices may share the same interrupt signal.

E Transceiver Interface Changed. This bit is set if the interface to at least one SDATA input has changed from a QuIET device to a non-QuIET device or from a non-QuIET device to a QuIET device.

S Source Address Match. This bit is set if the interrupt is caused by a source address match of the incoming data packet. This bit remains set until the Source Address Match Status Register is read.

B Bit Rate Error and Partition. This bit is set if the interrupt is caused by either a bit rate error or a change in the partition status of a port.

M Source Address Change. This bit is set if the interrupt is caused by a change in the source address or a mismatch between the incoming source address and a preferred address.

P Polarity and SQE. This bit is set if the interrupt is caused by a change in the SQE test results or a polarity change.

L Link and Loopback**.** This bit is set if the interrupt is caused by a link or loopback change.

X Reserved. The values of reserved bits are indeterminate.

Register Bank 0: Repeater Registers

These registers are accessed by writing the bit pattern 0000 0000 to the C Register. The contents of all attribute counters are indeterminate upon power up.

Source Address Match Register

Address: 1110 1010

D Port Read/Write

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3								
Byte 4								
Byte 5	bit 47							bit 40
	MSB							LSB

This is a read/write register. The six bytes are read or written in LOW byte to HIGH byte order. The sequence is (re)started once the C register is programmed for access to this register. This register may be used to track nodes within a LAN by reporting the port that received a packet with a specific source address. The source address field of incoming packets is always compared with the 48-bit quantity stored in this register. The initial value of this register is indeterminate.

The IMR2 indicates a match by setting the corresponding bit in the Source Address Match Interrupt Register of the receiving port. If the Source Address Match Interrupt Enable bit is enabled, then the $\overline{INT}$ output pin is driven LOW. The set bit(s) in the Source Address Match Interrupt Registers are cleared when these registers are read.

Note: *Once the sequence is started, all six bytes have to be written or the contents do not change.*

Total Octets

Address: 1110 1100

D Port Read/Write

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

This is a 4-byte attribute register whose contents are incremented while the repeater is repeating packet data. This counter is a truncated divide by 8 of the total number of bits transmitted by the repeated (i.e., the number of whole bytes transmitted by the repeater). The counter counts the bytes on all non-collision packets with a valid Start of Frame Delimiter (SFD). The preamble is included in the count. The four bytes in this attribute are sequentially accessed by reading the D register, LSB first. Note that once the C register is programmed for access to this attribute, reading the D register port causes the value of this register to be copied into the holding register. The data is then read off the holding register, without affecting this attribute. This sequence is repeated when the last byte is read and the D register is accessed.

Transmit Collisions

Address: 1110 1101

D Port Read/Write

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

This is a 4-byte attribute whose contents are incremented each time the repeater has entered the transmit collision state from any state other than ONE PORT LEFT. The bytes are read in LOW to HIGH order by reading the Data (D) register consecutively. The sequence will be restarted once the last byte is read or the C register is reprogrammed with this register number. This causes the current value of the counter to be copied into a holding register, which is then read by accessing the D register.

Configuration Register

Address: 1111 0000

This is a read/write register. The value read is the same as that written. Unused bits are read as zeros and only zeros should be written into these bits. Do not write non-zero values into unused bits. All bits are cleared upon reset.

D Port Read/Write

I	0	S	0	0	0	0	0
MSB							LSB

I Enable Interrupts**.** When this bit is set to 0 all interrupts from this IMR2 device are masked (but not cleared) and the $\overline{INT}$ output pin is forced into inactive state (not driven).

S Source Address Match Interrupt Enable. When this bit is set, IMR2 device will generate an interrupt if the Source Address of the received packet matches that which is programmed into the Source Address Match Register.

Repeater Status

Address: 1111 1010

This is a read only register. Bit 0 is the only bit of interest. When bit 0 is set, the IMR2 device has entered MAU Jabber Lockup Protection (MJLP). The Repeater Status register is cleared by reading.

D Port Read

0	0	0	0	0	0	0	E
MSB							LSB

E	**Status**
0	No Error
1	Error

QuIET Device Transceiver ID Register

Address: 1111 1011

This is a read-only register. It contains the transceiver ID of the QuIET device connected to the IMR2 device. The 16-bit quantity has the following format:

D Port Read

	Transceiver 1				Transceiver 0			
Byte 0	M_{13}	M_{12}	M_{11}	M_{10}	M_{03}	M_{02}	M_{01}	M_{00}
	Transceiver 3				Transceiver 2			
Byte 1	M_{33}	M_{32}	M_{31}	M_{30}	M_{23}	M_{22}	M_{21}	M_{20}
	MSB							LSB

Transceiver 0	PAUI [3:0]
Transceiver 1	PAUI [7:4]
Transceiver 2	PAUI [11:8]
Transceiver 3	AUI and RAUI ports or misc.

This 16-bit register is divided into four sections. Each section is labeled M_{X3} to M_{X0} where X refers to transceivers 0 through 3. These register bits are only valid if the appropriate Transceiver Interface Status Register bit indicates that a QuIET device is connected.

M_{X3-X0}	Transceiver
0	QuIET Device ID
1 to 15	Reserved

Repeater Device and Revision Register

Address: 1111 1100

This is a read only register. The 8-bit quantity read has the following format:

D Port Read

D3	D2	D1	D0	V3	V2	V1	V0
MSB							LSB

D Device Type. These bits contain the IMR2 device code.

D3-0 0010 IMR2

V Revision Number. These bits contain the revision number. Software may interrogate these bits to determine additional features that may be available with future versions of the device.

V3-0 0000 Revision 0

Device Configuration

Address: 1111 1101

This is a read/write register. When this register is written, zeros must be written into unassigned fields. The 8-bit quantity has the following format:

D Port Read/Write

R	M	A	0	0	0	0	0
MSB							LSB

R Repeater Reset. Setting Bit R resets the registers, repeater, and MAC engine. It is the functional equivalent of hardware reset, with the exception that the microprocessor interface is not reset and the ability to access RMON and port attribute registers is maintained.

M Management Reset. Setting this bit causes the MAC engine to be reset. When the M bit is set, the IMR2 device still functions as a repeater, however MIB tracking is disabled. Setting this bit also allows the RMON registers and the attribute registers to be preset by software.

A This bit configures the RAUI port. The configuration options are:

0 Normal Mode. The RAUI port is configured as a standard AUI port.

1 Reverse Mode. RCI is an output, i.e., RCI generates a 10-MHz signal during a collision.

Register Bank 1: Interrupts

When a bit on an interrupt register is set, the interrupt bit on the Status Register is set and the $\overline{INT}$ pin is driven. These registers are accessed by writing the bit pattern 0000 0001 to the C Register. These registers are read only and are cleared to 0 upon reading. When all the interrupt registers are clear (all bits zero), the Interrupt bit of the Status Register and $\overline{INT}$ are cleared.

Note that for each interrupt register there is a corresponding interrupt enable register. The bits on the interrupt register cannot set unless the corresponding bits on the corresponding interrupt enable register are set.

Port Partition Status Change Interrupt

Address: 1110 0000

Any port changing state between partitioned and reconnected causes the appropriate register bit to be set to 1.

The format is as follows:

D Port Read

	P7	P6	P5	P4	P3	P2	P1	P0
Byte 0								
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 Partition status of corresponding port unchanged

1 Partition status of corresponding port changed

Runts with Good FCS Interrupt

Address: 1110 0001

Any port receiving a packet that is less than 64 octets (not including preamble and SFD), but is otherwise well formed and error free, causes the appropriate bit to be set. The format is as follows:

D Port Read

	P7	P6	P5	P4	P3	P2	P1	P0
Byte 0								
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI/EP 0 No runts with valid FCS

1 Runt with valid FCS

Link Status Change Interrupt

Address: 1110 0010

A change in the Link Test state of a twisted pair port associated with a repeater port (from fail to pass or pass to fail) causes the appropriate bit to be set in this register. This register is only valid when a QuIET device is connected to the corresponding port(s).

D Port Read

	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 0								
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn 0 Link Test state unchanged
1 Link Test state changed

Loopback Error Change Interrupt

Address: 1110 0011

If a port is connected to a MAU which does not loopback data from DO to DI during transmission that port has a loopback error. For the error to be detected, the network needs to be active and a packet transmitted from the port. The corresponding bit is set to 1 when the loopback error condition changes.

D Port Read

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 No loopback error change
1 Loopback error change

Polarity Change Interrupt

Address: 1110 0100

The corresponding bit is set to 1 if the polarity of the connected port is switched.

D Port Read

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn 0 Polarity unchanged
1 Polarity changed

SQE Test Error Change Interrupt

Address: 1110 0101

If a port is connected to a MAU with SQE Test enabled that port has an SQE Test Error. For the error to be detected, the network needs to be active and a packet must be transmitted from the port. The corresponding bit on the register is set when the port changes from an error state to a non-error state or from a non-error state to an error state.

D Port Read

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 No SQE Test Error change
1 SQE Test Error change

Source Address Changed Interrupt

Address: 1110 0110

The corresponding bit in the register is set when the source address of the incoming data packet matches neither the Last Source Address Register nor the Preferred Source Address Register associated with the port. The incoming packet must be an error-free packet.

D Port Read

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI/EP 0 No change
1 Source address changed on the incoming port

Intruder Interrupt

Address: 1110 0111

A bit on the Intruder Interrupt Register is set when the source address of an error-free incoming packet does not match the corresponding Preferred Source Address Register. The incoming packet must be an error-free packet.

Note: *The Preferred Address attribute is programmable and can be used to store the expected Node ID for a port. If the appropriate interrupt is also enabled, then a Source Address Changed can be used to alert the network manager of an unauthorized access. This is particularly useful for segments that are supposed to be connected to a single station.*

D Port Read

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI/EP 0 Intruder status of port unchanged
1 Intruder status of port changed

Source Address Match Interrupt

Address: 1110 1000

When the source address of an incoming packet from any port matches the Source Address Match Register, the appropriate bit is set. The received packet must be an error-free packet.

D Port Read

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI/EP 0 No match

1 Source address matches the Source Address Match Register

Note: This function is useful for mapping stations to ports in a network.

Data Rate Mismatch Interrupt

Address: 1110 1010

A bit is set when the data received by the corresponding port has caused an overflow or underflow of the FIFO. This bit is not set unless the received packet, after SFD, is at least 512 bits long and collision did not occur

D Port Read

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI/EP 0 No error

1 Data rate error

Transceiver Interface Status

Address: 1110 1111

If a QuIET transceiver is not hardware connected, the corresponding bit on the register is set.

D Port Read

X	X	X	X	Q3	Q2	Q1	Q0
MSB							LSB

QuIET 0 (Q0) PAUI [3:0]
QuIET 1 (Q1) PAUI [7:4]
QuIET 2 (Q2) PAUI [11:8]
QuIET 3 (Q3) AUI and RAUI ports

Qn 0 QuIET device is connected

1 Non-QuIET transceiver is connected

Transceiver Interface Change Interrupt

Address: 1111 0000

If the device changes from a QuIET device to another type of transceiver or from a non-QuIET device to a QuIET device, the corresponding bit on the register is set.

D Port Read

X	X	X	X	Q3	Q2	Q1	Q0
MSB							LSB

QuIET 0 (Q0)PAUI [3:0]

QuIET 1 (Q1) PAUI [7:4]
QuIET 2 (Q2) PAUI [11:8]
QuIET 3 (Q3) AUI and RAUI ports

Qn 0 No change of transceiver type

1 Change of transceiver type

Jabber Interrupt

Address: 1111 0001

A bit on this register is set if the transceiver connected to the corresponding port detects jabber.

D Port Read

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn 0 Port does not jabber

1 Port in jabber

Register Bank 2: Interrupt Control Registers

These registers are accessed by writing the bit pattern 0000 0010 to the C Register. All registers can be read from as well as written to. A set (1) control bit enables an interrupt or function of the corresponding port. All control registers are cleared upon reset. Also, all interrupts are disabled and all status bits are cleared upon hardware reset.

Partition Status Change Interrupt Enable

Address: 1110 0000

This register is used to enable or mask interrupts caused by a change in the Port Partitioning Status. Note that if this is the only cause for the interrupt, disabling an active interrupt source causes the $\overline{INT}$ output to be placed into an inactive state. Software should be designed to write zeros into unused bits.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 Partition Status Change Interrupt masked (disabled)

1 Partition Status Change Interrupt enabled

Runts with Good FCS Interrupt Enable

Address: 1110 0001

This register is used to enable or mask interrupts caused by a port receiving a packet that is less than 64 octets (not including preamble and SFD), but is otherwise well formed and error free.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI/EP
- 0 Runts with Valid FCS Interrupt masked (disabled)
- 1 Runts with Valid FCS Interrupt enabled

Link Status Change Interrupt Enable

Address: 1110 0010

Setting any of the bits in this register causes the $\overline{INT}$ pin to be driven when there is a change in the Link Test state of the corresponding port. The corresponding status bit in the Link Test State Change Register is set to 1.

D Port Read/Write

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn
- 0 Link Status Change Interrupt masked (disabled)
- 1 Link Status Change Interrupt enabled

Loopback Error Change Interrupt Enable

Address: 1110 0011

Setting a bit in this register causes an interrupt to be generated when the IMR2 device senses a change in the Loop Back Error condition on the corresponding port.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI
- 0 Loopback Error Change Interrupt masked (disabled)
- 1 Loopback Error Change Interrupt enabled

Polarity Change Interrupt Enable

Address: 1110 0100

Setting a bit in this register causes an interrupt to be generated when the polarity of the connected port is changed.

D Port Read

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn
- 0 Polarity Change Interrupt masked (disabled)
- 1 Polarity Change Interrupt enabled

SQE Test Error Change Interrupt Enable

Address: 1110 0101

Setting a bit in this register causes an interrupt to be generated when the IMR2 device senses a change in the SQE Test Error condition at a port. This occurs when an attached MAU has SQE Test enabled. A new interrupt is generated when a condition change is sensed by the IMR2 device.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI
- 0 SQE Test Error Change Interrupt masked (disabled)
- 1 SQE Test Error Change Interrupt enabled

Source Address Changed Interrupt Enable

Address: 1110 0110

This register enables interrupts caused by a mismatch between the source address of an incoming packet and either the Last Source Address Register or the Preferred Source Address Register. If Last Source Address Lock is not set and the packet is a valid packet, a mismatch between the source address and the Last Source Address Register also causes the new source address to be written into the Last Source Address Register.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI/EP
- 0 Source Address Changed Interrupt masked (disabled)
- 1 Source Address Changed Interrupt enabled

Intruder Interrupt Enable

Address: 1110 0111

This register enables interrupts to be generated when the source address of an incoming packet does not match the Preferred Source Address Register on the corresponding port. The corresponding interrupt can be interpreted as an attempt by an intruder to gain access to the network. The management system can then take appropriate action, such as disabling the corresponding port.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI
- 0 Intruder Interrupt masked (disabled)
- 1 Intruder Interrupt enabled

Multicast Address Pass Enable

Address: 1110 1001

Setting EP disables packet compression on packets with multicast addresses.

D Port Read/Write

Byte 0	0	0	0	0	0	0	0	0
Byte 1	0	EP	0	0	0	0	0	0
	MSB							LSB

EP
- 0 Packet compression on packets with multicast addresses is enabled
- 1 Packet compression on packets with multicast addresses is disabled

Note: *Zeros should be written to all register bits except the EP bit.*

Data Rate Mismatch Interrupt Enable

Address: 1110 1010

The IMR2 device can generate an interrupt if received data is outside the data rate tolerances. Setting a bit enables the Data Rate Mismatch Interrupt control of the corresponding port.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI/EP
- 0 Data Rate Mismatch Interrupt masked (disabled)
- 1 Data Rate Mismatch Interrupt enabled

Last Source Address Compare Enable

Address: 1110 1100

Setting the EP bit in this register enables a comparison of the destination address of an incoming packet to the Last Source Address Register for the expansion port. Packet compression is disabled when the destination address matches the Last Source Address Register.

D Port Read/Write

Byte 0	0	0	0	0	0	0	0	0
Byte 1	0	EP	0	0	0	0	0	0
	MSB							LSB

EP
- 0 Last Source Address Compare masked (disabled)
- 1 Last Source Address Compare enabled

Note: *Zeros should be written to all register bits except the EP bit.*

Preferred Address Compare Enable

Address: 1110 1111

Setting the EP bit in this register enables a comparison of the destination address of an incoming packet to the Preferred Address Register for the expansion port. Packet compression is disabled when the destination address matches the Preferred Address Register.

D Port Read/Write

Byte 0	0	0	0	0	0	0	0	0
Byte 1	0	EP	0	0	0	0	0	0
	MSB							LSB

EP
- 0 Preferred Source Address Compare disabled
- 1 Preferred Source Address Compare enabled

Note: *Zeros should be written to all register bits except the EP bit.*

Transceiver Interface Changed Interrupt Enable

Address: 1111 0000

When a bit is set, an interrupt is generated if the device connected to the corresponding port changes from a QuIET device to a non-QuIET device or from a non-QuIET device to a QuIET device.

D Port Read/Write

X	X	X	X	Q3	Q2	Q1	Q0	
MSB								LSB

Transceiver 0 PAUI [3:0]

Transceiver 1 PAUI [7:4]

Transceiver 2 PAUI [11:8]

Transceiver 3 AUI and RAUI ports

Qn
- 0 Device Connection Changed Test masked (disabled)
- 1 Device Connection Changed Test enabled

Jabber Interrupt Enable

Address: 1111 0001

When a bit in this register is set, an indication of jabber from a port will cause an interrupt.

D Port Read/Write

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn
- 0 Jabber Interrupt masked (disabled)
- 1 Jabber Interrupt enabled

Register Bank 3: Port Control Registers

These registers are accessed by writing the bit pattern 0000 0011 into the C register. All registers can be read from as well as written to.

Alternative Reconnection Algorithm Enable

Address: 1110 0000

The AUI Partitioning/Reconnection state machine can be programmed for the alternative reconnection algorithm (transmit only). On reset, this register defaults to the standard reconnection algorithm.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 Standard Reconnection Algorithm

1 Alternative Reconnection Algorithm

Link Test Enable

Address 1110 0010

Setting a bit in this register enables the Link Test function for the corresponding port. This is only in effect when the IMR2 device is interfaced to a QuIET device. On reset, this register defaults to Link Test Enabled.

D Port Read/Write

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn 0 Link Test Function disabled

1 Link Test Function enabled

Link Pulse Transmit Enable

Address: 1110 0011

Setting a bit in this register enables the corresponding port to transmit a Link Test Pulse. This is only in effect when the IMR2 device is interfaced to a QuIET device. On reset, this register defaults to Link Test Pulse Transmit enabled.

D Port Read/Write

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8

TPn/SPn 0 Link Test Pulse Transmit disabled

1 Link Test Pulse Transmit enabled

Automatic Receiver Polarity Reversal Enable

Address 1110 0100

Setting a bit in this register enables the QuIET device to automatically invert the receive signal following detection of the first packet with inverted polarity. This is done once after reset or link fail. On reset, this register defaults to Automatic Receiver Polarity Reversal disabled.

D Port Read/Write

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn 0 Automatic Receiver Polarity Reversal disabled

1 Automatic Receiver Polarity Reversal enabled

SQE Mask Enable

Address: 1110 0101

Setting a bit in this register allows the corresponding port to ignore activity on CI during the SQE test window following a transmission on that port. The SQE test window is defined by ANSI/IEEE 802.3, Section 7.2.2.2.4 as 6-bit times to 31-bit times following the end of the packet. Note that the SQE Mask does not affect reporting SQE tests on the SQE Status Register and the SQE Test Change Interrupt Register. On reset, this register defaults to SQE Test Mask disabled.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 SQE Test Mask disabled

1 SQE Test Mask enabled

Port Enable/Disable

Address 1110 0110

Setting a bit in this register enables the corresponding port. On reset, the ports default to enabled.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 Disable the corresponding port

1 Enable the corresponding port

Setting the EP bit will not disable the expansion bus. However, if the EP bit is not set, data carried on the expansion bus that is addressed to a MAC will not be counted in the MIB attributes.

Port Switching Control

Address: 1110 0111

Setting a bit in this register isolates the corresponding port. All input signals to the corresponding port and all information concerning port activity from the transceiver

are ignored. This feature is useful when implementing port switching. The IMR2 device connected to the QuIET device serial interface will still report correct status on the Link and Polarity LEDs. The ports default to the XENA value on reset.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 Isolate the corresponding port

1 Connect the corresponding port

Note: *If a port is isolated during an incoming or transmitted packet, repeating the packet is immediately stopped. If a port is connected during an incoming packet, the actual connection is delayed until after the end of the packet. If a port is connected while the IMR2 device is repeating a packet, the connection is made immediately.*

Extended Distance Enable

Address: 1110 1000

Setting a bit on this register lowers the input threshold on RXD of the corresponding QuIET transceiver. This allows the use of a twisted pair cable longer than 100 meters. This register is only in effect if the corresponding port is connected to a QuIET device. On reset, this register defaults to Extended Distance Option disabled.

D Port Read/Write

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn 0 Extended Distance Option disabled

1 Extended Distance Option enabled

Automatic Last Source Address Intrusion Control

Address: 1110 1001

Automatic Intrusion Control disables a port automatically when a valid packet (no errors) is received with a source address which is not a valid address for that port. Before a bit on this register is set, the corresponding Last Source Address Register should contain a valid address for that port. On reset, this register defaults to Automatic Intrusion Control with Last Source Address disabled. See note under *Automatic Preferred Source Address Intrusion Control*.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAU 0 Automatic Intrusion Control with Last Source Address disabled

1 Automatic Intrusion Control with Last Source Address enabled

Automatic Preferred Source Address Intrusion Control

Address: 1110 1010

Automatic Intrusion Control disables a port automatically when a valid packet (no errors) is received with a source address which is not a valid address for that port. Before a bit on this register is set, the corresponding Preferred Address register should contain a valid address for that port. On reset, this register defaults to Automatic Intrusion Control with Preferred Source Address disabled.

D Port Read/ Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 Automatic Intrusion Control with Preferred Source Address disabled

1 Automatic Intrusion Control with Preferred Source Address enabled

Note: *The Automatic Preferred Source Address Intrusion Control Register and the Automatic Last Source Address Intrusion Control Register work together. If intrusion on a port is not enabled on either register, intrusion control is not performed for that port. If intrusion on a port is enabled on only one of the intrusion control registers, intrusion control is based on the corresponding enabled register. If intrusion on a port is enabled on both intrusion control registers, the port is disabled if the source address fails to match both the Last Source Address Register and the Preferred Source Address Register.*

Last Source Address Lock Control

Address: 1110 1011

Whenever the source address of an incoming packet is different from the Last Source Address Register, the new source address is written into the Last Source Address Register. Setting a bit on this register disables automatic updating of the Last Source Address Register based on the last received packet. The Last Source Address Register can still be written into via the node processor interface. On reset, this register defaults to Last Source Address Lock disabled. Note that a repeater that uses Last Source Address Lock Control will not comply with IETF RFC 1516.

D Port Read/Write

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	EP	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI/EP 0 Last Source Address Lock disabled

1 Last Source Address Lock enabled

Note: *Setting a bit on this register invalidates the corresponding Source Address Changes Register.*

Register Bank 4: Port Status Registers

These registers are accessed by writing 0000 0100 to the C register.

Partitioning Status of Ports

Address: 1110 0000

These bits indicate the partition status of the corresponding ports. Ports that are partitioned will transmit packets. However, the IMR2 device will not repeat packets received by a partitioned port.

D Port Read

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 Port partitioned

1 Port connected

Link Test Status of Ports

Address: 1110 0010

The register bits indicate the Link Test Status of the corresponding ports. The bit setting is based on data received by the QuIET device. Therefore, the bit setting is invalid if a non-QuIET transceiver is used for the port.

D Port Read

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn 0 Link Test failed

1 Link Test passed

Loopback Error Status

Address: 1110 0011

When a packet is transmitted, the DO signal is looped back to the IMR2 device through the corresponding DI pins. When a bit on this register is set, data is not being looped back to the IMR2 device.

D Port Read

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 No Loopback Error

1 Loopback Error

Note: *The RAUI bit is not valid when the RAUI port is in the reverse mode.*

Receive Polarity Status

Address: 1110 0100

Each register bit represents the receive polarity status of the corresponding port. The bit setting is based on data received from the QuIET device through the serial interface. If another transceiver device is used, the bit setting reflects what is on the corresponding SDATA.

D Port Read

Byte 0	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
Byte 1	SP3	SP2	SP1	SP0	TP11	TP10	TP9	TP8
	MSB							LSB

TPn/SPn 0 Polarity correct

1 Polarity reversed

SQE Test Status

Address: 1110 0101

These register bits reflect the status of the last packet received from the corresponding port. The RAUI bit is not valid when the RAUI port is in the reverse mode.

D Port Read

Byte 0	P7	P6	P5	P4	P3	P2	P1	P0
Byte 1	0	0	RAUI	AUI	P11	P10	P9	P8
	MSB							LSB

Pn/AUI/RAUI 0 No SQE Test Error

1 SQE Test Error

Register Bank 5: RMON Registers

The RMON registers can be accessed by writing to address 0000 0101 and then accessing the individual registers. The RMON registers are 32-bit counters and comply with etherStatsEntry of the statistics group of the RMON MIB (RFC 1757) or etherHistoryEntry of the History group of RFC 1757. They are 4 bytes long and are read low order byte to high order byte.

The RMON registers can usually only be read. However, they can be written to when the Repeater Reset bit or the Management Reset bit on the Device Configuration Register is set.

etherStatsOctets

Address: 1110 0000

The value in this register represents the total number of octets received (excluding preamble bits, but including FCS bits) by the IMR2 device.

etherStatsPkts

Address: 1110 0001

The value in this register represents the total number of packets received by the IMR2 device.

etherStatsBroadcastPkts

Address: 1110 0010

The value in this register represents the total number of valid packets received that were addressed to a broadcast address.

etherStatsMulticastPkts

Address: 1110 0011

The value in this register represents the total number of valid packets received that were addressed to a multicast address.

etherStatsCRCAlignErrors

Address: 1110 0100

The value in this register represents the total number of packets received that were between 64 and 1518 octets, inclusive, and had either FCS errors or alignment errors.

etherStatsUndersizePkts

Address: 1110 0101

The value in this register represents the total number of packets received that were less than 64 octets long, but were otherwise error free.

etherStatsOversizePkts

Address: 1110 0110

The value in this register represents the total number of packets received that were greater than 1518 octets long, but were otherwise error free.

etherStatsFragments

Address: 1110 0111

The value in this register represents the total number of packets received that were less than 64 octets long, not including the preamble or SFD, and had either an FCS error or an alignment error.

etherStatsJabbers

Address: 1110 1000

The value in this register represents the total number of packets that were greater than 1518 octets long and had either FCS errors or alignment errors.

Note: *This differs from the IEEE definition of Jabber.*

etherStatsCollisions

Address: 1110 1001

The value in this register represents the total number of collisions on the IMR2 device.

etherStats64Octets

Address: 1110 1010

The value in this register represents the total number of packets (including error packets) that were 64 octets long.

etherStats65to127Octets

Address: 1110 1011

The value in this register represents the total number of packets (including error packets) that were 65 octets to 127 octets long inclusive.

etherStats128to255Octets

Address: 1110 1100

The value in this register represents the total number of packets (including error packets) that were 128 octets to 255 octets long inclusive.

etherStats256to511Octets

Address: 1110 1101

The value in this register represents the total number of packets (including error packets) that were 256 octets to 511 octets long inclusive.

etherStats512to1023Octets

Address: 1110 1110

The value in this register represents the total number of packets (including error packets) that were 512 octets to 1023 octets long inclusive.

etherStats1024to1518Octets

Address: 1110 1111

The value in this register represents the total number of packets (including error packets) that were 1024 octets to 1518 octets long inclusive.

Activity

Address: 1111 0000

The value in this register represents the total number of octets that were active on the IMR2 device.

Register Bank 7: Management Support

These registers control packet compression and error sampling. The Management Support Registers can be accessed by writing 0000 0111 to the C Register and then writing the register address to the C Register.

Device ID

Address: 1110 0000

The Device ID Register is a read/write register. It is an 8-bit register and contains the assigned ID number of the IMR2 device. This number is transmitted as part of the tag field by the Packet Report Port.

Sample Error Status

Address: 1110 0010

Sample Error Status gives statistical data on packets that have errors. It is a 4-deep 8-byte FIFO. Each read requires accessing the data register eight times. The access can jump to the next level of the FIFO in the middle of a read by writing any value to the node processor port with the C/$\overline{D}$ pin HIGH. If the node processor port is accessed (with the C/$\overline{D}$ pin LOW) after the last byte is read,

the register jumps to the next level automatically. The data format is as follows:

D Port Read/Write

Byte 0	E	0	0	0	N3	N2	N1	N0
Byte 1	0	VL	DRE	RNT	S	L	A	FCS
Byte 2	bit 23							bit 16
Byte 3								
Byte 4								
Byte 5								
Byte 6								
Byte 7	bit 63							bit 56
	MSB							LSB

E Packet 0 - Empty
1 - Valid
N3-0 Port Number
VL Very Long Event
DRE Data Rate Error
RNT Runt Packet
S Short Event
L Long Event
A Alignment Error
FCS FCS Error
Bytes 2-7 Source Address. It is read low order byte to high order byte.

Note: *The FIFO is emptied by reading. If the FIFO is full, nothing more is recorded in Sample Error Status. If the FIFO is empty (bit E = 0), there is nothing in the remaining 7 bytes; therefore, the next access will be the first byte of the 8-byte register.*

Report Packet Size

Address: 1110 0011

Report Packet Size is a two-byte register. The eleven least significant bits are used. It sets the length of the original packet (in octets) that is transmitted over the Packet Report Port. The LS Byte is accessed first. The limits are 14 bytes (binary 000000001110) and 1535 bytes (binary 10111111111). If the register is set at less than 14, 14 bytes of the original packet are transmitted over the Packet Reports Port. If the register is set at greater than 1535 bytes, all of the original packet is sent over the Packet Report Port.

D Port Read/Write

Byte 0	bit 7							bit 0
Byte 1	bit 15							bit 8
	MSB							LSB

STATS Control

Address: 1110 0100

STATS Control is a 1-byte register. It sets the operation of the Packet Report Port and the RAUI port.

D Port Read/Write

0	T	F	0	0	0	0	0
MSB							LSB

T 0 Packet tagging is disabled
1 Packet tagging is enabled

F 0 Appending of a new FCS during port tagging is disabled
1 Appending of a new FCS during port tagging is enabled

Register Banks 16 through 30: Port Attribute Registers

Port Attribute registers are accessed by writing the appropriate port number into the C register, followed by the attribute number. The table below shows the corresponding register bank for each port.

Register Bank Access	Port
0001 0000	0
0001 0001	1
0001 0010	2
0001 0011	3
0001 0100	4
0001 0101	5
0001 0110	6
0001 0111	7
0001 1000	8
0001 1001	9
0001 1010	10
0001 1011	11
0001 1100	AUI
0001 1101	RAUI
0001 1110	Expansion Bus (activity recorded when $\overline{\text{MACEN}}$ is TRUE)

Except for the Last Source Address Register and the Preferred Source Register, all registers are four bytes long and read only unless special conditions are met. The Last Source Address Register and the Preferred Source Address Register are six bytes long and their contents can be written and read.

Once the C Register is programmed with a valid port and attribute number, the corresponding attribute is transferred to a holding register upon reading the first byte. Subsequent accesses to the D register access the value in a least significant to most significant byte order. During a read, once the last byte is read, the attribute value is re-transferred to the holding register and the sequence can be restarted.

When writing the Last Source Address Register and the Preferred Source Register, if the sequence is aborted prior to the 6th consecutive write cycle, the register value is not altered. The sequence (read or write) may be aborted and restarted by programming the C register.

The contents of all attribute registers are maintained during hardware or software reset.

These attributes and their definitions comply with the IEEE 802.3 Repeater Management standard, Section19 (*Layer Management for 10 Mb/s Baseband Repeaters)*. A brief description of attributes is included here for reference only. For more details refer to the IEEE document. An IMR2-based hub can be designed that will comply with IETF RFC 1515 and RFC 1516.

The Port Attribute Registers can be written into if one of two conditions are met. The first is when either the M bit or the R bit on the Device Configuration Register is set. The second is when the corresponding port is disabled.

Readable Frames

Address: 1110 0000

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Readable Frames is a read-only attribute that counts the number of valid frames detected by the port. Valid frames are from 64 bytes to 1518 bytes in length, have a valid frame CRC, and are received without a collision. This attribute is a 32-bit counter with a minimum roll-over time of 80 hours.

Readable Octets

Address: 1110 0001

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Readable Octets is a read-only attribute that counts the number of octets received on each port. This number is determined by adding the frame length to this register at the completion of every valid frame. This attribute is a 32-bit counter with a minimum rollover time of 58 minutes.

Frame Check Sequence (FCS) Errors

Address: 1110 0010

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

FrameCheckSequence (FCS) Errors is a read-only attribute that counts the number of frames detected on each port with an invalid frame check sequence. This counter is incremented on each frame of valid length (64 bytes to 1518 bytes) that does not suffer a collision during the frame. This counter is incremented on each invalid frame. However, it is not incremented for frames with both framing errors and frame check sequence errors. This attribute is a 32-bit counter with a minimum rollover time of 80 hours.

Alignment Errors

Address: 1110 0011

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Alignment Errors is a read-only attribute that counts the number of frames detected on each port with an FCS error and a framing error. This counter is incremented on each frame of valid length (64 bytes to 1518 bytes) that does not suffer a collision during the frame. Frames that have both framing errors and FCS errors are counted by this attribute, but not by the Frame Check Sequence Errors attribute. This attribute is a 32-bit counter with a minimum rollover time of 80 hours.

Frames Too Long

Address: 1110 0100

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Frames Too Long is a read-only attribute that counts the number of frames that exceed the maximum valid packet length of 1518 bytes. This attribute is a 32-bit counter with a minimum rollover time of 61 days.

Short Events

Address: 1110 0101

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Short Events is a read-only attribute that counts the number of instances where activity is detected with a duration less than the ShortEventMaxTime (74-82 bit times). This attribute is a 32-bit counter with a minimum rollover time of 16 hours.

Runts

Address: 1110 0110

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Runts is a read-only attribute that counts the number of instances where activity is detected with a duration greater than the ShortEventMaxTime (74-82 bit times, but less than the minimum valid frame time (512-bit times, or 64 bytes). This attribute is a 32-bit counter with a minimum rollover time of 16 hours.

Note: *Runts usually indicate collision fragments, a normal network event. In certain situations associated with large diameter networks, a percentage of runts may exceed ValidPacketMinTime.*

Collisions

Address: 1110 0111

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Collisions is a read-only attribute that counts the number of instances where a carrier is detected on the port, and a collision is detected. This attribute is a 32-bit counter with a minimum rollover time of 16 hours.

Late Events

Address: 1110 1000

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Late Events is a read-only attribute that counts the number of instances where a collision is detected after the LateEventThreshold (480-565 bit times) in the frame. This event will be counted both by the Late Events attribute, as well as the Collisions attribute. This attribute is a a 32-bit counter with a minimum rollover time of 81 hours.

Very Long Events

Address: 1110 1001

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Very Long Events is a read-only attribute that counts the number of times the transmitter is active in excess of the MAU Jabber Lockup Protection (MJLP) Timer (4 ms - 7.5 ms). This attribute is a 32-bit counter with a minimum rollover time of 198 days.

Data Rate Mismatches

Address: 1110 1010

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Data Rate Mismatches is a read-only attribute that counts the number of occurrences where the frequency or data rate of the incoming signal is detectably different from the local transmit frequency. To be counted, the incoming packet must be at least 512 bytes and not in collision. The attribute is a 32-bit counter with a minimum rollover time of 80 hours.

Note: *The rate at which the Data Rate Mismatches attribute will increment will depend on the magnitude of the difference between the received signal clock and the local transmit frequency.*

Auto Partitions

Address: 1110 1011

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Auto Partitions is a read-only attribute that counts the number of instances where the repeater has partitioned this port from the network. This attribute is a 32-bit counter that is incremented on each such event. The approximate minimum time between counter rollovers is 20 days.

Source Address Changes

Address: 1110 1100

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

Source Address Changes is a read-only attribute that counts the number of times the source address field of valid frames received on a port changes. This attribute is a 32-bit counter with a minimum rollover of 81 hours.

Note: *This may indicate whether a link is connected to a single DTE or another multi-user segment.*

Readable Broadcast Frames

Address: 1110 1101

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

The counter is incremented by one each time this port receives an error-free broadcast frame.

Last Source Address

Address: 1110 1110

D Port Read/Write

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3								
Byte 4								
Byte 5	bit 47							bit 40
	MSB							LSB

Last Source Address is a read/write attribute and is the source address of the last readable frame received by this port.

This 6-byte register may be read from or written to. This feature allows the software to preset this attribute to the known Node ID for a single node segment. A change in the contents of this register would then signal an anomaly. This will cause the Source Address Changes attribute to increment. Furthermore, setting the respective PAUI/AUI/RAUI Port Source Address Change Interrupt Enable bit (in the Port Control Registers) can be used to generate a hardware interrupt to signal the software to automatically disable this port.

Readable Multicast Frames

Address: 1110 1111

D Port Read

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3	bit 31							bit 24
	MSB							LSB

The counter is incremented by one each time this port receives an error-free multicast frame. Broadcast frames are not counted.

Preferred Source Address

Address: 1111 0000

D Port Read/Write

Byte 0	bit 7							bit 0
Byte 1								
Byte 2								
Byte 3								
Byte 4								
Byte 5	bit 47							bit 40
	MSB							LSB

The address programmed into this register is compared with the incoming source address to generate a Source Address Changed Interrupt. This is a 6-byte word. The operation will abort if all 6 bytes are not written.

SYSTEM APPLICATIONS

IMR2 to QuIET Connection

The IMR2 device provides a system solution to designing repeaters. It can be used with the QuIET transceivers to design 10BASE-T hubs or with other types of MAUs for 10BASE2 or 10BASE-FL hubs. The MAU types can be mixed to design a hub that supports multiple media types. The IMR2 device connects directly to the QuIET device transceivers. 7 shows the simplified connection. Three QuIET devices may be connected to a single IMR2 device for 12 ports. Only one connection is shown for simplicity.

Other Media

The IMR2 device, with some supporting circuitry, can be connected to the AUI port of any MAU device. Thus, it can support 10BASE2 and 10BASE-FL. The example in 8 shows a PAUI port connected to a 10BASE-FL transceiver (ml4663). For the ml4663, signals TX, RX, and COL are equivalent to the AUI signals DO, DI, and CI. The 360–Ω resistors are required by the ml4663 drivers.

MAC Interface

The IMR2 device can be connected to a MAC using either the RAUI port or the PR port. The RAUI port supports a direct connection. The PR port requires some glue logic.

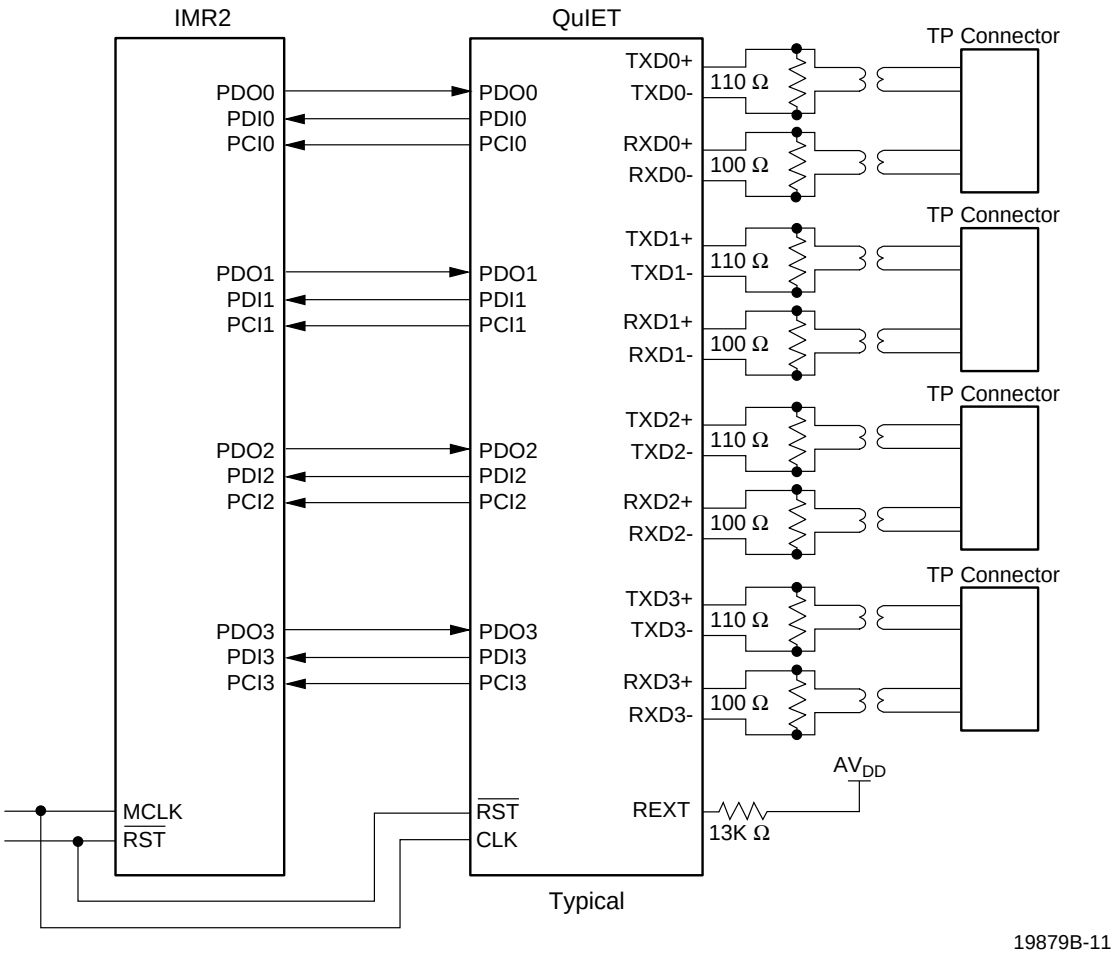
RAUI Port

When the RAUI port is to be connected to a MAC, it should be configured in reverse mode and connected as shown in 9 (a). Notice that RDI is connected to DO of the MAC and RDO is connected to DI. This is because the reverse configuration only affects RCI. 9 (b) shows the normal AUI configuration for reference.

PR Port Configuration

The PR port may be connected to the GPSI port of a MAC. Communication with the MAC involves both the PR port and the Expansion Bus. The PR port connects to the receive side of the MAC and the expansion bus connects to the transmit side.

An example of the MAC connection is shown in 10. Here the IMR2 device is connected to the SIA interface of the Am79C90 (C-LANCE). $\overline{\text{MACEN}}$, DAT, and ECLK are bus signals. Therefore, the AND gates and buffers to these signals must be open-collector or open-drain. The OR gate for RENA satisfies the loopback requirements for the C-LANCE.



***Note**: Common mode chokes may be required.*

Figure 7. Simplified 10BASE-T Connection

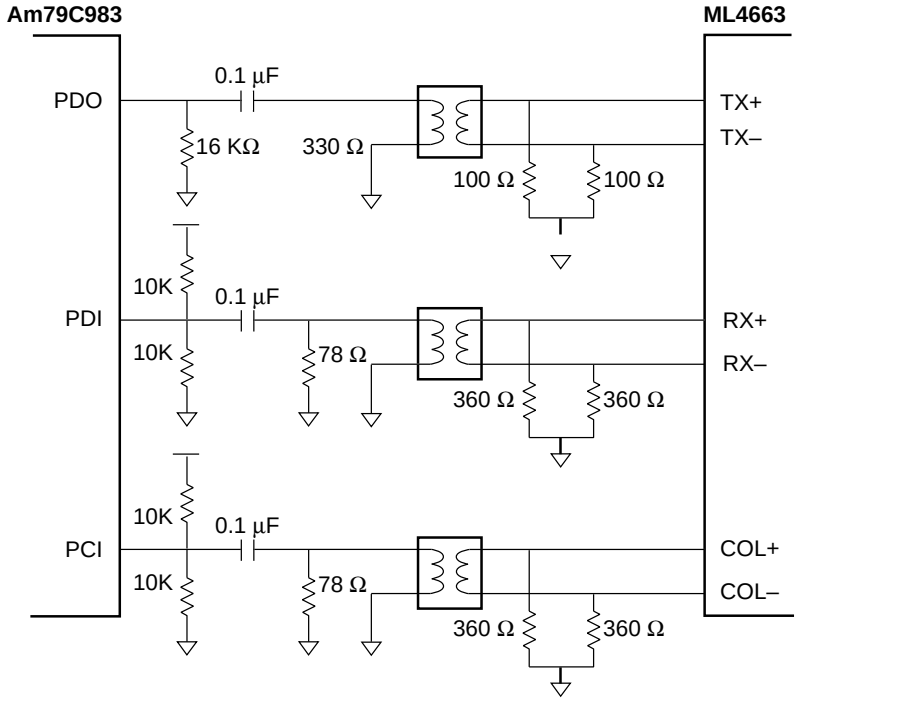


Figure 8. PAUI Interface to non-QuIET Device Transceiver

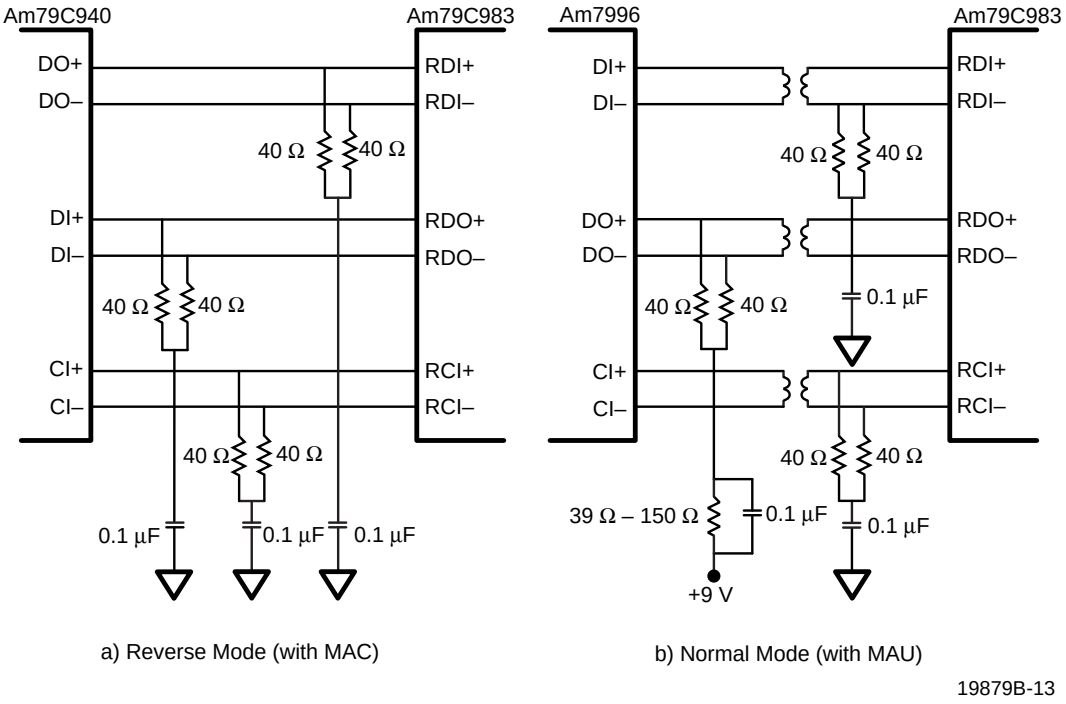


Figure 9. RAUI Port Interconnections

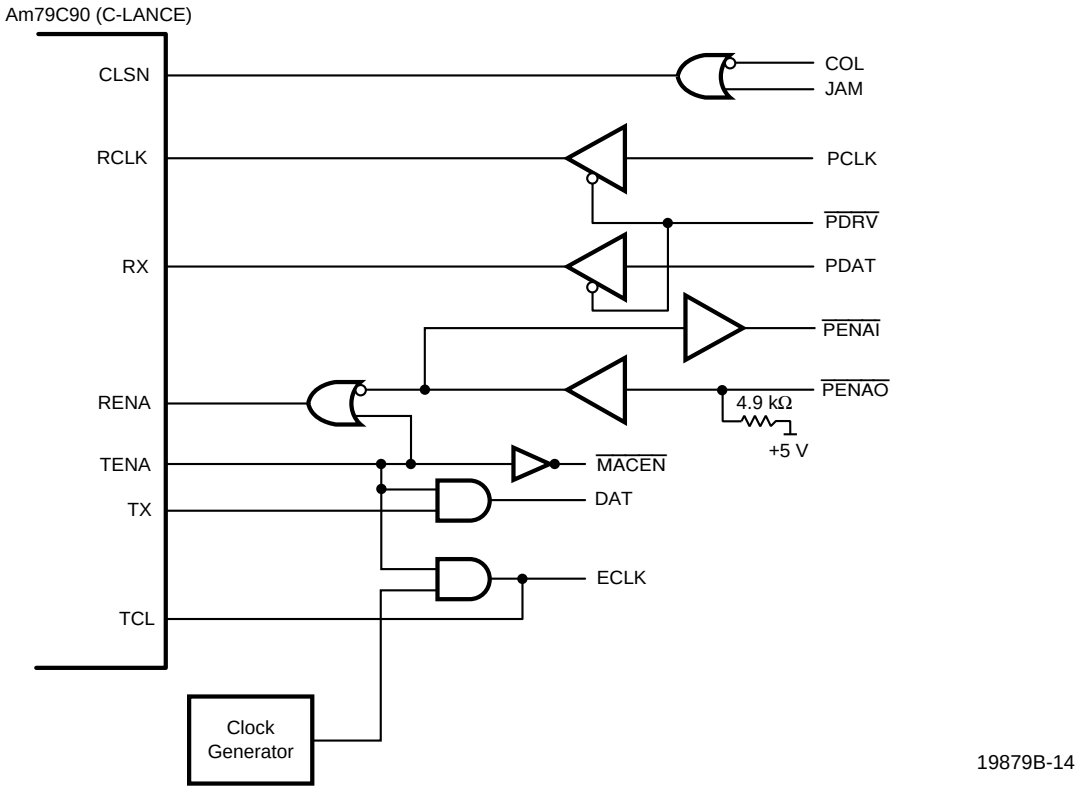


Figure 10. PR Port Connection to an Am79C90 C-Lance

Port Switching

Port switching allows the movement of individual ports between multiple Ethernet collision domains via software. This capability enables the network manager to optimize network performance by dynamically balancing the loads on a network. As an example, a port exhibiting a high level of activity can be moved to a less congested collision domain.

The method of implementing port switching with the IMR2/QuIET chip set is to connect a single transceiver port to multiple IMR2 devices. The number of IMR2 devices will equal the number of backplanes supported in the hub. 11 is a simplified schematic showing a hub with three separate backplanes. Only one QuIET device is shown for simplicity, although it is expected that most applications will use three QuIET devices to enable 12 port multiples.

The following discussion of port switching will consider only port 0; although, it is equally applicable to all of the ports. At any time, PAUI[0] is enabled on one, and only one, IMR2 device. As a result, port 0 is transferred to whichever IMR2 device has PAUI[0] enabled.

The other two IMR2 devices will have PAUI[0] disabled with PDO[0] in a high impedance state. To move port 0 to another backplane, the software will disable PAUI[0] on the active IMR2 device and enable PAUI[0] on the targeted IMR2 device that represents the desired backplane. Pseudo AUI ports can be disabled or enabled by setting the appropriate bit in the Port Switching Control Register.

Although there are multiple IMR2 devices, only one has management control of the QuIET devices. 11 shows IMR2 device 0 having management control. The other two devices do not have any control over the configuration of the QuIET devices.

The number of IMR2 devices that can be connected together is limited by the load on the PAUI drivers. The PAUI will operate reliably with a load up to 100 pF. On a system that uses sockets for the IMR2 devices, the maximum number of devices is six. This number can increase as long as the total load capacitance is kept below 100 pF.

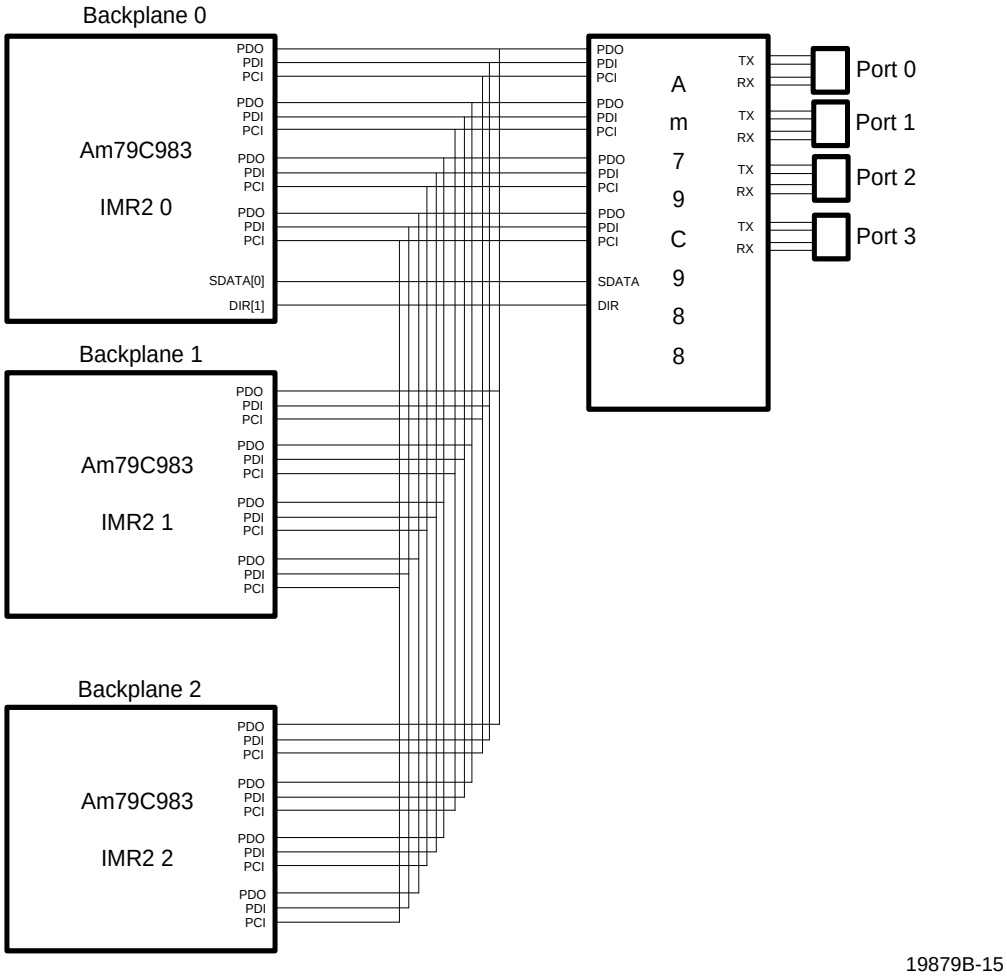


Figure 11. Port Switching Configuration

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . –65°C to +150°C

Ambient Temperature Under Bias. . . . . 0 to 70°C

Supply Voltage referenced to

AV_{SS} or DV_{SS} (AV_{DD}, DV_{DD}) . . . . . .–0.3 to +6V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (TA) . . . . . .0°C to + 70° C

Supply Voltages (V_{DD}) . . . . . +5 V ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Digital I/O					
V_{IL}	Input LOW Voltage	-	-0.5	0.8	V
V_{IH}	Input HIGH Voltage	-	2.0	0.5+V_{DD}	V
V_{OL}	Output LOW Voltage	I_{OL}=4.0 mA	-	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} =-0.4 mA	2.4	-	V
I_{IL}	Input Leakage Current	0<V_{IN} <V_{DD}	-	10	µA
V_{OLOD}	Open Drain Output LOW Voltage	I_{OLOD} = 12 mA	-	0.4	V
(R)AUI Ports					
I_{AIXD}	Input Current at DI± and CI ±	V_{SS}<V_{IN}<V_{DD}	-500	500	µA
V_{AICM}	DI±, CI± Open Circuit Input Voltage Range	I_{IN} = 0	V_{DD}-3	V_{DD}-1	V
V_{AIDV}	Differential Mode Input Voltage Range	V_{DD} = 5.0V	-2	+2	V
V_{ASQ}	DI, CI Squelch Threshold	-	-350	-160	mV
V_{AOD}	Differential Output Voltage |(DO+) -(DO)|	R_L = 78Ω	620	1100	mV
V_{AOC}	Differential Output Voltage |(RCI+)-(RCI-)| (Reverse Mode)	R_L = 39Ω	620	1100	mV
V_{AODI}	DO Differential Output Voltage Imbalance	R_L = 78Ω	-25	+25	mV
V_{AOD}OFF	DO Differential Idle Output Voltage	R_L = 78Ω	-40	+40	mV
I_{AOD}OFF	DO Differential Idle Output Current	R_L = 78Ω (Note 1)	-525	+525	µA
V_{AOCM}	DO+, DO- Output Voltage	R_L = 78Ω	2.5	V_{DD}	V
PAUI Ports					
V_{IDLE}	Idle Voltage	-	V_{DD}/2-10%	V_{DD}/2+10%	mV
V_{POH}	Output HIGH Voltage	-	V_{IDLE} + 0.45		mV
V_{POL}	Output LOW Voltage	-		V_{IDLE} - 0.45	mV
V_{PIH}	Input HIGH Voltage	(Note 1)	V_{IDLE} + 0.45		mV
V_{PIL}	Input LOW Voltage	(Note 1)	V_{IDLE} - 0.45		V
I_{PIL}	Input Leakage Current	V_{DD} = MAX		10	µA
v_{PASQ}	PDI & PCI Squelch (the value PDI & PCI must go to before internal PDI & PCI carrier sense can be turned on) (Note 11)	-	V_{IDLE} -550	V_{IDLE} -350	mV
Power Supply Current					
I_{DD}	Power Supply Current (Idle)	MCLK = 20 MHz V_{DD} = +5.25V	-	300	mA
	Power Supply Current (Transmitting)	MCLK = 20 MHz V_{DD} = +5.25V	-	450	mA

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Clock and Reset Timing					
tMCLK	MCLK Clock Period		49.995	50.005	ns
tMCLKH	MCLK Clock HIGH		20	30	ns
tMCLKL	MCLK Clock LOW		20	30	ns
tMCLKR	MCLK Rise Time		-	10	ns
tMCLKF	MCLK Fall Time		-	10	ns
tECLKH	ECLK HIGH	(Note 2)	0.4 tECLK	0.6 tECLK	ns
tECLKL	ECLK LOW	(Note 2)	0.4 tECLK	0.6 tECLK	ns
tECRR	ECLK Rise Time (When Receiving DAT)	(Note 1)	-	10	ns
tECRF	ECLK Fall Time (When Receiving DAT)	(Note 1)	-	10	ns
tECTR	ECLK Rise Time (When Transmitting DAT)	(Note 1)	-	10	ns
tECTF	ECLK Fall Time (When Transmitting DAT)	(Note 1)	-	10	ns
tRST	Reset Pulse Width		4	-	µs
tRSTP	Reset Pulse Width on Power-Up		150	-	µs
tRSTSET	Reset Input Setup Time with respect to MCLK		20	-	ns
tRSTHLD	Reset Input Hold Time with respect to MCLK		0	-	ns
(R)AUI Port Timing					
tDOTD	MCLK HIGH to DO Toggle		-	30	ns
tDOTR	DO Rise Time	(Note 1)	-	7.0	ns
tDOTF	DO Fall Time	(Note 1)	-	7.0	ns
tDORM	DO+, DO- Rise and Fall Time Mismatch		-	1.0	ns
tDOETD	DO End Of Transmission		275	375	ns
tPWODI	DI Pulse Width Accept/Reject	$\|V_{IN}\|>\|V_{ASQ}\|$ (Note 3)	15	45	ns
tPWKDI	DI Pulse Width Not to Turn Off Internal Carrier Sense	$\|V_{IN}\|>\|V_{ASQ}\|$ (Note 4)	136	220	ns
tPWOCI	CI Pulse Width Accept/Reject Threshold	$\|V_{IN}\|>\|V_{ASQ}\|$ (Note 5)	8	26	ns
tPWKCI	CI Pulse Width Not to Turn Off Threshold	$\|V_{IN}\|>\|V_{ASQ}\|$ (Note 6)	80	160	ns
tCITR	RCI Rise Time (in Reverse Mode)	(Note 1)	-	7.0	ns
tCITF	RCI Fall Time (In Reverse Mode)	(Note 1)	-	7.0	ns
tCIRM	RCI+, RCI- Rise and Fall Time Mismatch (RAUI in Reverse Mode)		-	1.0	ns
PAUI Port Timing					
tPDOTD	MCLK HIGH to DO Toggle		-	30	ns
tPDOETD	PDO End of Transmission	(Note 1)	275	375	ns
tPWOPDI	PDI Pulse Width Accept/Reject (Note 7)	$\|V_{IN}\|>\|V_{ASQ}\|$	15	45	ns
tPWKPDI	DI Pulse Width Not to Turn Off Internal Carrier Sense (Note 8)	$\|V_{IN}\|>\|V_{ASQ}\|$	136	220	ns
tPWOPCI	CI Pulse Width Accept/Reject Threshold (Note 9)	$\|V_{IN}\|>\|V_{ASQ}\|$	8	26	ns
tPWKPCI	CI Pulse Width Not to Turn Off Threshold (Note 10)	$\|V_{IN}\|>\|V_{ASQ}\|$	80	160	ns
Expansion Bus Timing					
tMHRL	MCLK HIGH to $\overline{REQ}$ Driven LOW	C_L=100pF	10	40	ns
tMHRH	MCLK HIGH TO $\overline{REQ}$ Driven HIGH	C_L=100pF	10	40	ns

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
tMHDR	MCLK HIGH to DAT/JAM Driven	C_L=100pF	10	40	ns
tMHDZ	MCLK HIGH TO DAT/JAM Not Driven	C_L=100pF	14	40	ns
tMDSET	DAT/JAM Setup Time to MCLK		10	-	ns
tMDHOLD	DAT/JAM Hold Time from MCLK		10	-	ns
tMASET	$\overline{COL}$/$\overline{ACK}$ Setup Time to MCLK		5	-	ns
tMAHLD	$\overline{COL}$/$\overline{ACK}$ Hold Time to MCLK		14	-	ns
tELDR	ECLK LOW to DAT Switching	C_L=100pF	-	20	ns
tEDSET	DAT Setup to ECLK		10	-	ns
tEDHOLD	DAT Hold Time from ECLK		14	-	ns
Microprocessor Interface Timing					
tCDS	C/$\overline{D}$ Setup Time with Respect to $\overline{RD}$/$\overline{WR}$ Leading Edge		10	-	ns
tCDH	C/$\overline{D}$ Hold Time with Respect to $\overline{RD}$/$\overline{WR}$ Rising Edge		0	-	ns
tCSS	$\overline{CS}$ Setup Time with Respect to $\overline{RD}$/$\overline{WR}$ Falling Edge		10	-	ns
tCSH	$\overline{CS}$ Hold Time with Respect to $\overline{RD}$/$\overline{WR}$ Rising		0	-	ns
tRDYD	RDY Leading Edge Delay	C_L=100pF	-	25	ns
tRDYH	RDY HIGH to $\overline{RD}$/$\overline{WR}$ Rising		0	-	ns
tDOUT	Data Out to RDY HIGH	C_L=100pF	50	-	ns
tDOH	Data Out HOLD after $\overline{RD}$ HIGH	C_L=100pF	10	50	ns
tDIS	Data In Setup Time with Respect to $\overline{WR}$ Rising Edge		25	-	ns
tREST	Rest Period between MPI Operations (Time between the Earliest $\overline{CS}$/$\overline{RD}$/$\overline{WR}$ Going HIGH to the Next $\overline{CS}$/$\overline{RD}$/$\overline{WR}$ Going LOW, whichever is the Latest		150	-	ns
tDIH	Data In HOLD after $\overline{WR}$ HIGH		0	-	ns
Management Port Timing					
tMSSO	MCLK to SDATA		10	40	ns
tMSDO	MCLK to DIR[1:0]		10	40	ns
tMSSSU	SDATA Setup Time		10	-	ns
tMSSHD	SDATA Hold Time		10	-	ns
Packet Report Port Timing					
tPRV	PCLK LOW to PDAT Switching		-	20	ns

Notes:

1. *Parameter is not tested.*
2. *ECLK is dependent on the frequency of the data on the active port.*
3. *(R)DI pulses narrower than tPWODI (min) will be rejected; (R)DI pulses wider than tPWODI (max) will turn internal (R)DI carrier sense on.*
4. *(R)DI pulses narrower than tPWKDI (min) will maintain internal (R)DI carrier sense on; (R)DI pulses wider than tPWKDI(max) will turn internal (R)DI carrier sense off.*
5. *(R)CI pulses narrower than tPWOCI (min) will be rejected; (R)CI pulses wider than tPWOCI (max) will turn internal (R)CI carrier sense on.*
6. *(R)CI pulses narrower than tPWKCI (min) will maintain internal (R)CI carrier sense; (R)CI pulses longer than tPWKCI (max) will turn internal (R)CI carrier sense off.*
7. *PDI pulses narrower than tPWOPDI (min) will be rejected; PDI pulses wider than tPWOPDI (max) will turn internal PDI carrier sense on.*

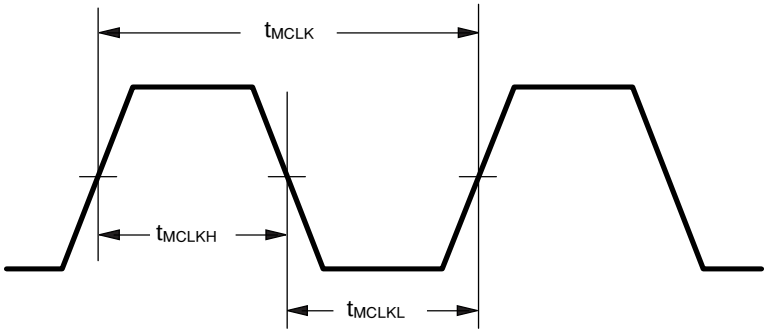
8. *PDI pulses narrower than tPWKPDI (min) will maintain internal PDI carrier sense on; PDI pulses wider than tPWKPDI (max) will turn internal PDI carrier sense off.*
9. *PCI pulses narrower than tPWOPCI (min) will be rejected; PCI pulses wider than tPWOPCI (max) will turn internal PCI carrier sense on.*
10. *PCI pulses narrower than tPWKPCI (min) will maintain internal PCI carrier sense on; PCI pulses wider than tPWKPCI (max) will turn internal PCI carrier sense off.*
11. *Squelch thresholds change proportionately with V_{DD}.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

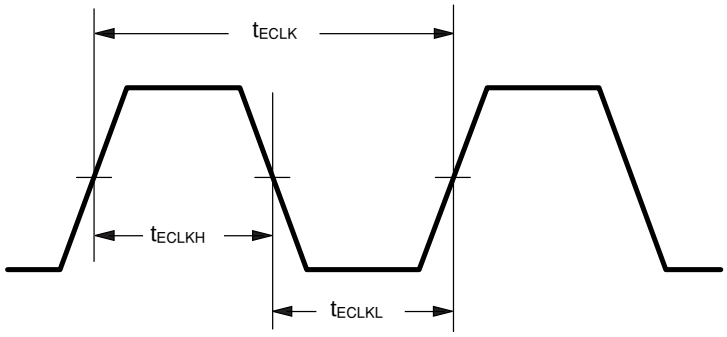
KS00010

SWITCHING WAVEFORMS



19879B-16

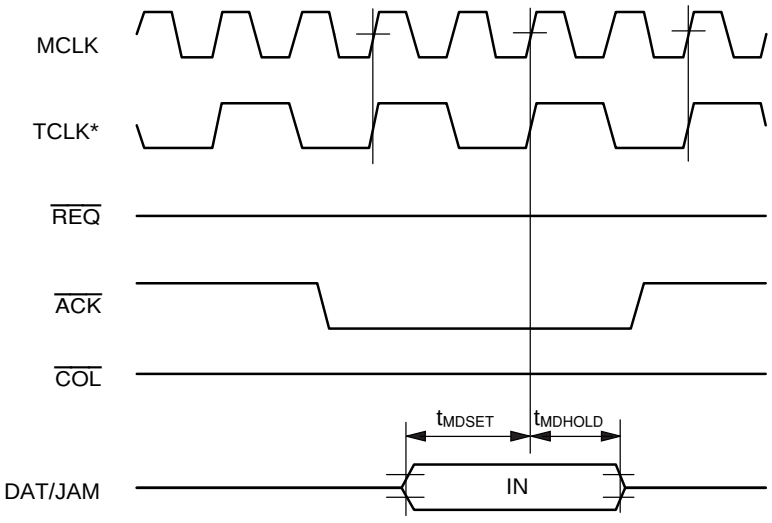
Figure 12. Master Clock (MCLK) Timing



19879B-17

Figure 13. Expansion Bus Asynchronous Clock (ECLK) Timing

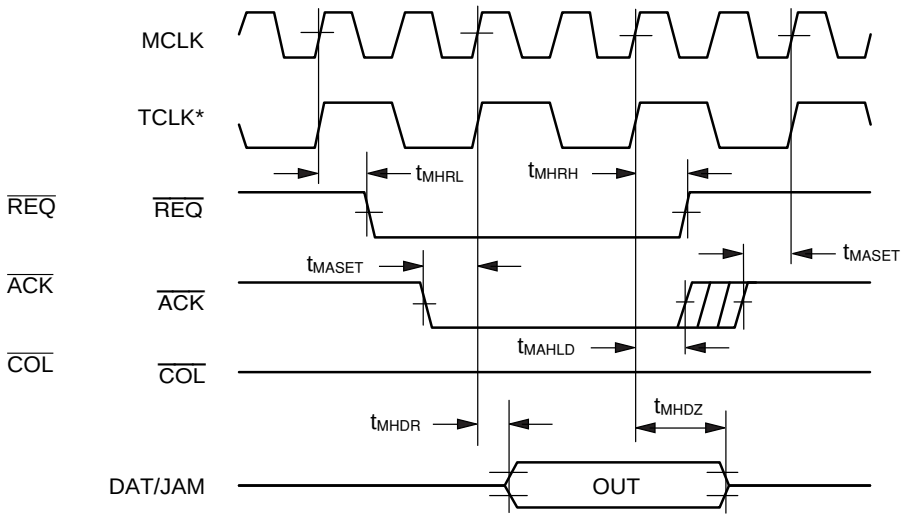
SWITCHING WAVEFORMS



19879B-18

**TCLK illustrates internal IMR2 chip clock phase relationships*

Figure 14. Expansion Bus Input Timing - Synchronous Mode

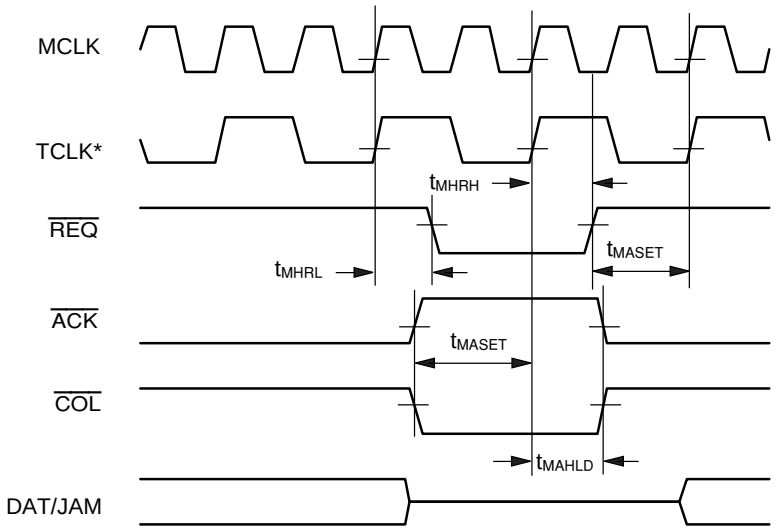


**TCLK illustrates internal IMR2 chip clock phrase relationships*

19879B-19

Figure 15. Expansion Bus Output Timing - Synchronous Mode

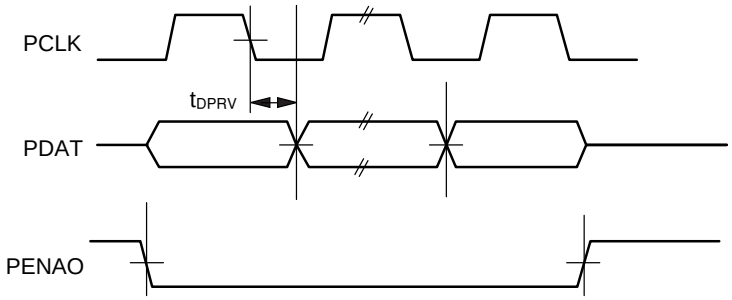
SWITCHING WAVEFORMS



**TCLK illustrates internal IMR2 chip clock phrase relationships*

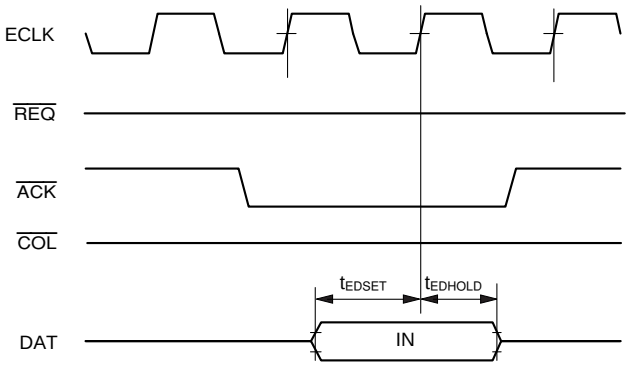
19879B-20

Figure 16. Expansion Port Collision Timing - Synchronous Mode



19879B-21

Figure 17. Packet Report Port Timing



19879B-22

Figure 18. Expansion Port Input Timing - Asynchronous Mode

SWITCHING WAVEFORMS

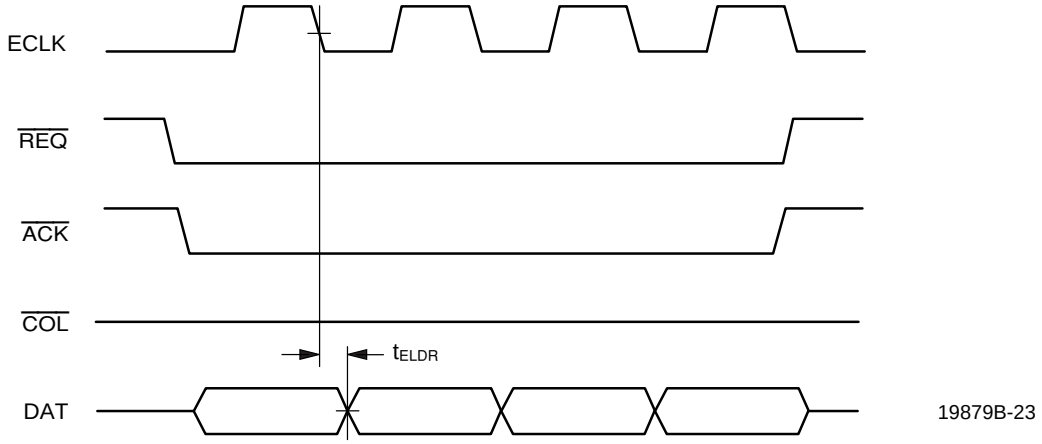


Figure 19. Expansion Port Output Timing - Asynchronous Mode

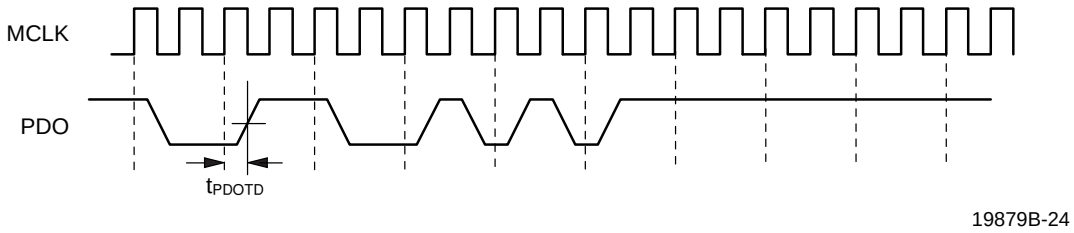


Figure 20. PAUI PDO Transmit

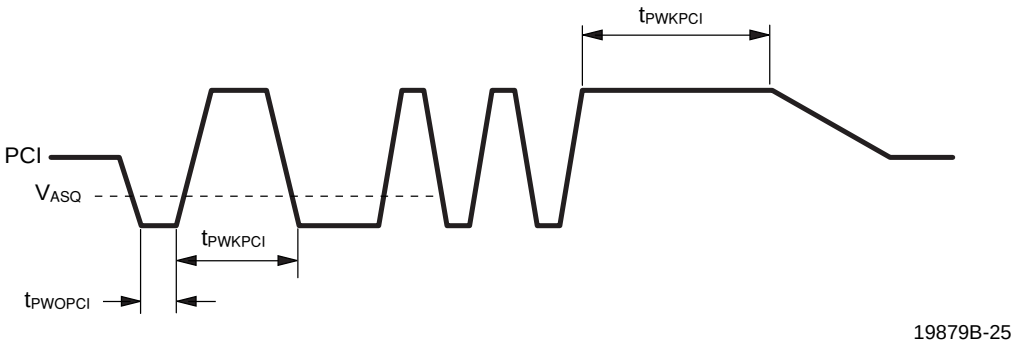


Figure 21. PAUI PCI Receive

SWITCHING WAVEFORMS

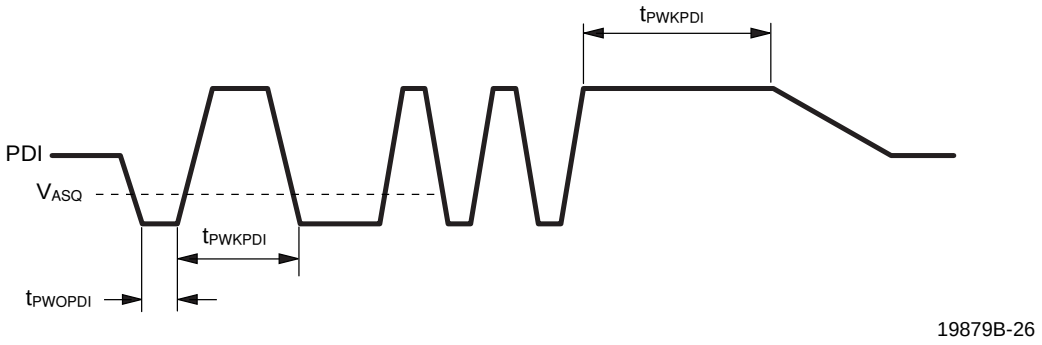


Figure 22. PAUI Receive

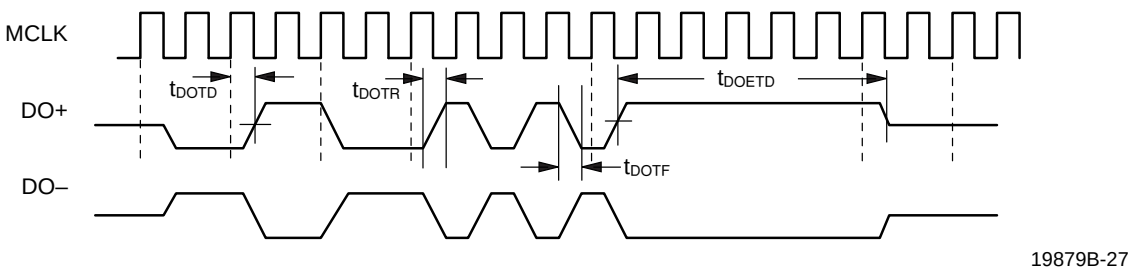


Figure 23. (R)AUI Timing

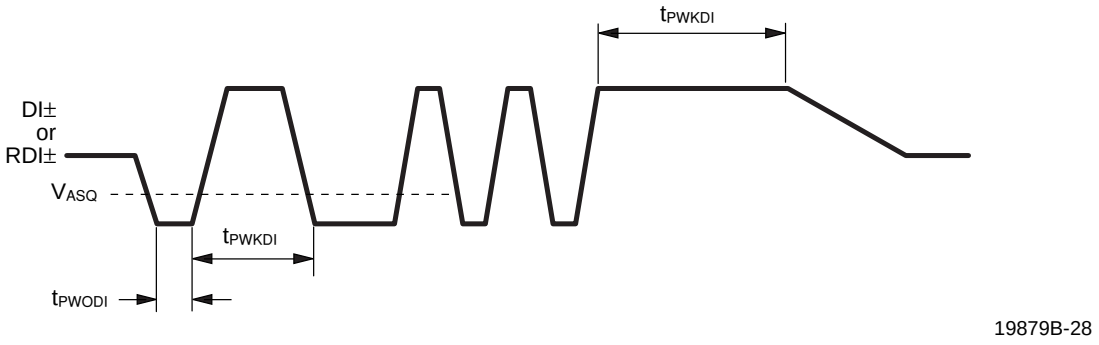


Figure 24. (R)AUI Receive

SWITCHING WAVEFORMS

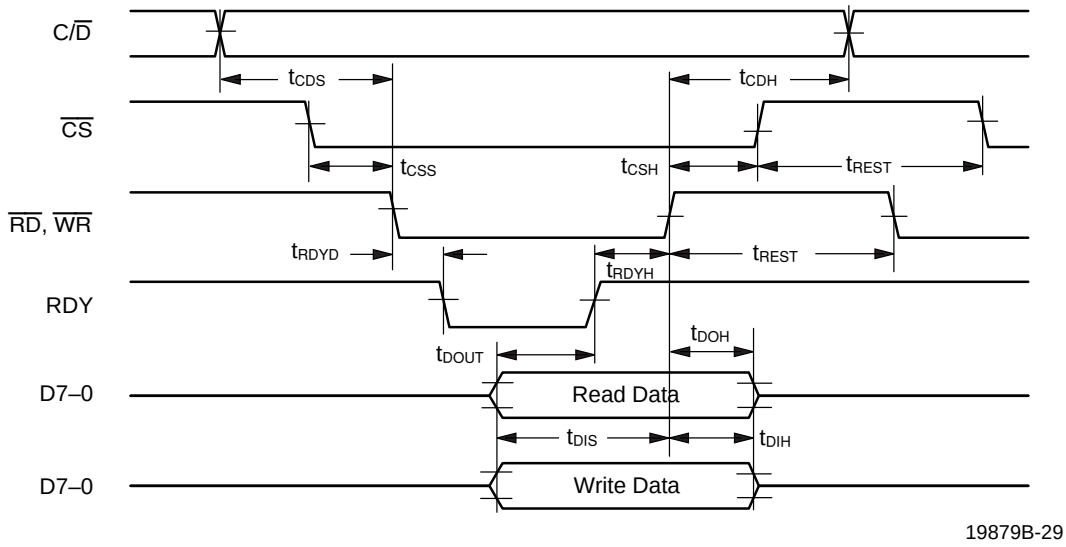
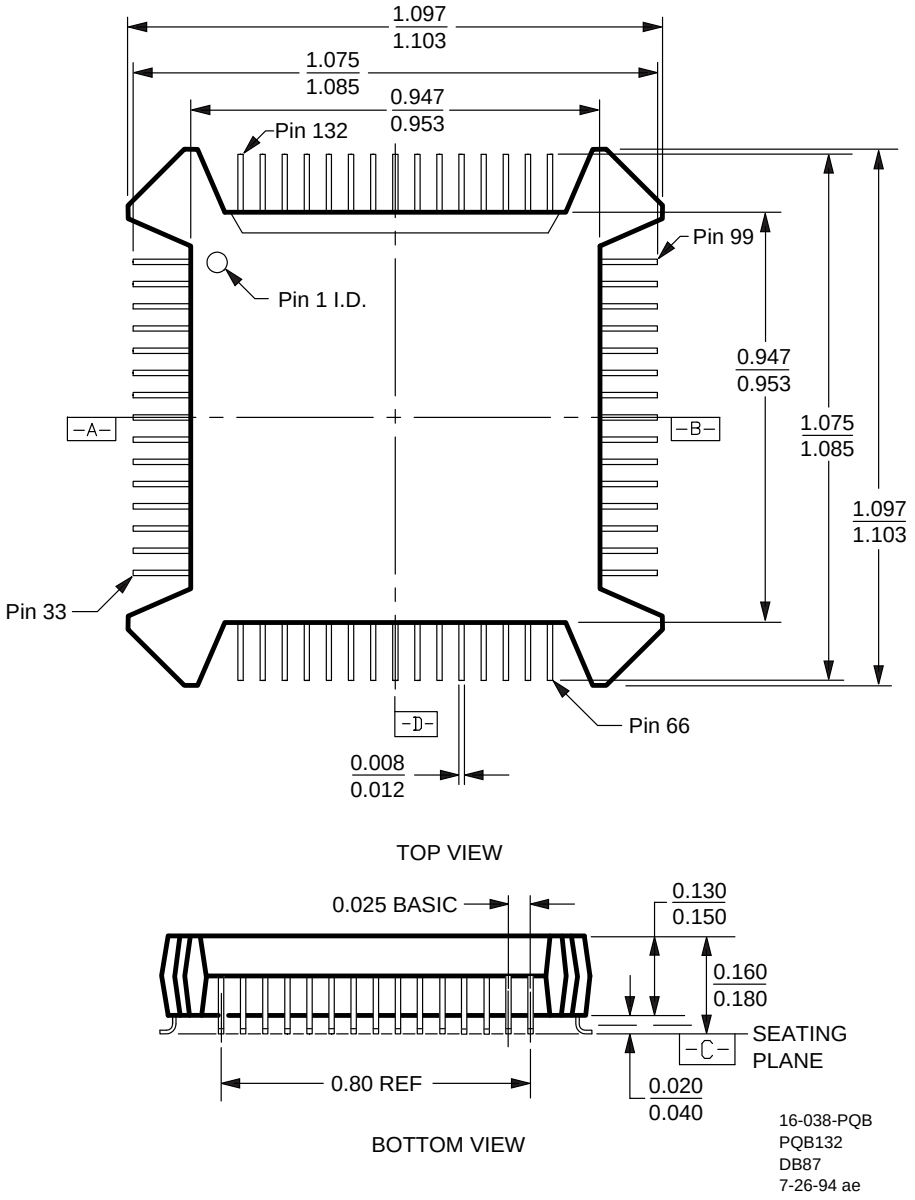


Figure 25. Microprocessor Bus Interface Timing

PHYSICAL DIMENSIONS*

PQB 132
132-Pin Plastic Quad Flat Pack (Measured in inches)



REVISION SUMMARY

This revision (B) reflects changes to Figures 4, 7, and 8. Changes have also been made to the Ordering Information page, DC Characteristics and Switching Characteristics tables. Also, the Table of Contents has been moved to page 7. No other technical changes have been made.

Trademarks