■ OVERVIEW

The SM5813AP/APT is a high-fidelity eight-times oversampling digital filter LSI for digital audio system, using the molibdenum gate C-MOS process developed solely by NPC.
This LSI has a two-channel FIR filter and three types of output modes (16bit/18bit/20bit). Since it has four kinds of system clocks --- 512fs/256fs/384fs/192fs, it can be used for not only CD players but also other audio systems.

■ FEATURES

• FILTER CHARACTERISTICS

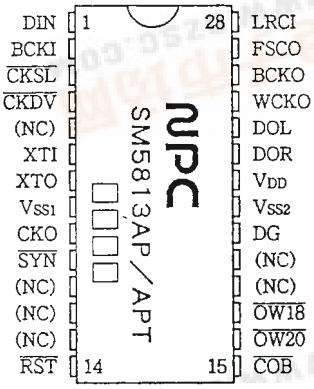
ITEMS	CHARACTERISTICS
Pass band	0 to 0.4535fs
Stop band	0.5465fs to 7.4535fs
Pass band ripple	Within ±0.00005dB
Stop band attenuation	More than 110dB

– Linear phase (There is no group delay distortion.)

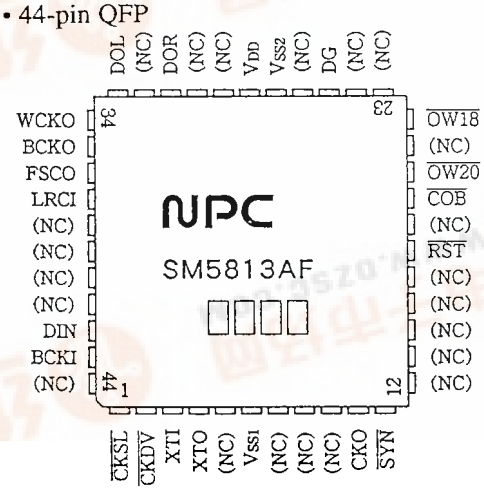
• FILTER STRUCTURE
– Eight-times oversampling
– Two-channel filters
– Cascaded three-stage linear phase FIR filters (153+29+17 order)
– 20 × 22 bit multiplier
– 25bit accumulator
– Overflow limiter
– Crystal oscillation circuit
• Power supply voltage: 5V ±0.5V
• Molybdenam gate C-MOS process
• Free running mode (Jitter-free)
• INPUT/OUTPUT
–16 bit serial data input
(2's complement code, MSB first)
– 16/18/20bit serial data output
(2's complement/Complemented offset binary, MSB first)
• SYSTEM CLOCK
(512fs/256fs/384fs/192fs)
• PACKAGE
28-pin DIP, 44-pin QFP

■ PIN OUT (TOP VIEW)

• 28-pin DIP

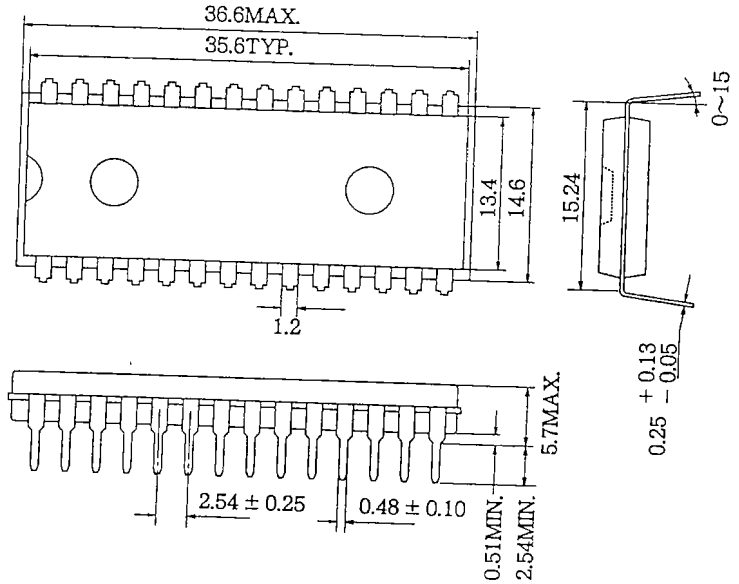


• 44-pin QFP

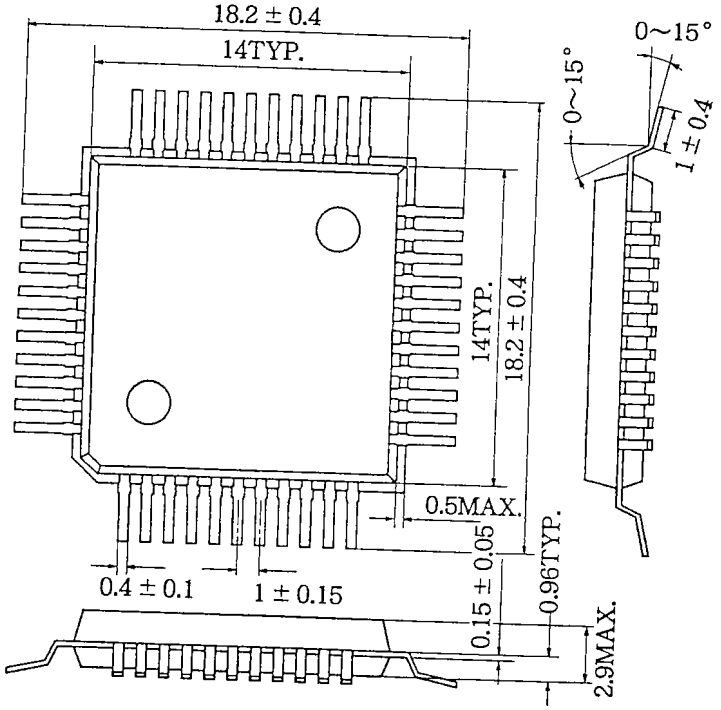


■ PACKAGE DIMENSION (UNIT: mm)

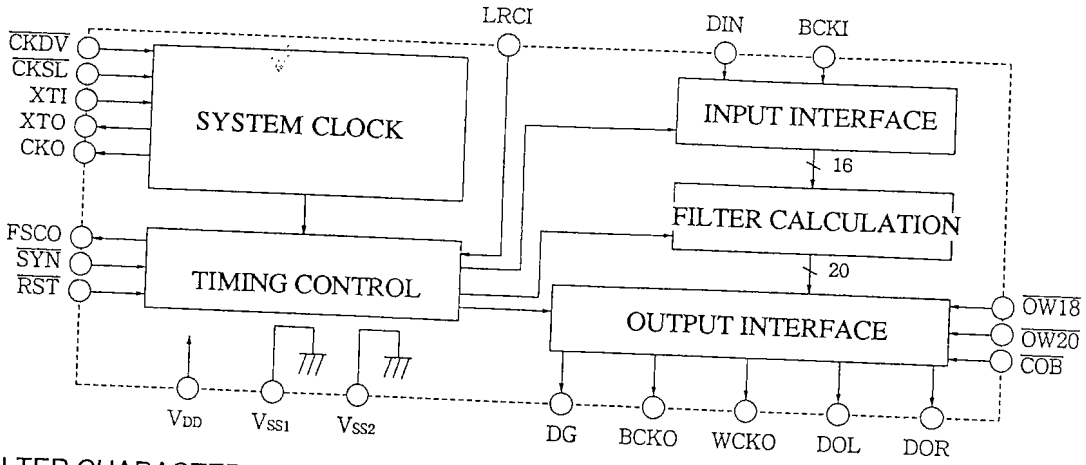
• 28-pin DIP



• 44-pin QFP



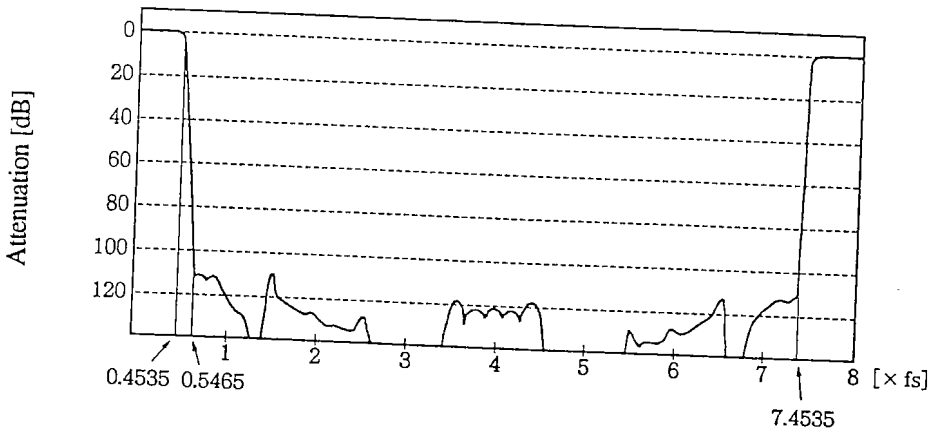
■ BLOCK DIAGRAM



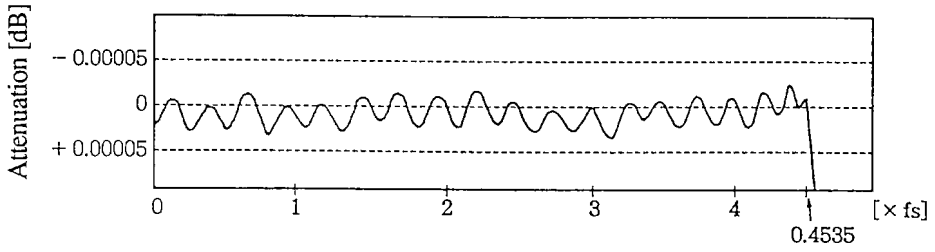
■ FILTER CHARACTERISTICS (THEORITICAL VALUE)

ITEMS	CHARACTERISTICS
Pass band	0 ~ 0.4535fs
Stop band	0.5465fs ~ 7.4535fs
Pass band ripple	Within ±0.00005B
Stop band attenuation	More than 110dB
Group delay time	Constant

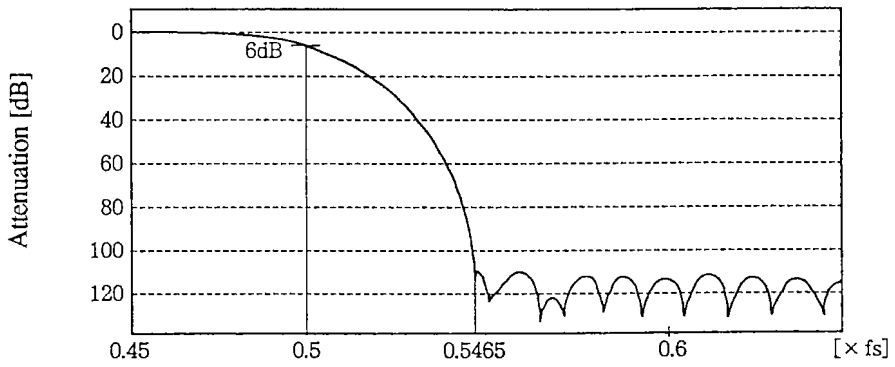
STOP BAND ATTENUATION



PASS BAND RIPPLE



THE DOMAIN BETWEEN PASS BAND AND STOP BAND



■ PIN DESCRIPTION

NO. DIP	NO. QFP	NAME	I/O*	DESCRIPTION
1	42	DIN	I	Serial data input
2	43	BCKI	I	Timing clock for serial input data
3	1	$\overline{\text{CKSL}}$	I	Selecting system clock *2
4	2	$\overline{\text{CKDV}}$	I	
6	3	XTI	I	Input for oscillator or external clock input (System clock)
7	4	XTO	0	Output for oscillator, No connect when using external clock
8	6	V_{SS1}	-	Ground 1
9	10	CKO	0	Clock output (Same frequency as XTI input clock)
10	11	$\overline{\text{SYN}}$	I	H: Free running mode L: Forced synchronizing mode
14	17	$\overline{\text{RST}}$	I	H: Normal operation L: System reset
15	19	$\overline{\text{COB}}$	I	Selecting output data format H: 2's complement L: Complemented offset binary (COB)
16	20	$\overline{\text{OW20}}$	I	Selecting number of output data bits *3
17	22	$\overline{\text{OW18}}$	I	
20	25	DG	0	Deglitch control clock
21	27	V_{SS2}	-	Ground 2
22	28	VDD	-	Supply voltage (+5V)
23	31	DOR	0	Rch serial data output (8fs rate)
24	33	DOL	0	Lch serial data output (8fs rate)
25	34	WCKO	0	Output timing control (Word clock)
26	35	BCKO	0	Output timing control for serial data (Bit clock)
27	36	FSCO	0	Internal timing clock (fs rate)
28	37	LRCI	I	Multiplex clock for Lch/Rch input data (fs rate): H: Lch L: Rch

*1) I: Input terminal
Ip: Input terminal with pull-up resistance
O: Output terminal

*2)

$\overline{\text{CKSL}}$	$\overline{\text{CKDV}}$	System clock (Input to XTI)
H	H	192fs
H	L	384fs
L	H	256fs
L	L	512fs

*3)

$\overline{\text{OW18}}$	$\overline{\text{OW20}}$	The number of output data bit
H	H	16 bit
L	H	18 bit
H	L	20 bit

■ ABSOLUTE MAXIMUM RATINGS

(Vss=OV)

ITEM	SYMBOL	LIMITS	UNIT
SUPPLY VOLTAGE	V_{DD}	-0.3 to 7.0	V
INPUT VOLTAGE	V_{IN}	-0.3 to V_{DD} + 0.3	V
STORAGE TEMPERATURE	T_{STG}	-40 to 125	°C
POWER DISSIPATION	P_W	250	mW
SOLDERING TEMPERATURE	T_{SLD}	255	°C
SOLDERING TIME	T_{SLD}	10	Sec

■ RECOMMENDATORY OPERATING CONDITIONS

(Vss=OV)

ITEM	SYMBOL	LIMITS	UNIT
SUPPLY VOLTAGE	V_{DD}	4.75 to 5.25	V
OPERATING TEMPERATURE	T_{OPRD}	-20 to 70	°C

■ ELECTRIC CHARACTERISTICS

• DC CHARACTERISTICS (Ta = -20 to 70°C, V_{DD} = 4.75 to 5.25V, V_{SS} = 0V)

ITEM	TER-MINAL	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION	V_{DD}	I_{DD}	V_{DD}=5V,fsys*3			45	mA
INPUT VOLTAGE (1)	XTI	V_{IH1}		0.7V_{DD}			V
		V_{IL1}				0.3V_{DD}	V
INPUT VOLTAGE (2)	(*1)	V_{IH2}		2.4			V
		V_{IL2}				0.5	V
OUTPUT VOLTAGE	(*2)	V_{OH}	I_{OH} =-0.4mA	2.5			V
		V_{OL}	I_{OL} =1.6mA			0.4	V
INPUT LEAK CURRENT (1)	XTI	I_{LH}	V_{IN} =VDD		10	20	µA
		I_{LL}	V_{IN} =0V		10	20	µA
INPUT LEAK CURRENT (2)	(*1)	I_{LH}	V_{IN} =V_{DD}			1.0	µA
INPUT CURRENT	(*2)	I_{TI}	V_{TN} =0V		10	20	µA

< TERMINAL>

*1	LRCI, DIN, BCKI, $\overline{\text{CKSL}}$, $\overline{\text{CKDV}}$, $\overline{\text{SYN}}$, $\overline{\text{RST}}$, $\overline{\text{COB}}$, $\overline{\text{OW20}}$, $\overline{\text{OW18}}$
*2	CKO, DG, DOL, DOR, WCKO, BCKO, FSCO

(*3) fsys; Frequency of internal system clock (AP ... 9.5MHz/APT ...13MHz)
When $\overline{\text{CKDV}}$ = L fXTI/2
When $\overline{\text{CKDV}}$ = H fXTI (fXTI: Frequency of XTI input clock)

■ AC CHARACTERISTICS

SM5813AP

(Ta = -20 to 70°C, V_{DD} = 4.75 to 5.25V, V_{SS} = 0V)

1. XTI TERMINAL

a. In case of crystal oscillation

ITEM	SYM-BOL	MIN	TYP	MAX	UNIT	CONDITION CKSL	CONDITION CKDV	NOTE
Oscillating frequency	f_{MAX}	1.0		9.5	MHz	H	H	192fs
		2.0		19.0		H	L	384fs
		1.0		9.5		L	H	256fs
		2.0		19.0		L	L	512fs

b. In case of terminal clock input

ITEM	SYM-BOL	MIN	TYP	MAX	UNIT	CONDITION CKSL	CONDITION CKDV	NOTE
Width of clock pulse	tcw	38		500	nSec	H	H	192fs
		15		250		H	L	384fs
		38		500		L	H	256fs
		15		250		L	L	512fs
Cycle time of clock pulse	tcy	105		1000	nSec	H	H	192fs
		52		500		H	L	384fs
		105		1000		L	H	256fs
		52		500		L	L	512fs

2. INPUT TIMING

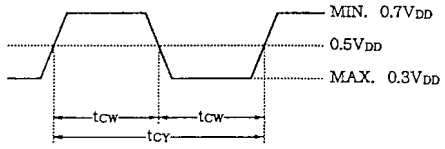
BCKI, DIN, LRCI terminal

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
BCKI, Pulse width	t_{BCW}	100			nSec
BCKI, Cycle time	t_{BCY}	200			nSec
DIN, Set up time	t_{DS}	75			nSec
DIN, Hold time	t_{DH}	75			nSec
Rising edge of last BCKI → Edge of LRCI	t_{BL}	75			nSec
Edge of LRCI → Rising edge of first BCKI	t_{LB}	75			nSec
Falling edge of XTI → Rising edge of LRCI	t_{XL}	20			nSec
Rising edge of LRCI → Falling edge of XTI	t_{LX}	0			nSec

3. OUPUT TIMING

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
BCKO delay time from XTI	txbH	35		120		$\overline{CKDV}$=L
	txbL	35		120	nSec	
	txbH	35		120	nSec	$\overline{CLDV}$=H
	txbL	35		120		
Output delay	tbdL	-10	0	+10	nSec	15pF
	tbdH	-10	0	+10		Load

(1) XTI input clock



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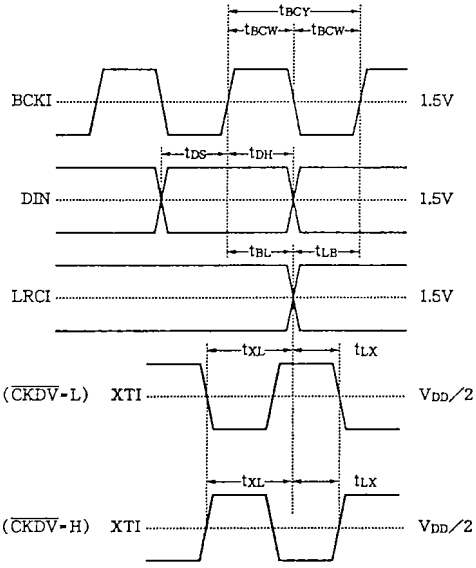
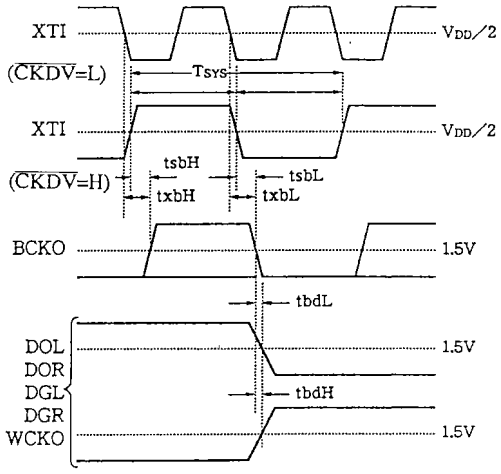


(3) ($\overline{CKDV}$-H) XTI ... $V_{DD}/2$



SM5813APT/AF

(Ta = -20 to 70°C, V_{DD} = 4.75 to 5.25V, V_{SS} = 0V)

1. XTI TERMINAL

a. In case of crystal oscillation

ITEM	SYM-BOL	MIN	TYP	MAX	UNIT	CONDITION CKSL	CONDITION CKDV	NOTE
Oscillating frequency	f_{MAX}	1.0		13.0	MHz	H	H	192fs
		2.0		26.0		H	L	384fs
		1.0		13.0		L	H	256fs
		2.0		26.0		L	L	512fs

b. In case of external clock input

ITEM	SYM-BOL	MIN	TYP	MAX	UNIT	CONDITION CKSL	CONDITION CKDV	NOTE
Width of clock pulse	tcw	35		500	nSec	H	H	192fs
		15		250		H	L	384fs
		35		500		L	H	256fs
		15		250		L	L	512fs
Cycle time of clock pulse	tcy	76		1000	nSec	H	H	192fs
		38		500		H	L	384fs
		76		1000		L	H	256fs
		38		500		L	L	512fs

2. INPUT TIMING

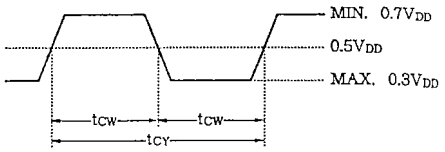
BCKI, DIN, LRCI terminal

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
BCKI, Pulse width	t_{BCW}	100			nSec
BCKI, Cycle time	t_{BCY}	200			nSec
DIN, Set up time	t_{DS}	75			nSec
DIN, Hold time	t_{DH}	75			nSec
Rising edge of last BCKI → Edge of LRCI	t_{BL}	75			nSec
Edge of LRCI → Rising edge of first BCKI	t_{LB}	75			nSec
Falling edge of XTI → Rising edge of LRCI	t_{XL}	20			nSec
Rising edge of LRCI → Falling edge of XTI	t_{LX}	0			nSec

3. OUTPUT TIMING

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
BCKO delay time from XTI	txbH	35		120	nSec	CKDV=L
	txbL	35		120		
	txbH	35		120	nSec	CKDV=H
	txbL	35		120		
Output delay	tbdL	-10		+10	nSec	15pF
	tbdH	-10		+10		Load

(1) XTI input clock



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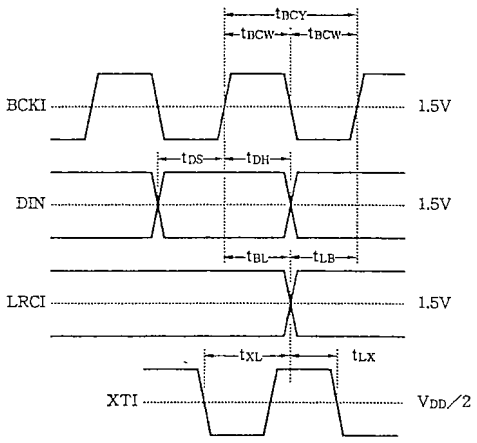

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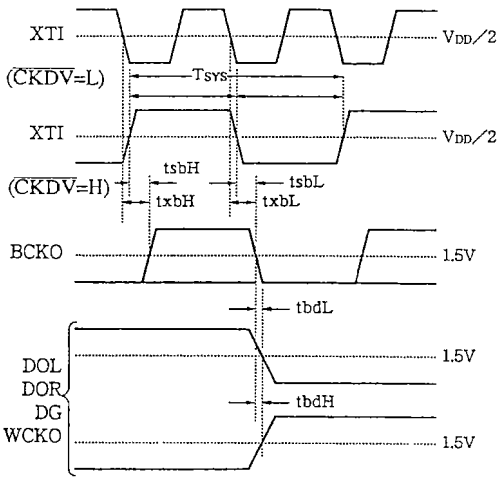


■ FUNCTION

1. EIGHT-TIMES OVERSAMPLING

In put of fs sampling rate to the SM5813 is output with 8fs sampling rate after calculating in the digital filter.

This LSI has cascaded three-stage FIR filter as follows:

2. SYSTEM CLOCK

• SELECTION OF SYSTEM CLOCK

The SM5813AP/APT/AF has an internal clock generator that may be used by connecting a crystal of the appropriate frequency between pins XTI and XTO. Alternatively, an externally generated clock can be input on XTI. The clock frequency Fxi is selected by the CKDV and CKSL inputs from one of the four multiples of the sample frequency shown in the right table, where the clock period txi=1/Fxi. For the 384fs and 512fs clock frequencies, the clock is divided by two for internal use. The system clock signal, of the same frequency as the signal on pin XTI, is available on the CKO output pin.

CONDITION		XTI	Cycle time of internal system clock
$\overline{CKDV}$	$\overline{CKSL}$	clock (F_{xi})	
H	H	192fs	
H	L	256fs	$1/F_{xi}$
L	H	384fs	
L	L	512fs	$2/F_{xi}$

3. AUDIO DATA INPUT

Input data is processed MSB first and 2's complement. Each bit of serial data input on the DIN pin is read into the SIPO register (serial to parallel conversion register) at the rising-edge of BCKI bit clock and converted to parallel data. The SIPO output is transferred to the Lch/Rch input register, respectively, at the rising-edge/ falling-edge of the LRCI clock. (See Figure A and B)

The timing of the operation part and output part are independent from the timing of the input part, so that it is not affected by jitter of the input part.

4. JITTER-FREE MODE AND FORCED SYNCHRONIZATION MODE SELECTION ($\overline{SYN}$, FSCO)

The timing of the internal operation and output (internal timing) are determined by the system clock (the XTI input), which is independent of the input clock timing (BCKI, LRCI).

The internal timing is provided with 2 kinds of "jitter-free mode," and "forced synchronization mode" to cope with jitter on the LRCI clock input. The setting of $\overline{SYN}$ enables selection.

Figure A. Input SIPO

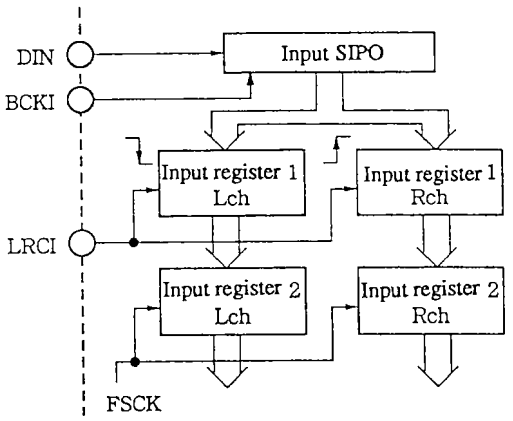
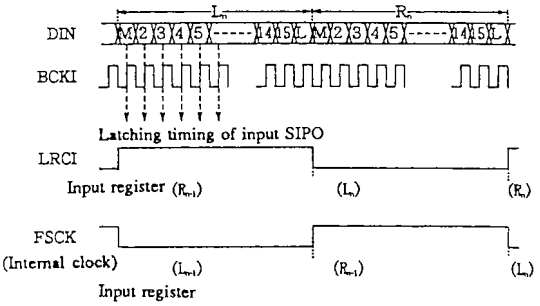


Figure B. Input timing of audio data



● Jitter-free mode ($\overline{SYN}$=H)

When the phase difference between the LRCI clock and the internal timing is within +3/8 to -3/8 of the input sampling frequency (1/fs), the internal timing is not adjusted. Thus jitter on the LRCI clock does not affect the internal timing to prevent malfunctions and jitter transmission.

If the phase difference exceeds the said range, the phase of internal timing is adjusted synchronously with the starting-side edge f the LRCI clock. When a reset is input, the phase is also adjusted.

● Forced synchronization mode ($\overline{SYN}$=L)

In this mode, the internal timing is always reset at the starting-edge of the LRCI input. In this case, malfunction occurs if a cycle which does not statisfy the required system clock cycle due to jitter onthe LRCI input exists. To the contrary, if a cycle which is longer than the specified clock cycle exists, the intervals of the output timing are not the same though operation is performed corrtectly.

● FSCO clock (output)

The fs frequency clock obtained by dividing the XTI clock.

5. DATA AND DAC CONTROL SIGNAL OUTPUT
(DOL, DOR, BCKO, WCKO, DG, $\overline{COB}$, $\overline{OW18}$, $\overline{OW20}$)

● Output data format

(1) MSB first

(2) 2's complement and COB (complemented offset binary) switch COB format ($\overline{COB}$=H)
COB foramt ($\overline{COB}$=L)

● Bit number selection of output data ($\overline{OW18}$, $\overline{OW20}$)

Bit number of output data can be selected from among 16, 18 and 20.

16-bit output ($\overline{OW18}$=H, $\overline{OW20}$=H)
18-bit output ($\overline{OW18}$=L, $\overline{OW20}$=H)
20-bit output ($\overline{OW18}$=H, $\overline{OW20}$=L)

● Output tining

The timing of audio output part is determined corresponding to the system clock frequency of each part. (See Table B, Figure C)

Table B. Output timing

Item	Symbol	$\overline{CKSL}$	
Internal system clock freq.		192fs	256fs
Bit clock cycle	Tb	Tsys	Tsys
Data word length	Tw	24×Tsys	32×Tsys

Tsys is internal system clock cycle.

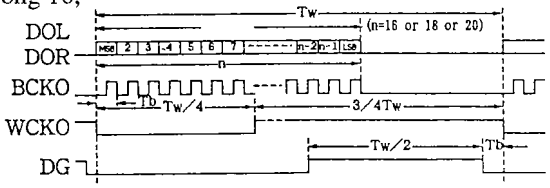


Table C. Output timing

6. SYSTEM RESET ($\overline{RST}$)

When a reset is input in the jitter-free mode, the internal operation timing is reset synchronously with the rising-edge of the following LRCI clock input. Taking advantage of this, the output timing in the jitter-free mode can match to LRCI.

The reset pulse (L level) should be longer than 50ns after power-on. A reset is also unnecessary in the jitter-free mode if the output timing is not required to match with the LRCI input.

In the case of performing the system reset at power-on, connect a 100pF or so capacitor to the RST pin. (See Figure D).

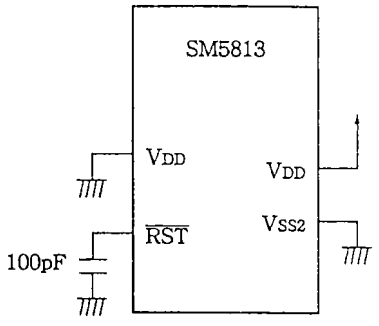
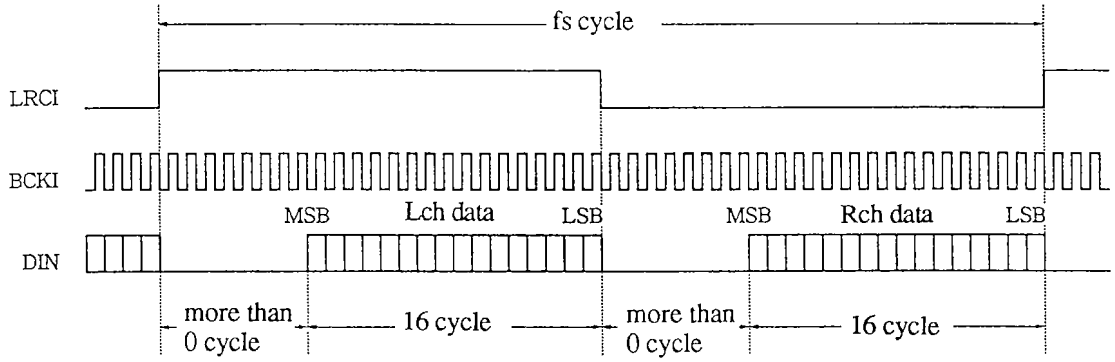


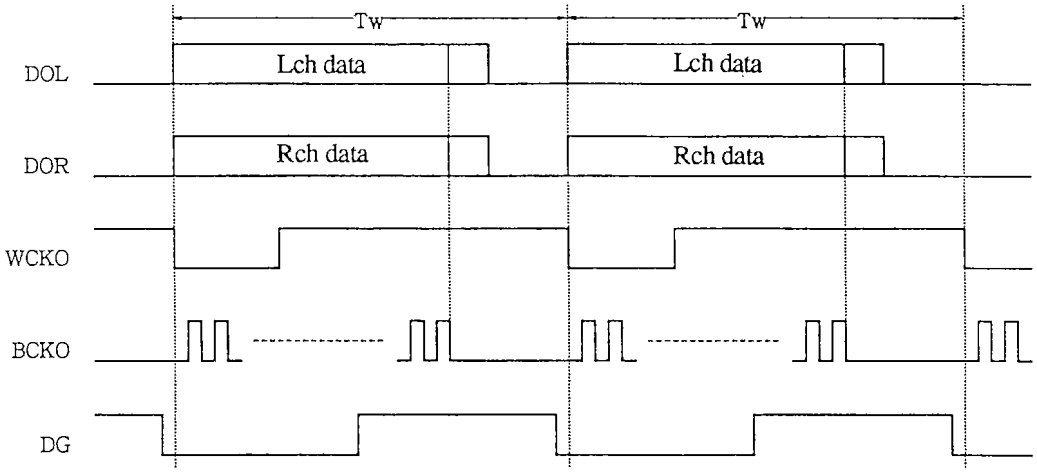
Table D. System reset circuit sample at power-on

■ TIMING CHART

1. SERIAL INPUT TIMING

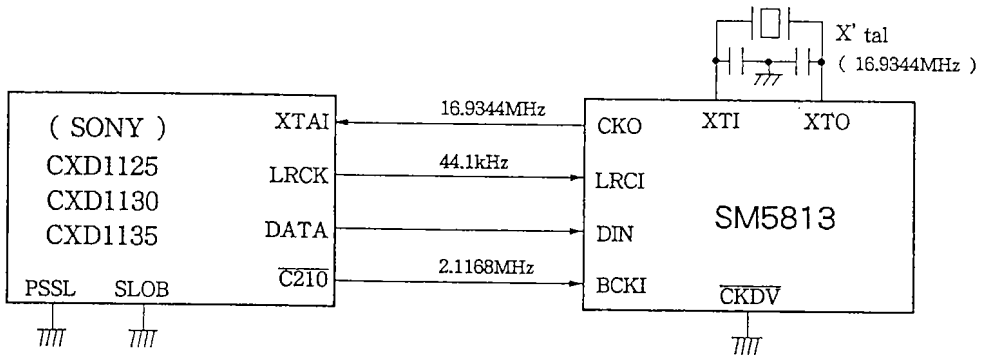


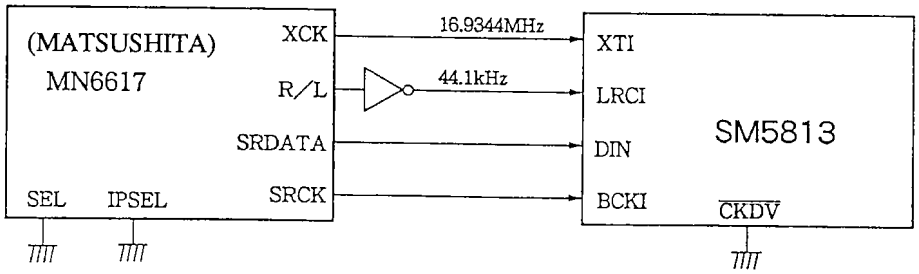
2. SERIAL OUTPUT TIMING

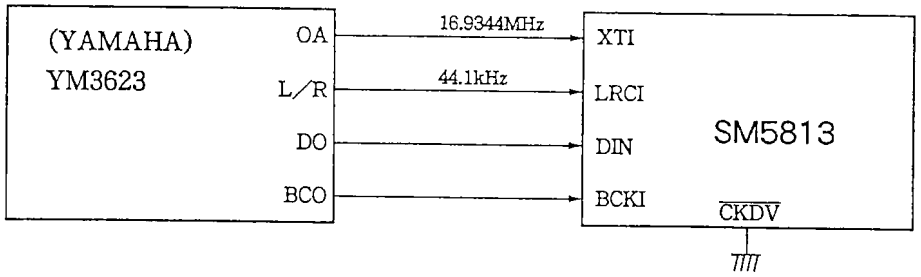


■ TYPICAL APPLICATION

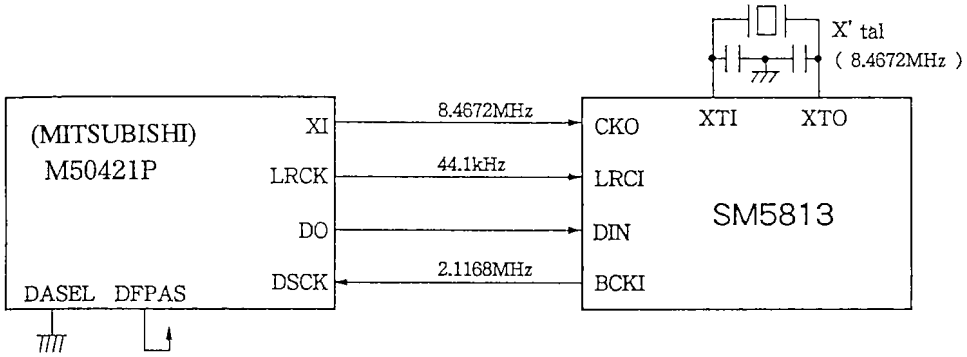
1. INPUT







2. OUTPUT


X' tal
(8.4672MHz)
(MITSUBISHI)
M50421P
XI
LRCK
DO
DSCK
DASEL
DFPAS
8.4672MHz
44.1kHz
2.1168MHz
CKO
LRCI
DIN
BCKI
XTI
XTO
SM5813