NIPPON PRECISION CIRCUITS INC.

SM5843A×1

Audio Multi-function Digital Filter

OVERVIEW

The SM5843A×1 is a multi-function digital filter IC, fabricated using NPC's Molybdenum-gate CMOS process, for digital audio reproduction equipment. It features 8-times oversampling (interpolation), digital deemphasis and soft muting functions. It accepts 16, 18, or 20-bit input data, and outputs data in 18 or 20-bit format. It operates using either a 384fs or 256fs system clock.

FEATURES

- Filter configuration (2-channel processing)
  - 8-times oversampling (interpolation)
    - 3-stage FIR configuration
  - Deemphasis filter
    - IIR filter configuration for correct gain and phase characteristics
    - 2-channel independent ON/OFF control
    - 32/44.1/48 kHz sampling frequency (fs)
  - 21 × 22-bit parallel multiplier/25-bit accumulator for high precision
  - Overflow limiter
- 2 oversampling filter characteristics
  - Sharp roll-off characteristic (response 1)
    - ≤ ±0.00005 dB passband ripple (0 to 0.4535fs)
    - ≥ 110 dB stopband attenuation (0.5465fs to 7.4535fs)
  - Slow roll-off characteristic (response 2)
    - ≤ ±0.00003 dB passband ripple (0 to 0.235fs)
    - ≥ 77 dB stopband attenuation (0.745fs to 7.255fs)
- Soft muting
- Digital attenuator
- Input data format
  - 2s complement, MSB first
    - LR alternating, 16/18/20-bit serial, trailing data
    - LR alternating, 20-bit serial, leading data
    - LR simultaneous, 20-bit serial, leading data
- Output data format
  - 2s complement, MSB first, LR simultaneous
  - 18/20-bit serial
  - BCKO burst (NPC format)
- Dither processing ON/OFF control
- Jitter-free/Sync mode selectable
- 256fs/384fs system clock selectable
  - 21.2/14.2MHz maximum frequency (384fs/256fs)
- 5 V supply
- Crystal oscillator circuit built-in
- TTL-compatible input/outputs
- 28-pin plastic DIP and SOP
- Molybdenum-gate CMOS

APPLICATIONS

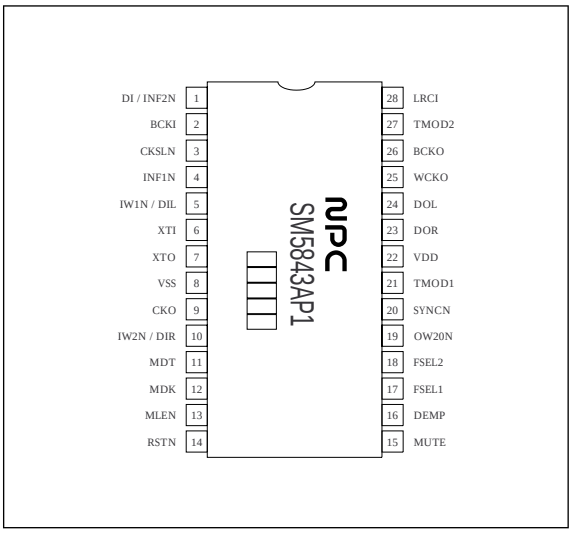
- CD players
- DAT players
- PCM systems

ORDERING INFOMATION

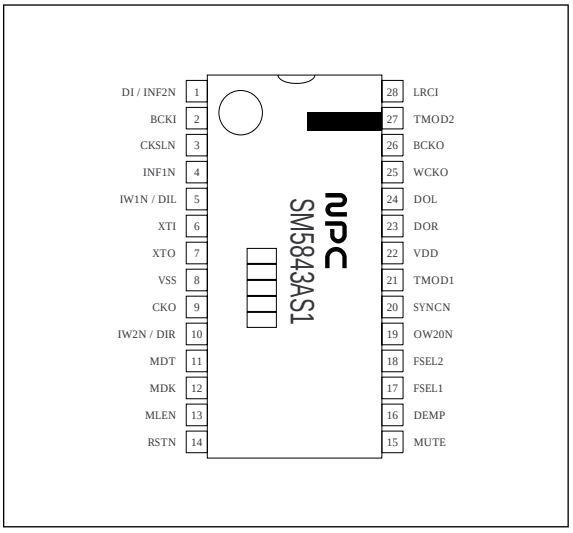
Device	Package
SM5843AP1	28pin DIP
SM5843AS1	28pin SOP

PINOUT(TOP VIEW)

28-pin DIP

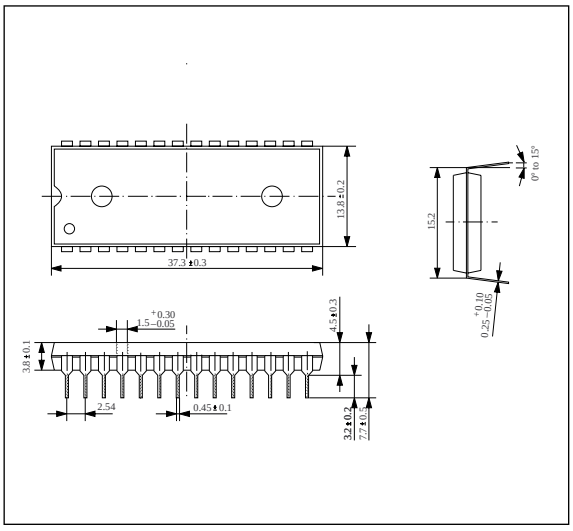


28-pin SOP

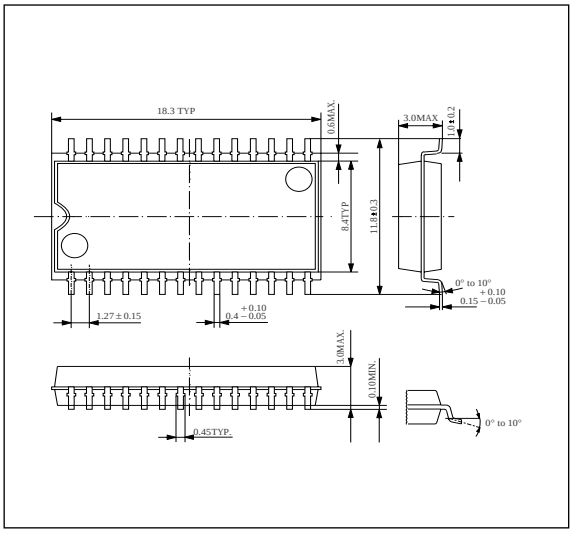


PACKAGE DIMENSIONS(Unit: mm)

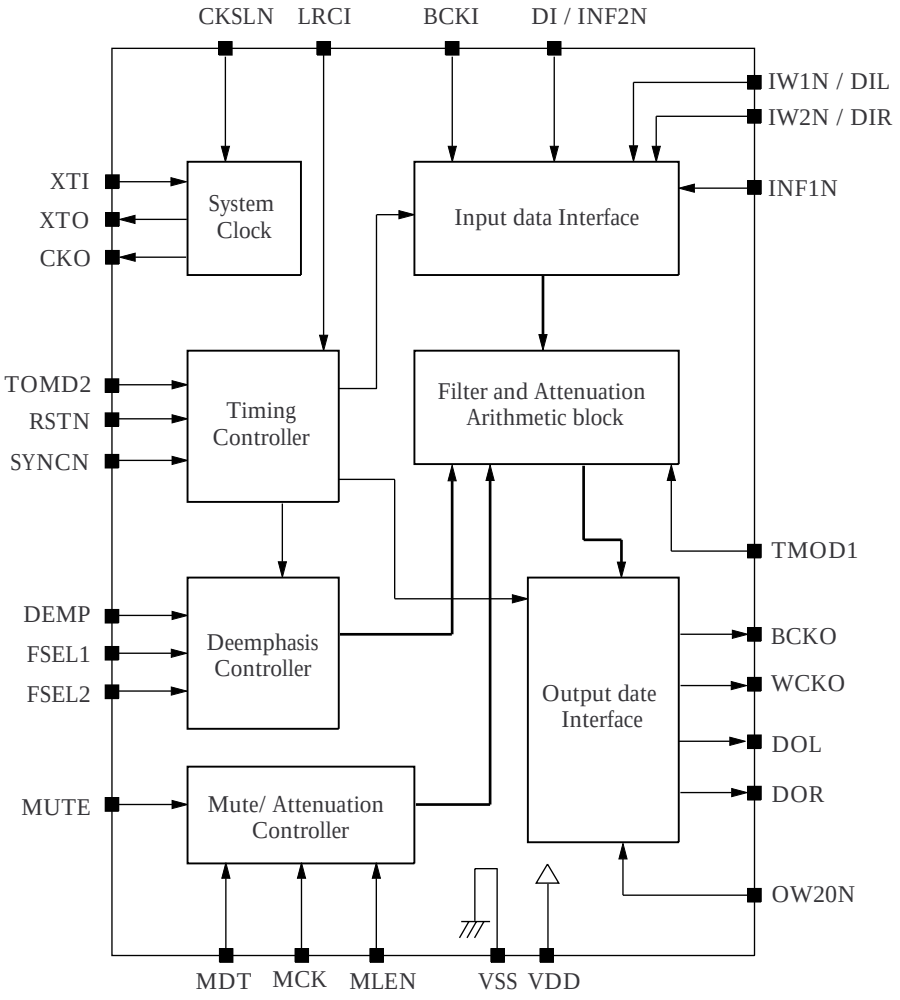
28-pin DIP



28-pin SOP



BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Number</th><th>Name</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>1</td><td>DI/INF2N</td><td>Ip</td><td>Data input when INF1N is LOW, and input format select pin when INF1N is HIGH.</td></tr>
<tr><td>2</td><td>BCKI</td><td>Ip</td><td>Input bit clock</td></tr>
<tr><td>3</td><td>CKSLN</td><td>Ip</td><td>Oscillator and system clock select input. 384fs when HIGH, and 256fs when LOW.</td></tr>
<tr><td>4</td><td>INF1N</td><td>Ip</td><td>Input format select pin. INF1N and INF2N select the pin functions below.
<table>
<tr><th rowspan="2">INF1N</th><th rowspan="2">DI/INF2N</th><th rowspan="2">Input format</th><th colspan="3">Pin function selection</th></tr>
<tr><th>DI/INF2N</th><th>IW1N/DIL</th><th>IW2N/DIR</th></tr>
<tr><td>LOW</td><td>LOW</td><td rowspan="2">LR alternating, trailing data</td><td rowspan="2">DI</td><td rowspan="2">IW1N</td><td rowspan="2">IW2N</td></tr>
<tr><td>LOW</td><td>HIGH</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>LR alternating, leading data</td><td rowspan="2">INF2N</td><td rowspan="2">DIL</td><td rowspan="2">DIR</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>LR simultaneous, leading data</td></tr>
</table></td></tr>
<tr><td>5</td><td>IW1N/DIL</td><td>Ip</td><td>Input bit length select pin when INF1N is LOW, and left-channel data input when INF1N is HIGH. IW1N and IW2N select the input data length.
<table>
<tr><th>INF1N</th><th>IW2N/DIL</th><th>IW1N/DIR</th><th>Input bit length</th></tr>
<tr><td rowspan="4">LOW</td><td>LOW</td><td>LOW</td><td>20 bits</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>20 bits</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>18 bits</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>16 bits</td></tr>
<tr><td>HIGH</td><td>×</td><td>×</td><td>20 bits</td></tr>
</table></td></tr>
<tr><td>6</td><td>XTI</td><td>I</td><td>Oscillator input connection</td></tr>
<tr><td>7</td><td>XTO</td><td>O</td><td>Oscillator output connection</td></tr>
<tr><td>8</td><td>VSS</td><td>–</td><td>Ground</td></tr>
<tr><td>9</td><td>CKO</td><td>O</td><td>Oscillator output clock. Same frequency as XTI.</td></tr>
<tr><td>10</td><td>IW2N/DIR</td><td>Ip</td><td>Input bit length select pin when INF2N is LOW, and right-channel data input when INF2N is HIGH. IW1N and IW2N select the input data length as shown in the table for pin 5.</td></tr>
<tr><td>11</td><td>MDT</td><td>Ip</td><td>Attenuator serial data input</td></tr>
<tr><td>12</td><td>MCK</td><td>Ip</td><td>Attenuator bit clock input</td></tr>
<tr><td>13</td><td>MLEN</td><td>Ip</td><td>Attenuator latch enable input</td></tr>
<tr><td>14</td><td>RSTN</td><td>Ip</td><td>System reset. Reset operation when LOW, and normal operation when HIGH.</td></tr>
<tr><td>15</td><td>MUTE</td><td>Ip</td><td>Mute control signal. Muting when HIGH, and normal operation when LOW.</td></tr>
<tr><td>16</td><td>DEMP</td><td>Ip</td><td>Deemphasis control signal. OFF when LOW, and ON when HIGH.</td></tr>
<tr><td>17</td><td>FSEL1</td><td>Ip</td><td rowspan="2">Deemphasis filter select inputs
<table>
<tr><th>FSEL1</th><th>FSEL2</th><th>Sampling frequency (fs)</th></tr>
<tr><td>LOW</td><td>LOW</td><td>44.1 kHz</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>48 kHz</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>Test mode</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>32 kHz</td></tr>
</table></td></tr>
<tr><td>18</td><td>FSEL2</td><td>Ip</td></tr>
<tr><td>19</td><td>OW20N</td><td>Ip</td><td>Output bit length select pin. 20-bit output when LOW, and 18-bit output when HIGH.</td></tr>
<tr><td>20</td><td>SYNCN</td><td>Ip</td><td>Sync mode select pin. Normal sync mode when LOW, and jitter-free mode when HIGH.</td></tr>
<tr><td>21</td><td>TMOD1</td><td>Ip</td><td>Dither processing control. ON when LOW, and OFF when HIGH.</td></tr>
<tr><td>22</td><td>VDD</td><td>–</td><td>5 V supply</td></tr>
</table>

Number	Name	I/O[1]	Description
23	DOR	O	Right-channel data output
24	DOL	O	Left-channel data output
25	WCKO	O	Output word clock
26	BCKO	O	Output bit clock
27	TMOD2	Ip	Filter characteristic select pin. Sharp roll-off (response 1) when HIGH, and slow roll-off (response 2) when LOW.
28	LRCI	Ip	Input data sample rate (fs) clock

1. I = input, Ip = Input with pull-up resistor, O = output

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	550 (DIP)	mW
		390 (SOP)	
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

fs = 384fs (CKSLN = HIGH): V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.5 to 5.5	V
Operating temperature range	T_{opr}	–20 to 80	°C

fs = 256fs (CKSLN = LOW): V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.75 to 5.25	V
Operating temperature range	T_{opr}	–20 to 70	°C

DC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 5.0 V[1]	–	50	65	mA
XTI HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
XTI AC-coupled input voltage	V_{INAC}		0.3V_{DD}	–	–	V_{p-p}
HIGH-level input voltage[2]	V_{IH2}		2.4	–	–	V
LOW-level input voltage[2]	V_{IL2}		–	–	0.5	V
HIGH-level output voltage[3]	V_{OH}	I_{OH} = –0.4 mA	2.5	–	–	V
LOW-level output voltage[3]	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH}	V_{IN} = V_{DD}	–	10	20	µA
XTI LOW-level input current	I_{IL1}	V_{IN} = 0 V	–	10	20	µA
LOW-level input current[2]	I_{IL2}	V_{IN} = 0 V	–	10	20	µA
Input leakage current[2]	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA

1. f_{SYS} = 256fs = 14.2 MHz (CKSLN = LOW), no output load
2. Pins DI/INF2N, BCKI, CKSLN, INF1N, IW1N/DIL, IW2N/DIR, MDT, MCK, MLEN, RSTN, MUTE, DEMP, FSEL1, FSEL2, OW20N, SYNCN, LRCI, TMOD1, TMOD2
3. Pins CKO, DOL, DOR, BCKO, WCKO

AC Electrical Characteristics

Input Clock (XTI)

Crystal oscillator

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	2.0	–	21.2	MHz

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	1.0	–	14.2	MHz

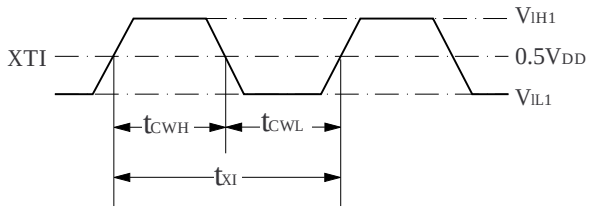
External clock input

fs = 384fs (CKSLN = HIGH): V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	20	–	250	ns
Clock LOW-level pulsewidth	t_{CWL}	20	–	250	ns
Clock pulse cycle time	t_{XI}	47	–	500	ns

fs = 256fs (CKSLN = LOW): V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 70 °C

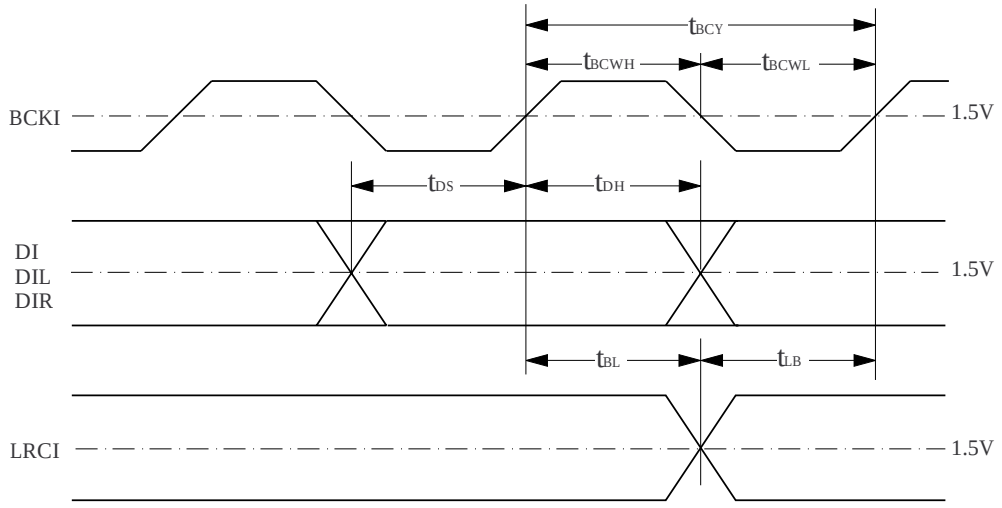
Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock HIGH-level pulsewidth	t_{CWH}	30	–	500	ns
Clock LOW-level pulsewidth	t_{CWL}	30	–	500	ns
Clock pulse cycle time	t_{XI}	70	–	1000	ns



Serial input timing (BCKI, DI, DIL, DIR, LRCI)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI pulse cycle	t_{BCY}	100	–	–	ns
DIN setup time	t_{DS}	50	–	–	ns
DIN hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns



Reset timing (RSTN)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

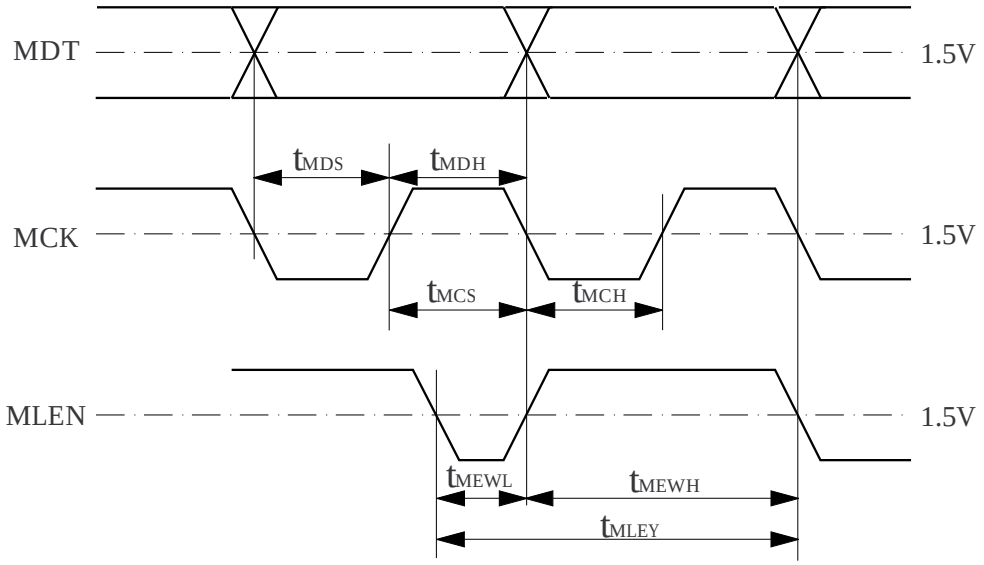
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
$\overline{RST}$ LOW-level reset pulsewidth	t_{RST}	At power-ON	1	–	–	µs
		At all other times	50	–	–	ns

Attenuator timing (MDT, MCK, MLEN)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
MDT setup time	t_{MDS}	20	–	–	ns
MDT hold time	t_{MDH}	20	–	–	ns
MLEN setup time	t_{MCS}	40	–	–	ns
MLEN hold time	t_{MCH}	20	–	–	ns
MLEN LOW-level pulsewidth	t_{MEWL}	20	–	–	ns
MLEN HIGH-level pulsewidth	t_{MEWH}	20	–	–	ns
MLEN pulse cycle time	t_{MLEY}	6	–	–	t_{SYS}[1]

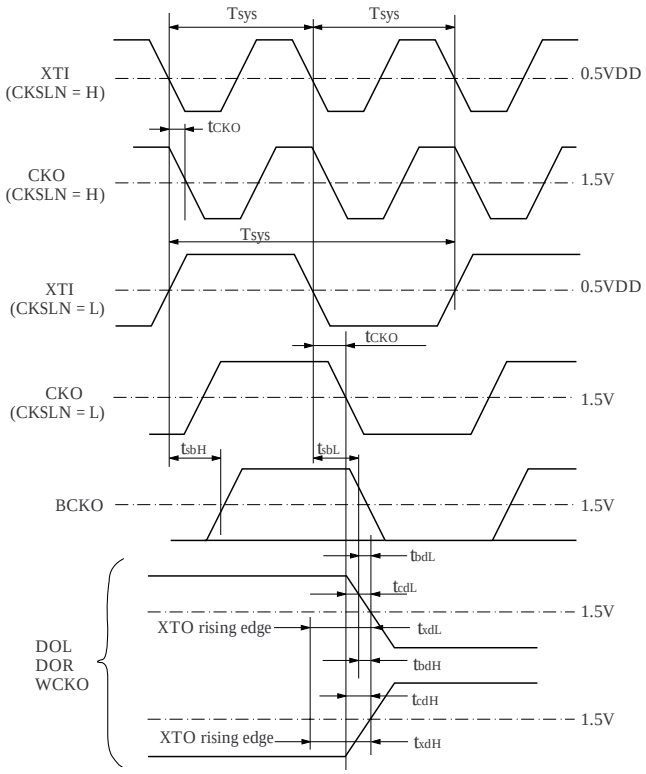
1. t_{SYS} = 1/384fs when CKSLN is HIGH, and 1/256fs when CKSLN is LOW.



Output timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 °C, C_L = 15 pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI to XTO delay	t_{XTO}	XTI fall to XTO rise	3	–	15	ns
XTI to CKO delay	t_{CKO}	XTI fall to CKO fall	10	–	35	ns
XTI to BCKO delay (CKSLN = HIGH)	t_{sbH}	XTI fall to BCKO rise	20	–	60	ns
	t_{sbL}	XTI fall to BCKO fall	20	–	60	
XTI to BCKO delay (CKSLN = LOW)	t_{sbH}	XTI fall to BCKO rise	20	–	60	ns
	t_{sbL}	XTI fall to BCKO fall	20	–	60	
BCKO to DOL, DOR, WCKO delay	t_{bdH}	BCKO fall to output rise	–5	–	10	ns
	t_{bdL}	BCKO fall to output fall	–5	–	10	
CKO TODOL, DOR, WCKO delay	t_{cdH}	CKO fall to output rise	5	–	25	ns
	t_{cdL}	CKO fall to output fall	5	–	25	
XTO TODOL, DOR, WCKO delay	t_{xdH}	XTO rise to output rise	15	–	50	ns
	t_{xdL}	XTO rise to output fall	15	–	50	



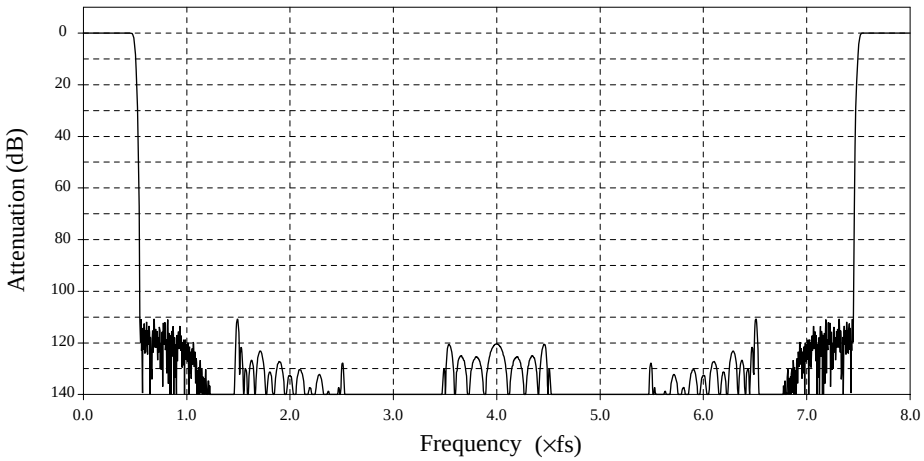
Filter Characteristics

8-times interpolation filter (sharp roll-off: response 1)

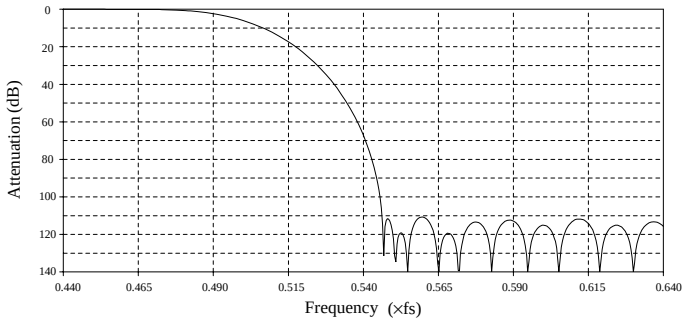
Parameter	Condition	Rating @ 256fs
Passband		0 to 0.4535fs
Stopband		0.5465fs to 7.4535fs
Passband ripple		≤ ±0.00005 dB
Stopband attenuation		≥ 110 dB
Group delay[1]	SYNCN = LOW	44.625/fs
	SYNCN = HIGH	44.25/fs to 45.0/fs

1. The digital filter arithmetic computation time from when the completion of data input at rate fs to the start of data output at rate 8fs.

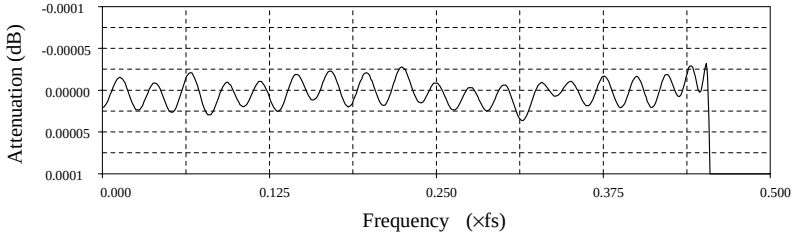
8fs filter response with deemphasis OFF



8fs filter band transition response with deemphasis OFF



8fs filter passband response with deemphasis OFF

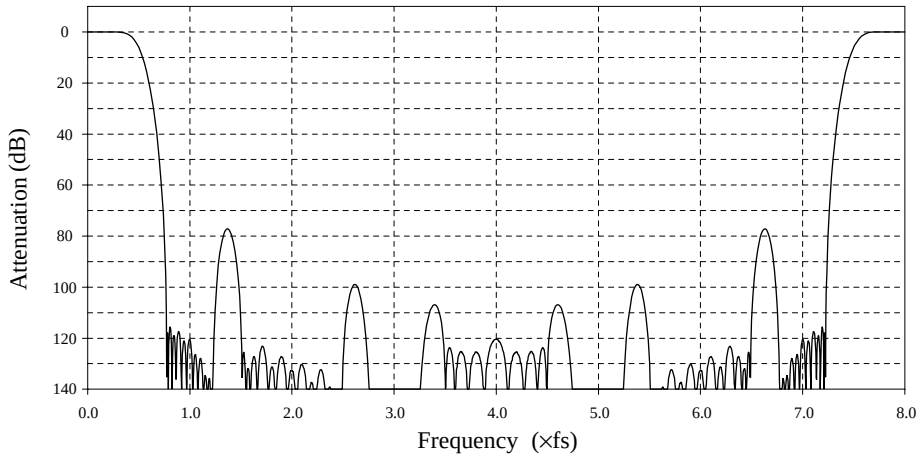


8-times interpolation filter (slow roll-off: response 2)

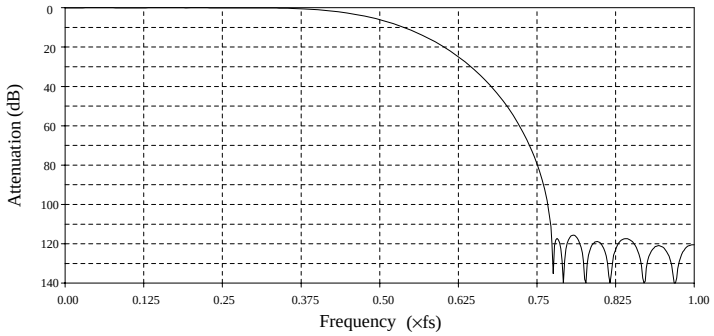
Parameter	Condition	Rating @ 256fs
Passband	< 3 dB attenuation	0 to 0.455fs
Stopband	> 77 dB attenuation	0.745fs to 7.255fs
Passband ripple	0 to 0.235fs	≤ ±0.00003 dB
Stopband attenuation		≥ 77 dB
Group delay[1]	SYNCN = LOW	25.625/fs
	SYNCN = HIGH	25.25/fs to 26.0/fs

1. The digital filter arithmetic computation time from when the completion of data input at rate fs to the start of data output at rate 8fs.

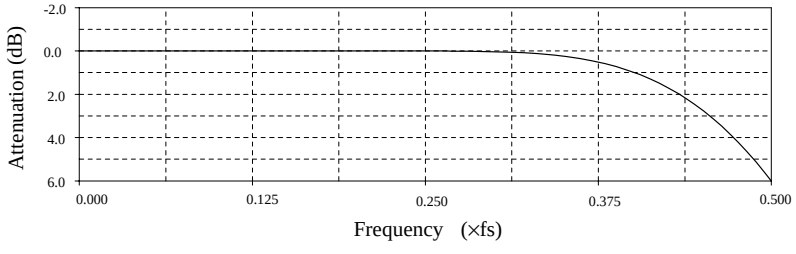
8fs filter response with deemphasis OFF



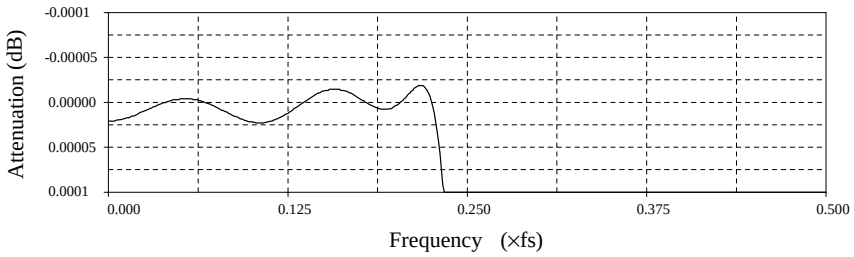
8fs filter band transition response with deemphasis OFF



8fs filter passband response with deemphasis OFF



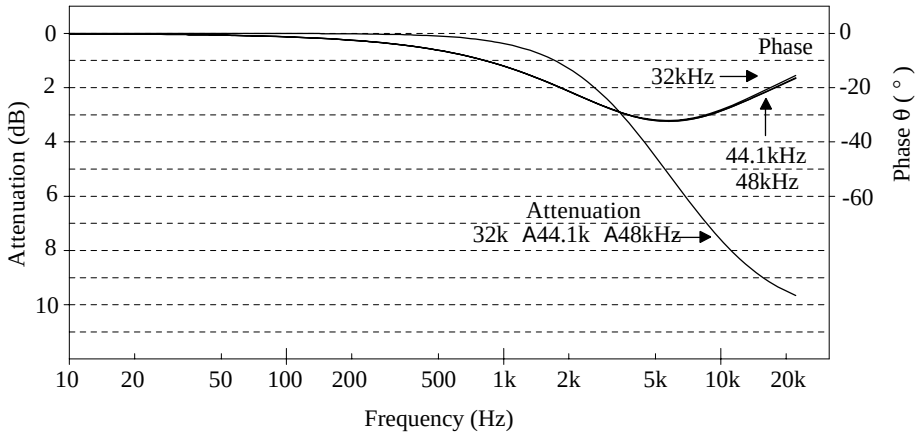
8fs filter passband response [amplitude gain enlarged]



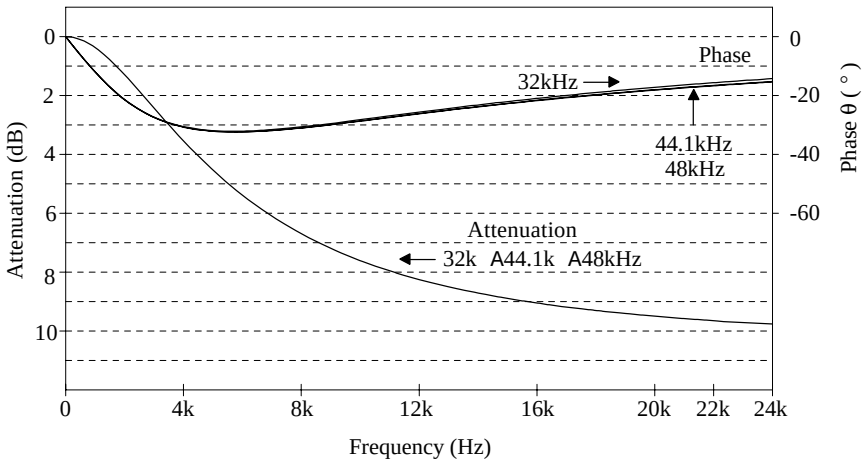
Deemphasis filter

Parameter		Sampling frequency (fs)		
		32 kHz	44.1 kHz	48 kHz
Passband bandwidth (kHz)		0 to 14.5	0 to 20.0	0 to 21.7
Deviation from ideal characteristic	Attenuation	≤ ±0.001 dB		
	Phase, θ	0 to 1.5°		

Passband response with deemphasis ON (logarithmic frequency axis)



Passband response with deemphasis ON (linear frequency axis)



FUNCTIONAL DESCRIPTION

The basic arithmetic block is shown in figure 1, and the function of each block is described in the following sections.

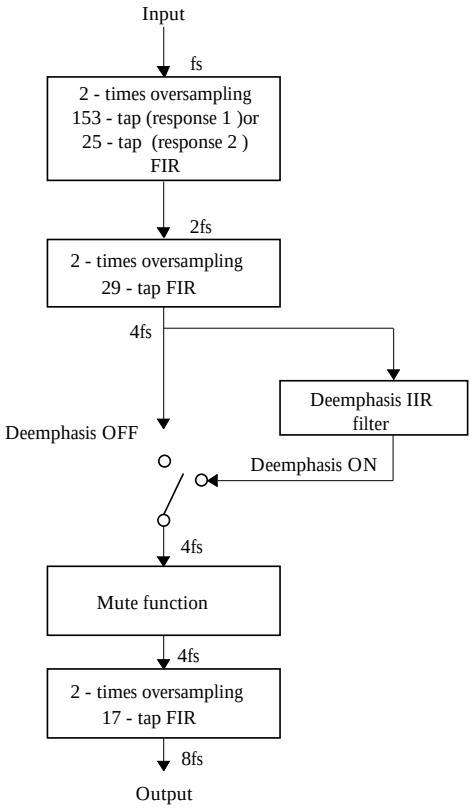


Figure 1. Arithmetic block diagram

8-times Oversampling (Interpolation)

The interpolation arithmetic block is comprised of 3 cascaded, 2-times FIR interpolation filters, as shown in figure 1.

The input signal is sampled at rate fs, and then 8-times oversampling data is output. Sampling noise in the 0.5465fs to 7.4535fs stopband for the sharp roll-off (response 1) characteristic, 0.745fs to 7.255fs for the slow roll-off (response 2) characteristic, is removed by the interpolation filter.

Digital Deemphasis

The digital deemphasis filter has the same construction as analog filters. It is implemented as an IIR filter to faithfully reproduce the gain and phase characteristics of standard analog deemphasis filters. The three sets of filter coefficients for the three fs = 32.0/44.1/48.0 kHz sampling frequencies are selected by FSEL1 and FSEL2 when the sampling frequency is specified, as shown in the following table. Deemphasis is ON when DEMP is HIGH, and OFF when DEMP is LOW.

FSEL1	FSEL2	Sampling frequency (fs)
LOW	LOW	44.1 kHz
LOW	HIGH	48 kHz
HIGH	LOW	Test mode
HIGH	HIGH	32 kHz

Note that test mode is not available for operation.

Soft Muting

The muting function controls the muting of both left and right channels simultaneously. Muting is ON when MUTE is HIGH, muting is OFF when MUTE is LOW.

When MUTE goes HIGH, the attenuation changes smoothly from 0 to –∞ dB in 512/fs, or approximately 11.6 ms when fs = 44.1 kHz. When MUTE goes LOW, muting is released and the attenuation changes smoothly from –∞ to 0 dB, again taking approximately 11.6 ms.

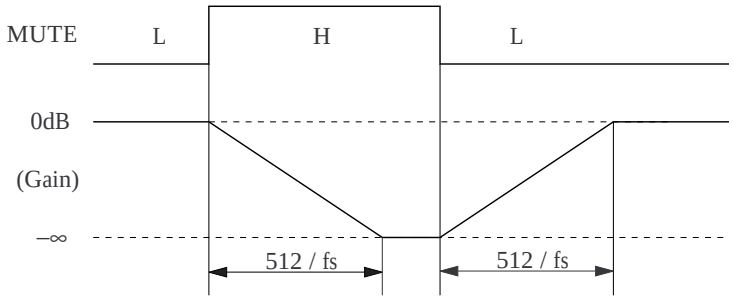


Figure 2. Mute timing

When RSTN goes LOW, the DOL and DOR outputs go LOW, immediately muting the output signal. Muting is released and timing is synchronized immediately after RSTN goes HIGH.

Digital Attenuator (MDT, MCK, MLEN)

The attenuation function is controlled by MDT, MCK and MLEN. MDT data, in 11-bit serial MSB first format, is shifted into an internal shift register on the rising edge of the serial data clock MCK. The contents of the shift register are transferred to the internal processing circuits on the rising edge of the MLEN gate pulse. The attenuation data format is shown in figure 3.

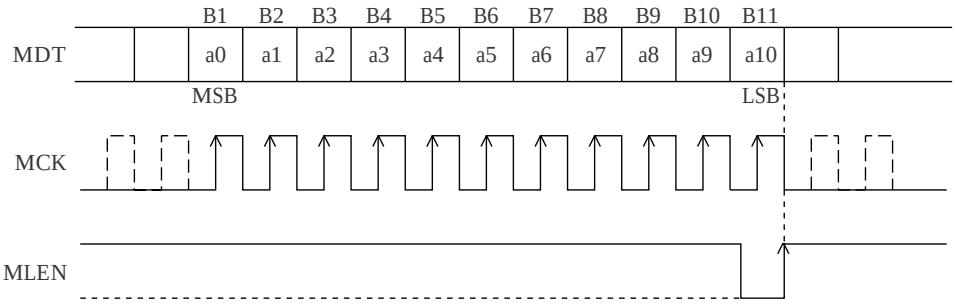


Figure 3. Attenuation data format

The attenuation register data DATT can take on any value between 0 and 1024 (400_H). The attenuation is given by the following equation for both left and right channels simultaneously.

Attenuation = $20 \times \log_{10}(DATT/1024)$ [dB]

Thus, the attenuation level is –∞ when DATT is 0, and attenuation is 0 dB when DATT is 1024. DATT is set to 1024 (400_H) after system reset initialization. The attenuation data and attenuation level for sample DATT values are shown in the following table.

Attenuation data DATT	Attenuation level (dB)
000_H	–∞
001_H to $3FF_H$	–60.206 to –0.0085
400_H	0

Attenuation operation

When an attenuation value DATT is set, the attenuation changes smoothly from the current attenuation level to the new level. The new attenuation data is stored in the attenuation register while the current attenuation data is stored in a temporary register. The attenuation then changes smoothly by ramping between the two register values, updating the temporary register with each step. If a new attenuation value for DATT is set before the previous target attenuation level is reached, the attenuation then ramps toward the new attenuation level.

When MUTE is HIGH, the attenuation level is −∞. When MUTE goes LOW (muting OFF), the attenuation level returns to that of the original value of DATT.

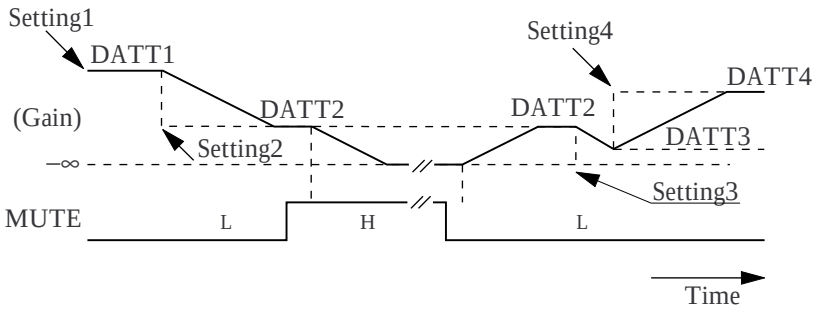


Figure 4. Attenuation and mute timing

System Clock (XTI, XTO, CKO, CKSLN)

Two system clock frequencies, 384fs and 256fs, can be used. An external clock source can be input on XTI, or a crystal oscillator can be constructed by connecting a crystal between XTI and XTO. The system clock is also buffered and then output on CKO. The system clock frequency selection and the internal clock frequency are shown in the following table.

Parameter	CKSL	
	HIGH	LOW
XTI input clock frequency ($f_{XI} = 1/t_{XI}$)	384fs	256fs
CKO clock frequency	384fs	256fs
Internal clock frequency (t_{SYS})	$2 \times t_{XI}$	t_{XI}

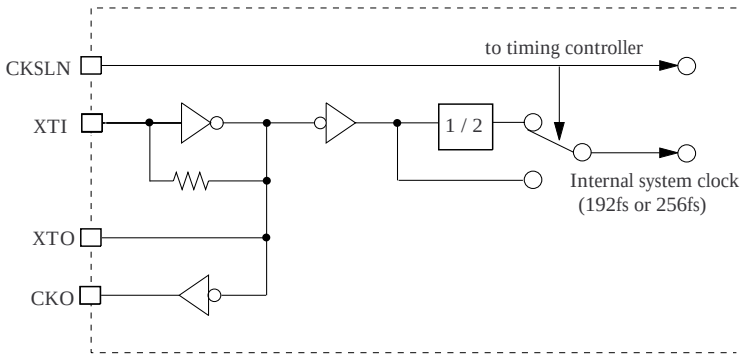


Figure 5. Clock generator circuit

Audio Data Input (INF1N, INF2N, IW1N, IW2N, DI, DIL, DIR, BCKI, LRCI)

The input data format and several input pin functions are selected by the state of INF1N and INF2N.

INF1N	DI/INF2N	Input format	Pin function selection		
			DI/INF2N	IW1N/DIL	IW2N/DIR
LOW	LOW	LR alternating[1], trailing data	DI	IW1N	IW2N
LOW	HIGH				
HIGH	LOW	LR alternating, leading data	INF2N	DIL	DIR
HIGH	HIGH	LR simultaneous[2], leading data			

1. Alternating left-channel and right-channel data input on a single input DI.
2. Simultaneous left-channel and right-channel data input on two inputs, DIL and DIR, respectively.

The input data word length is selected by the state of IW1N and IW2N when INF1N is LOW. 20-bit is selected when INF1N is HIGH.

INF1N	IW2N/DIL	IW1N/DIR	Input bit length
LOW	LOW	LOW	20 bits
	LOW	HIGH	20 bits
	HIGH	LOW	18 bits
	HIGH	HIGH	16 bits
HIGH	×	×	20 bits

Jitter-free Function (SYNCN)

The arithmetic circuit and output control timing is derived from the system clock, and is therefore independent of the input LRCI and BCKI clocks. Accordingly, any jitter in the data input clock (LRCI and BCKI) does not cause jitter in the output.

Generally, the internal timing is synchronized to the LRCI input timing after a system reset release, when RSTN goes from LOW to HIGH, on the first LRCI clock start edge. If the input timing and LRCI start edge timing subsequently drift, the input timing is automatically resynchronized when the timing error exceeds a certain value. There are 2 timing error values at which resynchronization occurs, selected by the state of SYNCN.

Jitter-free mode (SYNCN = HIGH)

When SYNCN is HIGH, the timing error value is ±3/8 × (LRCI clock period). When the difference between the input timing and LRCI start edge position do not exceed this value, internal timing is not resynchronized and all functions continue to operate normally.

Sync mode (SYNCN = LOW)

When SYNCN is LOW, the timing error value is ±1 × (system clock period), which is a much smaller timing error tolerance than in jitter-free mode. In this mode, the internal timing is guaranteed to follow the LRCI clock timing within this tolerance, making this mode useful for systems constructed from a multiple number of SM5843A×1 devices.

Note that resynchronization affects the internal operation and can generate a momentary click noise output.

Audio Data Output (DOL, DOR, BCKO, WCKO, OW20N)

The output data is in serial, simultaneous left and right-channel, 2s complement, MSB first, BCKO burst (NPC format) format. The output data word length is selected by the state of OW20N. 18-bit output is selected when OW20N is HIGH, and 20-bit output when OW20N is LOW.

8fs serial data is output in sync with the falling edge of the internal system clock and BCKO clock. The number of BCKO bit clock pulses per word changes depending on the output bit length selected (18/20 bits). Consequently, output data is latched into the internal output register on the falling of the edge of an output word clock WCKO, which has timing independent of the number of output bits as specified in the following table.

Parameter	Symbol	CKSLN = HIGH	CKSLN = LOW
Bit clock rate	T_B	1/192fs	1/256fs
Data word length	T_{DW}	$24t_{SYS}$	$32t_{SYS}$

System Reset (RSTN)

The SM5843A×1 must be reset under the following conditions.

- At power-ON.
- When the LRCI clock and internal operation timing need to be resynchronized.
- When switching the CKSLN clock select input.
- When switching between filter characteristics using TMOD2.
- When either or both of the LRCI and XTI clocks stop or are interrupted.

The system is reset by applying a LOW-level pulse on RSTN.

The arithmetic and output timing counters are reset on the first LRCI start edge after reset is released, as long as the XTI clock has already stabilized. The LRCI start edge is determined by the state of INF1N and INF2N. When INF1N is LOW or when both INF1N and INF2N are HIGH, the start edge is the rising edge. When INF1N is HIGH and INF2N is LOW, the start edge is the falling edge.

When RSTN is LOW, the DOL and DOR outputs are LOW, muting the output signal to an attenuation level of −∞.

The power-ON reset pulse can be applied by a microcontroller or, for systems where XTI and LRCI are stable at power-ON, by connecting a capacitor of several hundred pF between RSTN and VSS. For systems that do not use a microcontroller, the capacitor must be chosen such that the XTI and LRCI clocks fully stabilize before RSTN goes from LOW to HIGH.

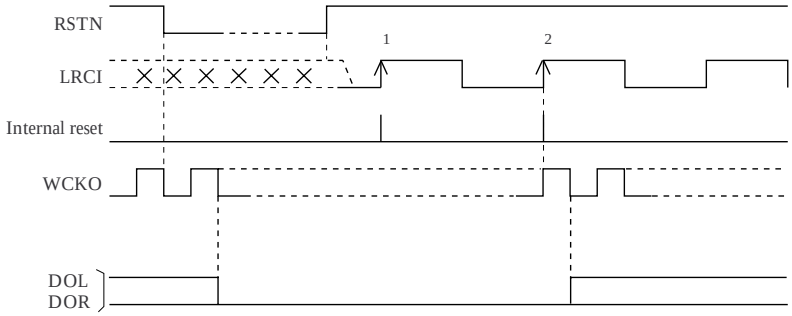


Figure 6. System reset timing and output muting

Filter Characteristic Selection (TMOD2)

There are 2 digital filter frequency response characteristics incorporated into the SM5843A×1, selected by the state of TMOD2. A sharp roll-off characteristic (response 1) is selected when TMOD2 is HIGH, and a slow roll-off characteristic (response 2) when TMOD2 is LOW. The response is modified by changing the number of taps in the 1st FIR filter stage, as shown in figure 1.

- Filter response 1
  - 153-tap 1st FIR
  - 29-tap 2nd FIR
  - 17-tap 3rd FIR
- Filter response 2
  - 25-tap 1st FIR
  - 29-tap 2nd FIR
  - 17-tap 3rd FIR

Note that the device should be reset when changing TMOD2 during normal operation.

Dither Rounding-off Processing (TMOD1)

Dither rounding-off processing of output data is ON when TMOD1 is LOW. Dither is OFF and normal processing mode is selected when TMOD1 is HIGH.

TIMING DIAGRAMS

Input Timing Examples (DIN, BCKI, LRCI)

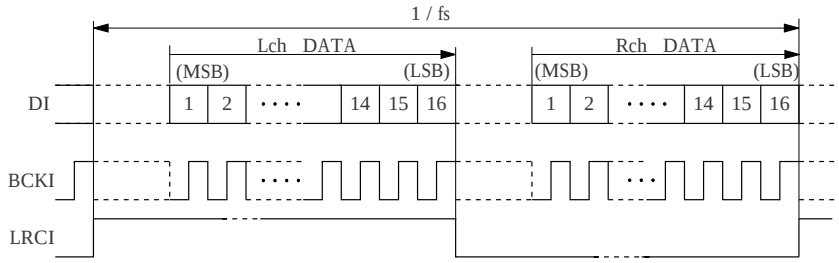
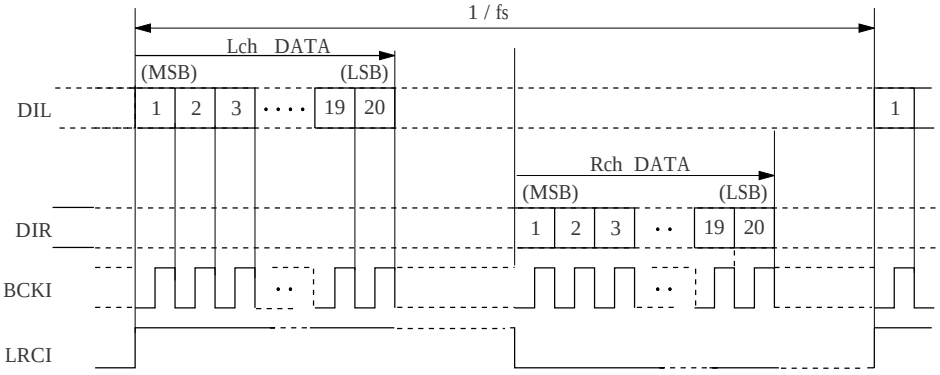
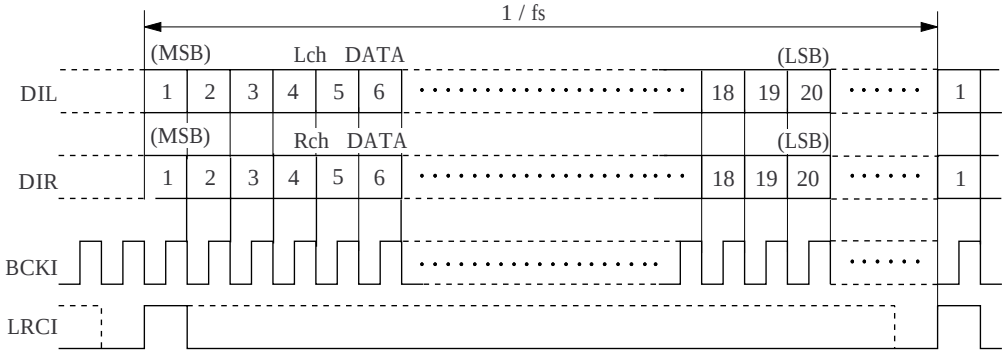


Figure 7. LR alternating, trailing data, 16-bit input



Data after lsb (bit 20) is ignored. After bit 20, BCKI clock input is not needed.

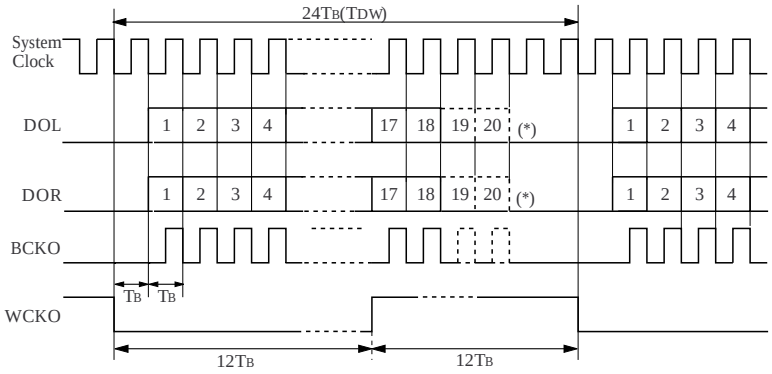
Figure 8. LR alternating, leading data, 20-bit input



Data after lsb (bit20) is ignored. After bit 20, BCKI clock input is not needed.

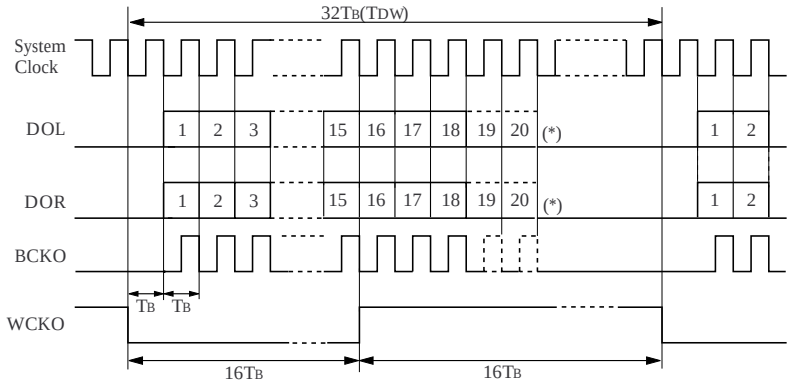
Figure 9. LR simultaneous, leading data, 20-bit input

Output Timing Examples (DOL, DOR, BCKO, WCKO)



The number of output bits is determined by the output bit length selected.

Figure 10. 18/20-bit output ($\overline{CKSL}$ = HIGH)



The number of output bits is determined by the output bit length selected.

Figure 11. 18/20-bit output ($\overline{CKSL}$ = LOW)

Data Input to Output Delay Timing

This is the digital filter arithmetic computation time from the completion of data input at rate fs (t_{INPUT}) on the rising edge of LRCI to the start of data output at rate 8fs (t_{OUTPUT}) on the falling edge of WCKO.

Filter response	CKSLN	SYNCN	Mode	$t_{OUTPUT} - t_{INPUT}$
Filter response 1	LOW (256fs)	LOW	After reset + sync mode	44.625/fs
		HIGH	Jitter-free mode	44.25/fs – 45.0/fs
	HIGH (384fs)	LOW	After reset + sync mode	44.75/fs
		HIGH	Jitter-free mode	44.375/fs – 45.125/fs
Filter response 2	LOW (256fs)	LOW	After reset + sync mode	25.625/fs
		HIGH	Jitter-free mode	25.25/fs – 26.0/fs
	HIGH (384fs)	LOW	After reset + sync mode	25.75/fs
		HIGH	Jitter-free mode	25.375/fs – 26.125/fs

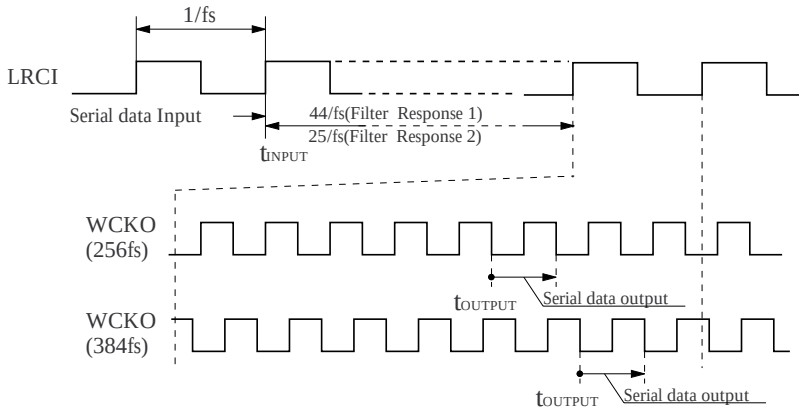


Figure 12. Delay timing (SYNCN = LOW)

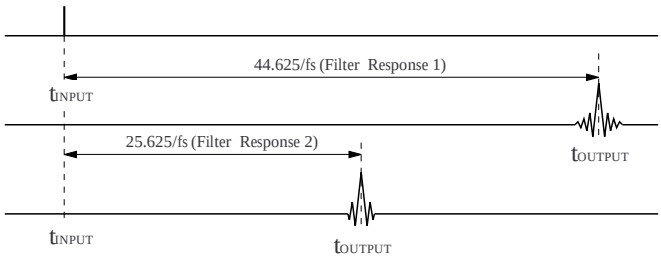
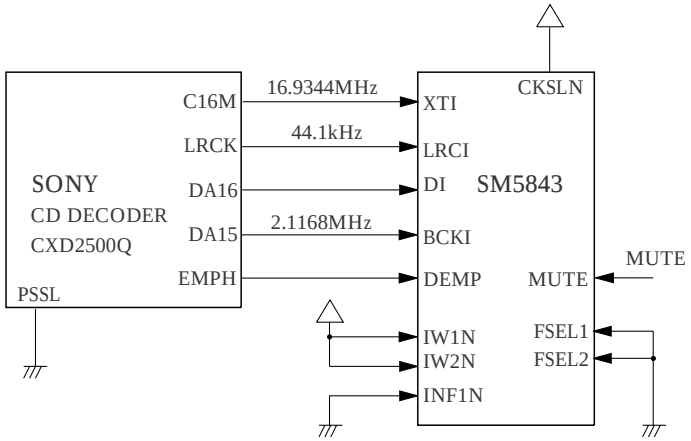


Figure 13. Delay timing (SYNCN = CKSLN = LOW)

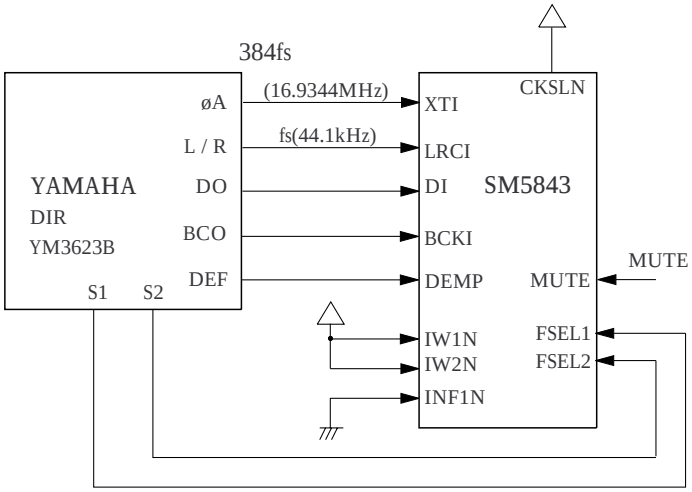
APPLICATION CIRCUITS

Input Interface Circuits

CD decoder (CXD2500Q) connection

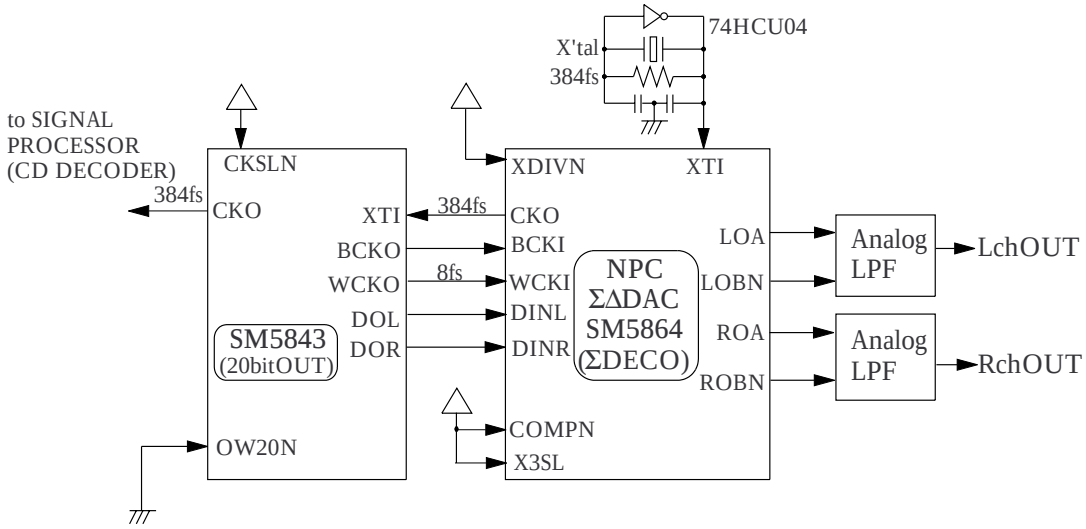


Digital audio interface receiver (YM3623B) connection



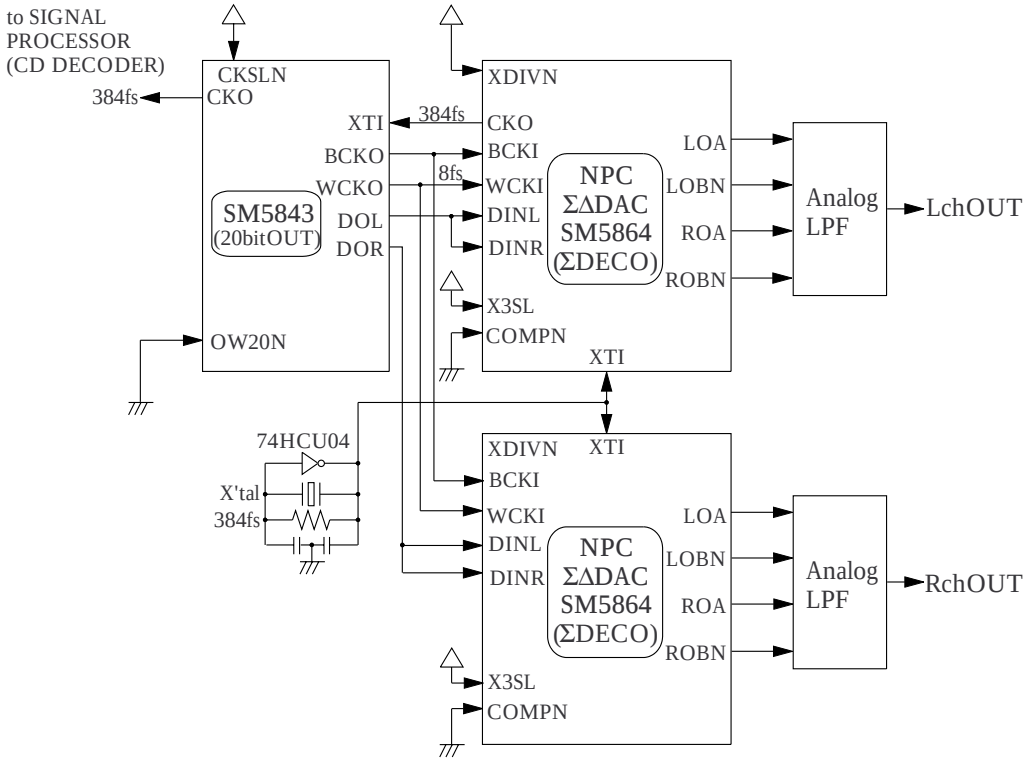
Output Interface Circuits

20-bit input ΣΔ DAC (SM5864AP) connection 1



20-bit input ΣΔ DAC (SM5864AP) connection 2

L/R-channel independent complementary PWM output



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