Integrated Device Technology, Inc.

# FAST CMOS OCTAL D FLIP-FLOP WITH MASTER RESET

**IDT54/74FCT273T/AT/CT**

## FEATURES:

- Std., A, and C speed grades
- Low input and output leakage ≤1µA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH}$ = 3.3V (typ.)
  - $V_{OL}$ = 0.3V (typ.)
- High drive outputs (-15mA $I_{OH}$, 48mA $I_{OL}$)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

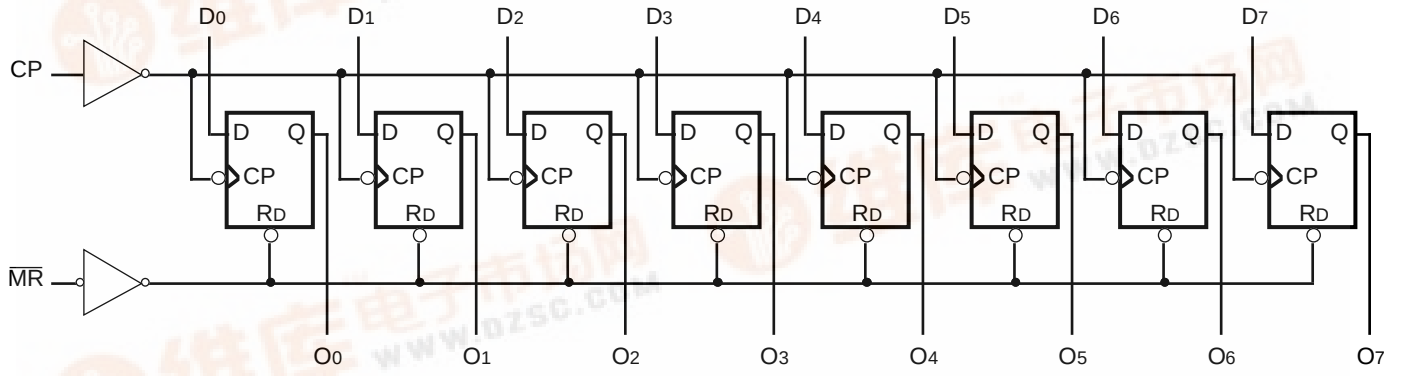
## DESCRIPTION:

The IDT54/74FCT273T/AT/CT are octal D flip-flops built using an advanced dual metal CMOS technology. The IDT54/74FCT273T/AT/CT have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

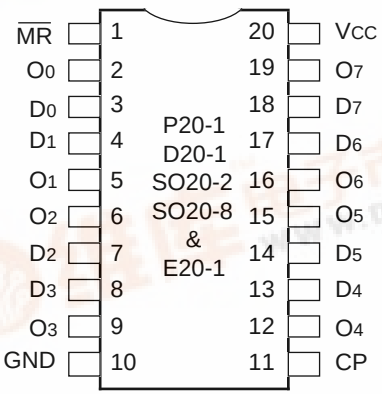
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

## FUNCTIONAL BLOCK DIAGRAM




2568 drw 03

## PIN CONFIGURATIONS

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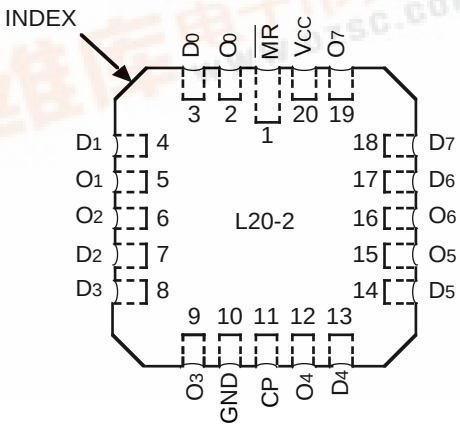
**DIP/SOIC/QSOP/CERPACK TOP VIEW**




2568 drw 02

**LCC TOP VIEW**

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| $D_N$ | Data Inputs |
| $\overline{MR}$ | Master Reset (Active LOW) |
| CP | Clock Pulse Input (Active Rising Edge) |
| $O_N$ | Data Outputs |

2568 tbl 01

## FUNCTION TABLE(1)

| Operating Mode | Inputs | | | Outputs |
|---|---|---|---|---|
| | $\overline{MR}$ | CP | $D_N$ | $O_N$ |
| Reset (Clear) | L | X | X | L |
| Load "1" | H | ↑ | h | H |
| Load "0" | H | ↑ | I | L |

**NOTE:**
2568 tbl 02

1. H = HIGH voltage level steady state
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
   L = LOW voltage level steady state
   I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7.0 | –0.5 to +7.0 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ +0.5 | –0.5 to $V_{CC}$ +0.5 | V |
| $T_A$ | Operating Temperature | 0 to +70 | –55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | –65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 0.5 | 0.5 | W |
| $I_{OUT}$ | DC Output Current | –60 to +120 | –60 to +120 | mA |

**NOTES:**
2568 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed $V_{CC}$ by +0.5V unless otherwise noted.
2. Input and $V_{CC}$ terminals only.
3. Outputs and I/O terminals only.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 8 | 12 | pF |

**NOTE:**
2568 lnk 04

1. This parameter is measured at characterization but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current[4] | $V_{CC}$ = Max. | $V_I$ = 2.7V | — | — | ±1 | µA |
| $I_{IL}$ | Input LOW Current[4] | $V_{CC}$ = Max. | $V_I$ = 0.5V | — | — | ±1 | µA |
| $I_I$ | Input HIGH Current[4] | $V_{CC}$ = Max., $V_I$ = $V_{CC}$ (Max.) | | — | — | ±1 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_N$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max.[3], $V_O$ = GND | | –60 | –120 | –225 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –6mA MIL.<br>$I_{OH}$ = –8mA COM'L. | 2.4 | 3.3 | — | V |
| | | | $I_{OH}$ = –12mA MIL.<br>$I_{OH}$ = –15mA COM'L. | 2.0 | 3.0 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 32mA MIL.<br>$I_{OL}$ = 48mA COM'L. | — | 0.3 | 0.5 | V |
| $V_H$ | Input Hysteresis | — | | — | 200 | — | mV |
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max.<br>$V_{IN}$ = GND or $V_{CC}$ | | — | 0.01 | 1 | mA |

2568 tbl 05

**NOTES:**
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test parameter for this parameter is ±5µA at $T_A$ = -55°C.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>$\overline{MR}$ = $V_{CC}$<br>One Input Toggling<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 0.15 | 0.25 | mA/<br>MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>$f_{CP}$= 10MHz<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 1.5 | 3.5 | mA |
| | | $\overline{MR}$ = $V_{CC}$<br>One Bit Toggling<br>at fi = 5MHz<br>50% Duty Cycle | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 2.0 | 5.5 | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>$f_{CP}$= 10MHz<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 3.8 | 7.3[5] | |
| | | $\overline{MR}$ = $V_{CC}$<br>Eight Bits Toggling<br>at fi = 2.5MHz<br>50% Duty Cycle | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 6.0 | 16.3[5] | |

**NOTES:**

2568 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V); all other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$
   All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

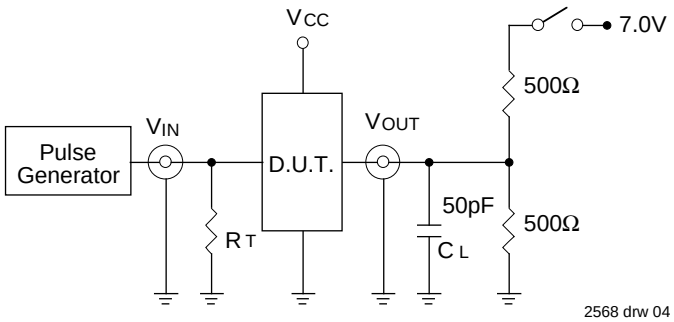
| Symbol | Parameter | Condition[1] | IDT54/74FCT273T | | | | IDT54/74FCT273AT | | | | IDT54/74FCT273CT | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CP to $O_N$ | CL = 50pF<br>RL = 500Ω | 2.0 | 13.0 | 2.0 | 15.0 | 2.0 | 7.2 | 2.0 | 8.3 | 2.0 | 5.8 | 2.0 | 6.5 | ns |
| $t_{PHL}$ | Propagation Delay<br>$\overline{MR}$ to $O_N$ | | 2.0 | 13.0 | 2.0 | 15.0 | 2.0 | 7.2 | 2.0 | 8.3 | 2.0 | 6.1 | 2.0 | 6.8 | ns |
| $t_{SU}$ | Set-up Time HIGH or LOW<br>$D_N$ to CP | | 3.0 | — | 3.5 | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| $t_H$ | Hold Time HIGH or LOW $D_N$<br>to CP | | 2.0 | — | 2.0 | — | 1.5 | — | 1.5 | — | 1.5 | — | 1.5 | — | ns |
| $t_W$ | CP Pulse Width HIGH or<br>LOW | | 7.0 | — | 7.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | ns |
| $t_W$ | $\overline{MR}$ Pulse Width LOW | | 7.0 | — | 7.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | ns |
| $t_{REM}$ | Recovery Time $\overline{MR}$<br>to CP | | 4.0 | — | 5.0 | — | 2.0 | — | 2.5 | — | 2.0 | — | 2.5 | — | ns |

**NOTES:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2568 tbl 07

# TEST CIRCUITS AND WAVEFORMS

## TEST CIRCUITS FOR ALL OUTPUTS




2568 drw 04

## SWITCH POSITION

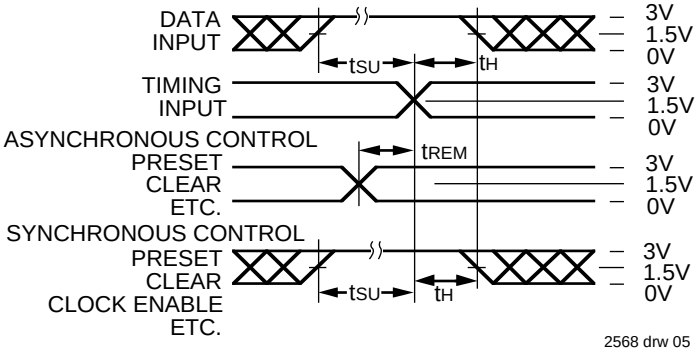
| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

2568 lnk 08

**DEFINITIONS:**

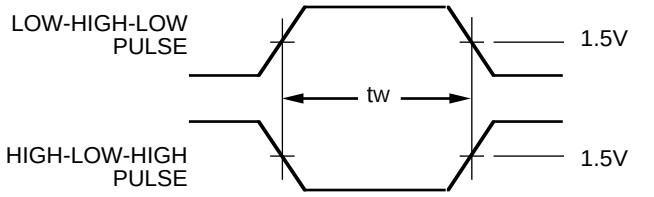
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## SET-UP, HOLD AND RELEASE TIMES



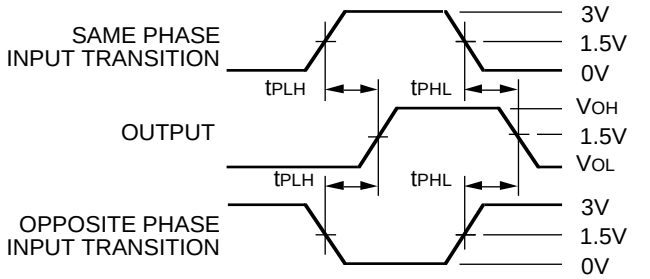

2568 drw 05

## PULSE WIDTH



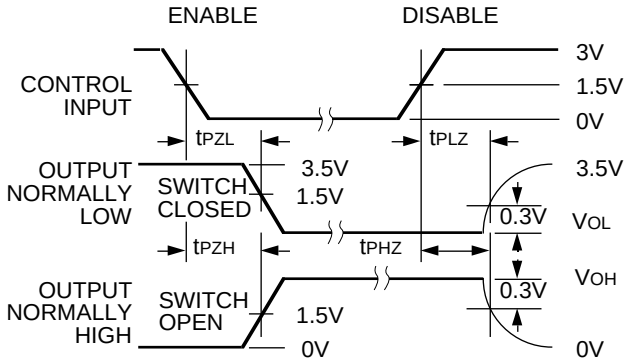

2568 drw 06

## PROPAGATION DELAY




2568 drw 07

## ENABLE AND DISABLE TIMES

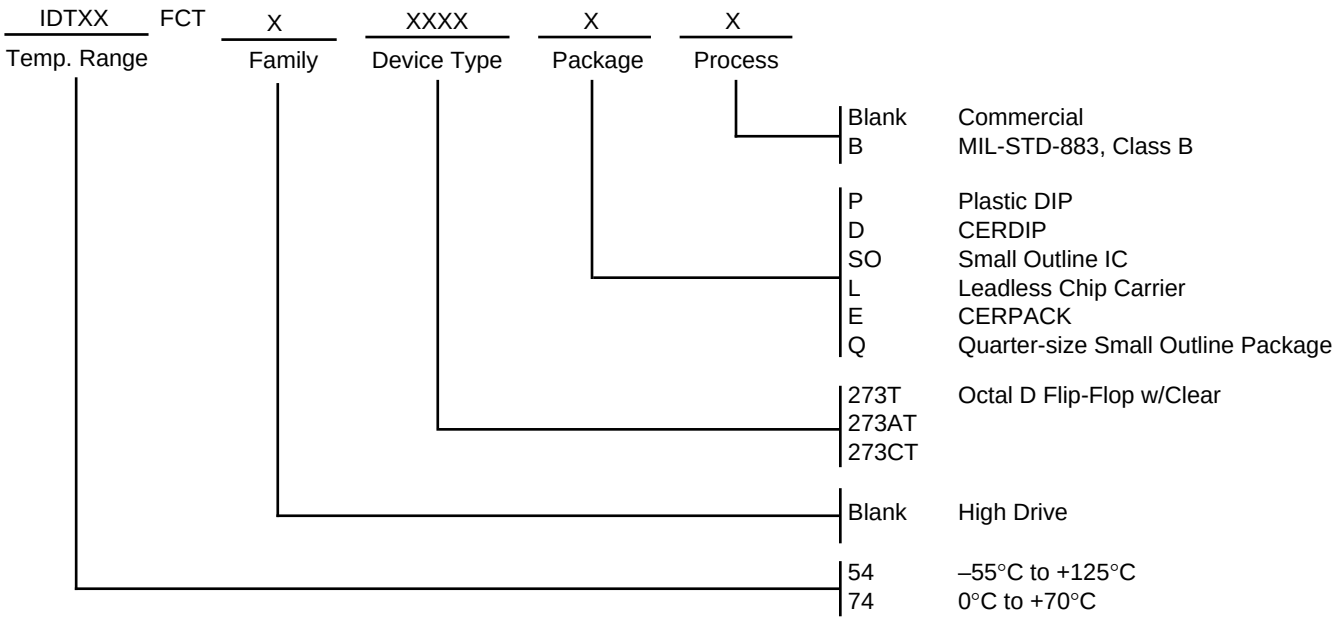



2568 drw 08

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns

## ORDERING INFORMATION

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