

MC14043B, MC14044B

CMOS MSI

Quad R–S Latches

The MC14043B and MC14044B quad R–S latches are constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three–state buffers having a common enable input. The outputs are enabled with a logical “1” or high on the enable input; a logical “0” or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Double Diode Input Protection
- Three–State Outputs with Common Enable
- Outputs Capable of Driving Two Low–power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|-------------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in}, I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 3.) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | $^{\circ}C$ |
| T_{stg} | Storage Temperature Range | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature (8–Second Soldering) | 260 | $^{\circ}C$ |

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
Plastic “P and D/DW” Packages: - 7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

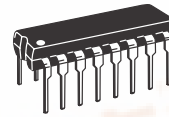
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



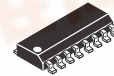
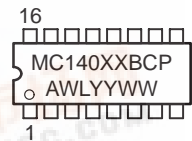
ON Semiconductor

<http://onsemi.com>

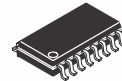


PDIP–16
P SUFFIX
CASE 648

MARKING DIAGRAMS



SOIC–16
D SUFFIX
CASE 751B



SOEIAJ–16
F SUFFIX
CASE 966



XX = Specific Device Code
A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

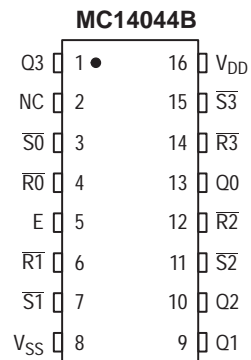
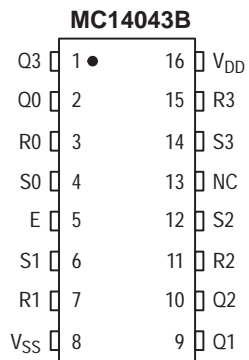
| Device | Package | Shipping |
|-------------|-----------|------------------|
| MC14043BCP | PDIP–16 | 2000/Box |
| MC14043BD | SOIC–16 | 2400/Box |
| MC14043BDR2 | SOIC–16 | 2500/Tape & Reel |
| MC14043BF | SOEIAJ–16 | See Note 1. |
| MC14043BFEL | SOEIAJ–16 | See Note 1. |
| MC14044BCP | PDIP–16 | 2000/Box |
| MC14044BD | SOIC–16 | 2400/Box |
| MC14044BDR2 | SOIC–16 | 2500/Tape & Reel |

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

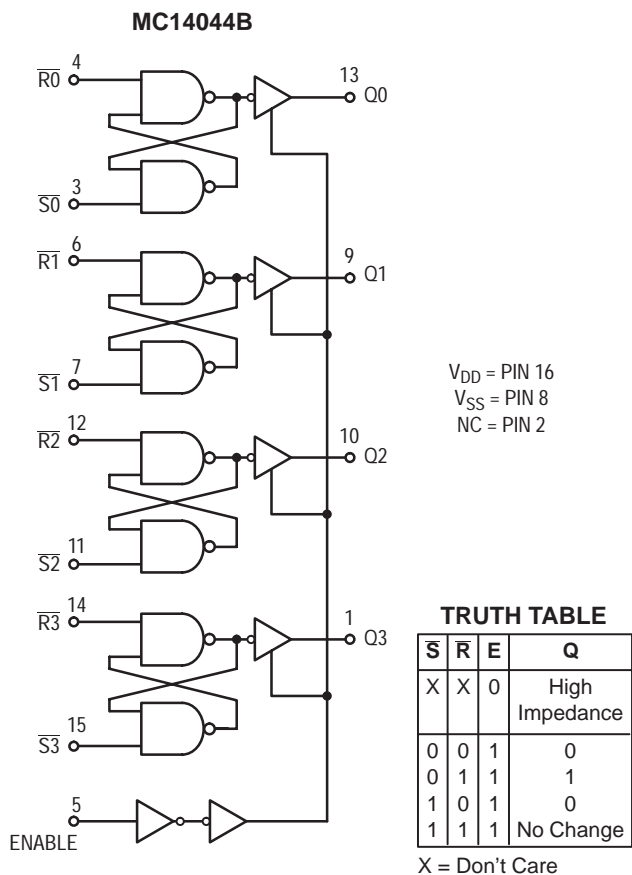
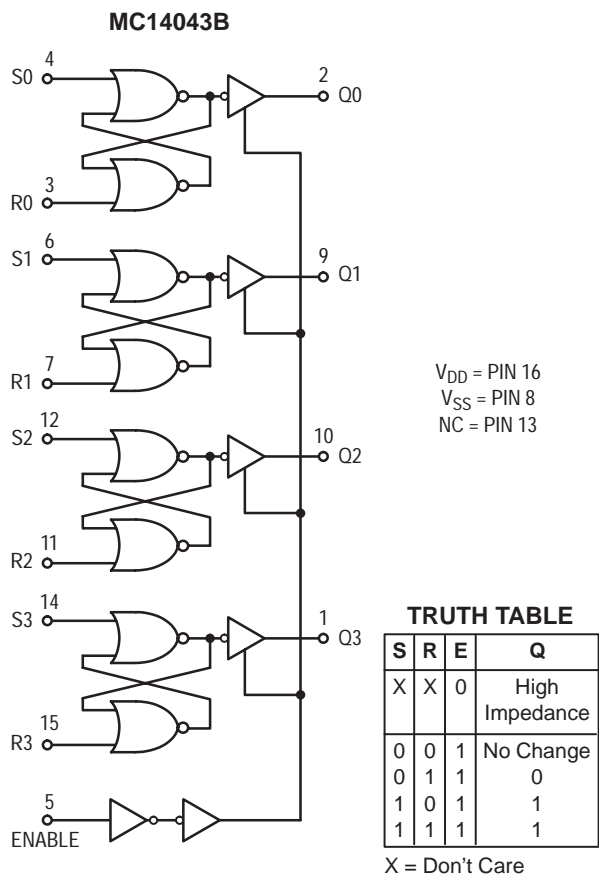


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PIN ASSIGNMENT



NC = NO CONNECTION



MC14043B, MC14044B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V_{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit | |
|---|---------------------------|-----------------|---|-----------|-------|--------------------|-----------|-------|-----------|-----------|------|
| | | | Min | Max | Min | Typ ⁽⁴⁾ | Max | Min | Max | | |
| Output Voltage $V_{in} = V_{DD}$ or 0 $V_{in} = 0$ or V_{DD} | "0" Level V_{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc | |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | |
| | "1" Level V_{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | | Vdc |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | | |
| Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc) ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc) | "0" Level V_{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc | |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | | |
| | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | | |
| | "1" Level V_{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | | Vdc |
| | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | | |
| | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | | |
| Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc) | Source I_{OH} | 5.0 | -3.0 | — | -2.4 | -4.2 | — | -1.7 | — | mAdc | |
| | | 5.0 | -0.64 | — | -0.51 | -0.88 | — | -0.36 | — | | |
| | | 10 | -1.6 | — | -1.3 | -2.25 | — | -0.9 | — | | |
| | | 15 | -4.2 | — | -3.4 | -8.8 | — | -2.4 | — | | |
| | Sink I_{OL} | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | | mAdc |
| | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | | |
| 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | — | | | |
| Input Current | I_{in} | 15 | — | ± 0.1 | — | ± 0.00001 | ± 0.1 | — | ± 1.0 | μ Adc | |
| Input Capacitance ($V_{in} = 0$) | C_{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF | |
| Quiescent Current (Per Package) | I_{DD} | 5.0 | — | 1.0 | — | 0.002 | 1.0 | — | 30 | μ Adc | |
| | | 10 | — | 2.0 | — | 0.004 | 2.0 | — | 60 | | |
| | | 15 | — | 4.0 | — | 0.006 | 4.0 | — | 120 | | |
| Total Supply Current ^(5.) ^(6.) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs all buffers switching) | I_T | 5.0 | $I_T = (0.58 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | μ Adc | |
| | | 10 | $I_T = (1.15 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | | |
| | | 15 | $I_T = (1.73 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | | |
| Three-State Output Leakage Current | I_{TL} | 15 | — | ± 0.1 | — | ± 0.0001 | ± 0.1 | — | ± 3.0 | μ Adc | |

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.004$.

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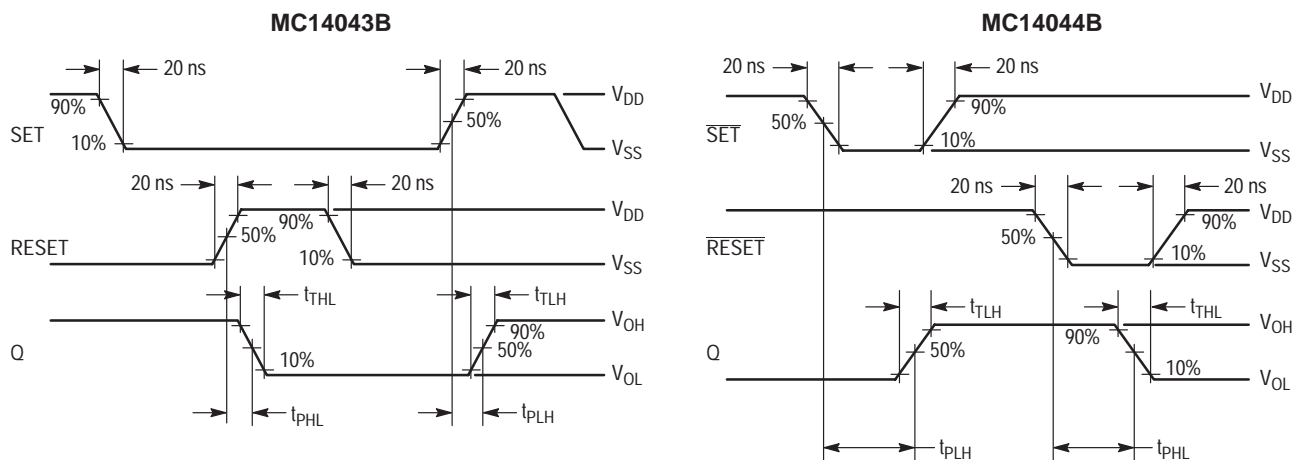
SWITCHING CHARACTERISTICS (7.) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} Vdc | Min | Typ (8.) | Max | Unit |
|--|--|-----------------|------------------|-----------------|-------------------|------|
| Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$ | t_{TLH} | 5.0 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$ | t_{THL} | 5.0 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time $t_{PLH} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PLH} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$ | t_{PLH} | 5.0 10 15 | — — — | 175 75 60 | 350 175 120 | ns |
| | t_{PHL} | 5.0 10 15 | — — — | 175 75 60 | 350 175 120 | ns |
| Set, $\overline{\text{Set}}$ Pulse Width | t_W | 5.0 10 15 | 200 100 70 | 80 40 30 | — — — | ns |
| Reset, $\overline{\text{Reset}}$ Pulse Width | t_W | 5.0 10 15 | 200 100 70 | 80 40 30 | — — — | ns |
| Three-State Enable/Disable Delay | t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH} | 5.0 10 15 | — — — | 150 80 55 | 300 160 110 | ns |

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

AC WAVEFORMS

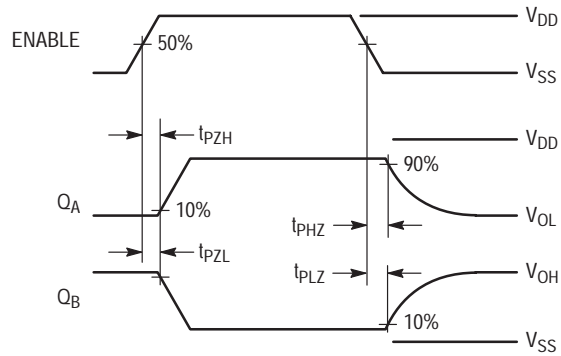
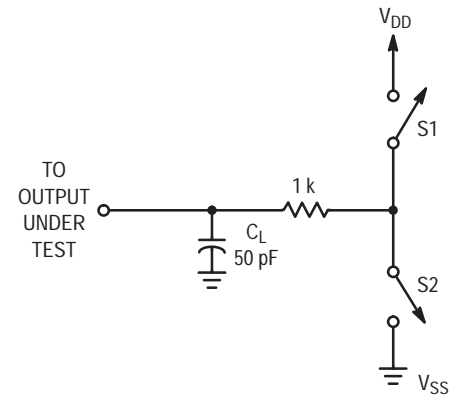


MC14043B, MC14044B

THREE-STATE ENABLE/DISABLE DELAYS

Set, Reset, Enable, and Switch Conditions for 3-State Tests

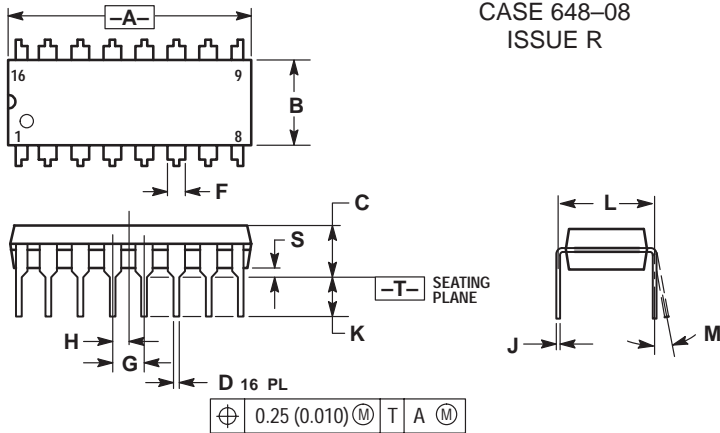
| Test | Enable | S1 | S2 | Q | MC14043B | | MC14044B | |
|-----------|--------|--------|--------|---|----------|----------|-----------|----------|
| | | | | | S | R | \bar{S} | R |
| t_{PZH} | | Open | Closed | A | V_{DD} | V_{SS} | V_{SS} | V_{DD} |
| t_{PZL} | | Closed | Open | B | V_{SS} | V_{DD} | V_{DD} | V_{SS} |
| t_{PHZ} | | Open | Closed | A | V_{DD} | V_{SS} | V_{SS} | V_{DD} |
| t_{PLZ} | | Closed | Open | B | V_{SS} | V_{DD} | V_{DD} | V_{SS} |



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PACKAGE DIMENSIONS

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

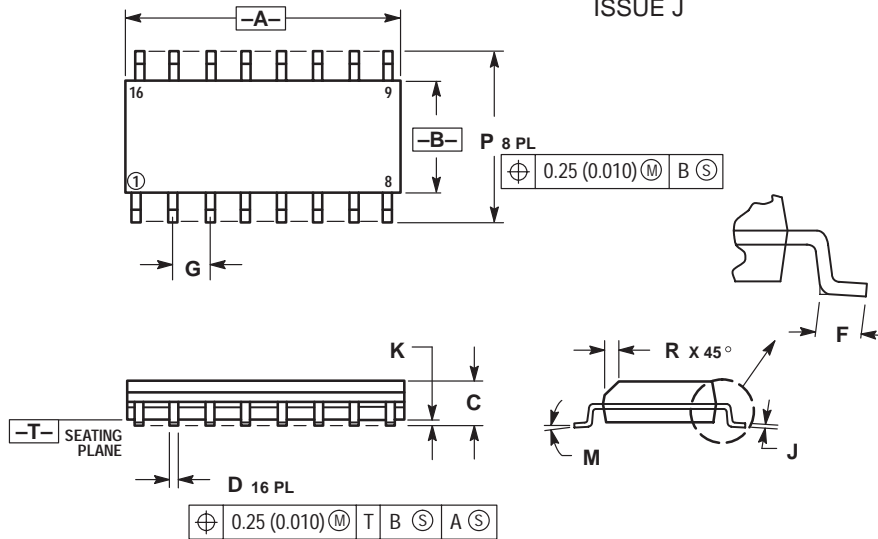


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

SOIC-16 D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

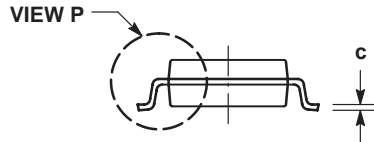
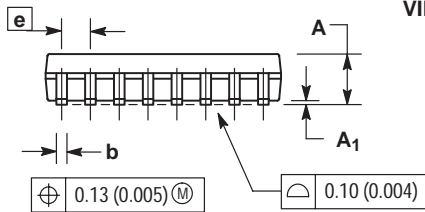
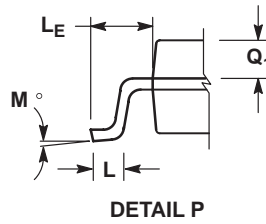
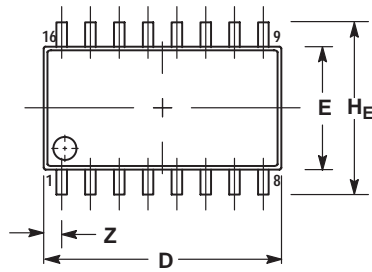
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

MC14043B, MC14044B

PACKAGE DIMENSIONS

SOEIAJ-16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966-01
ISSUE O




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| HE | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| LE | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

MC14043B, MC14044B

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