National Semiconductor

October 1989

# CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
# CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
# CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

## General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD}=5V$, $V_{SS}=0V$ and $V_{EE}=-5V$, analog signals from −5V to +5V can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs. A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

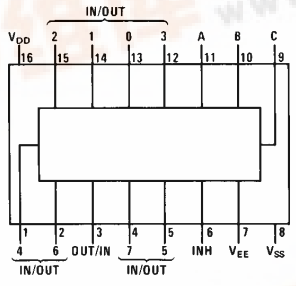
## Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to $15V_{p-p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD}-V_{EE}=15V$
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at $V_{DD}-V_{EE}=10V$
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD}-V_{SS}=3-15V$) to switch analog signals to 15 $V_{p-p}$ ($V_{DD}-V_{EE}=15V$)
- Matched switch characteristics: $\Delta R_{ON}=5\Omega$ (typ.) for $V_{DD}-V_{EE}=15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at $V_{DD}-V_{SS}=V_{DD}-V_{EE}=10V$
- Binary address decoding on chip

## Connection Diagrams

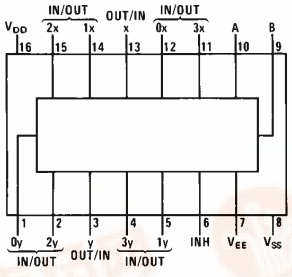
**Dual-In-Line Packages**

**CD4051BM/CD4051BC**



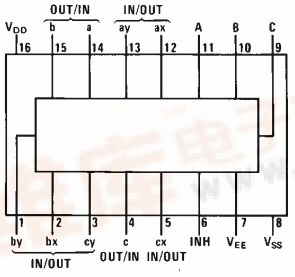

TOP VIEW

**CD4052BM/CD4052BC**




TOP VIEW

**CD4053BM/CD4053BC**




TOP VIEW

TL/F/5662–1

**Order Number CD4051B, CD4052B, or CD4053B**



RRD-B30M105/Printed in U. S. A.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| DC Supply Voltage ($V_{DD}$) | $-0.5\ V_{DC}$ to $+18\ V_{DC}$ |
| Input Voltage ($V_{IN}$) | $-0.5\ V_{DC}$ to $V_{DD}+0.5\ V_{DC}$ |
| Storage Temperature Range ($T_S$) | $-65°C$ to $+150°C$ |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temp. ($T_L$) (soldering, 10 sec.) | 260°C |

## Recommended Operating Conditions

| | |
|---|---|
| DC Supply Voltage ($V_{DD}$) | $+5\ V_{DC}$ to $+15\ V_{DC}$ |
| Input Voltage ($V_{IN}$) | 0V to $V_{DD}\ V_{DC}$ |
| Operating Temperature Range ($T_A$) | |
| 4051BM/4052BM/4053BM | $-55°C$ to $+125°C$ |
| 4051BC/4052BC/4053BC | $-40°C$ to $+85°C$ |

## DC Electrical Characteristics (Note 2)

| Symbol | Parameter | Conditions | | −55°C | | +25° | | | +125°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{DD}$ | Quiescent Device Current | $V_{DD}=5V$<br>$V_{DD}=10V$<br>$V_{DD}=15V$ | | | 5<br>10<br>20 | | | 5<br>10<br>20 | | 150<br>300<br>600 | $\mu A$<br>$\mu A$<br>$\mu A$ |
| **Signal Inputs ($V_{IS}$) and Outputs ($V_{OS}$)** | | | | | | | | | | | |
| $R_{ON}$ | "ON" Resistance (Peak for $V_{EE} \le V_{IS} \le V_{DD}$) | $R_L=10\ k\Omega$ (any channel selected) | $V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$ | | 800 | | 270 | 1050 | | 1300 | $\Omega$ |
| | | | $V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$ | | 310 | | 120 | 400 | | 550 | $\Omega$ |
| | | | $V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$ | | 200 | | 80 | 240 | | 320 | $\Omega$ |
| $\Delta R_{ON}$ | $\Delta$"ON" Resistance Between Any Two Channels | $R_L=10\ k\Omega$ (any channel selected) | $V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$ | | | | 10 | | | | $\Omega$ |
| | | | $V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$ | | | | 10 | | | | $\Omega$ |
| | | | $V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$ | | | | 5 | | | | $\Omega$ |
| | "OFF" Channel Leakage Current, any channel "OFF" | $V_{DD}=7.5V$, $V_{EE}=-7.5V$<br>O/I = ±7.5V, I/O = 0V | | | ±50 | | ±0.01 | ±50 | | ±500 | nA |
| | "OFF" Channel Leakage Current, all channels | Inhibit = 7.5V | CD4051 | | ±200 | | ±0.08 | ±200 | | ±2000 | nA |
| | "OFF" (Common OUT/IN) | $V_{DD}=7.5V$, $V_{EE}=-7.5V$, O/I = 0V, | CD4052 | | ±200 | | ±0.04 | ±200 | | ±2000 | nA |
| | | I/O = ±7.5V | CD4053 | | ±200 | | ±0.02 | ±200 | | ±2000 | nA |
| **Control Inputs A, B, C and Inhibit** | | | | | | | | | | | |
| $V_{IL}$ | Low Level Input Voltage | $V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to $V_{SS}$<br>$I_{IS}<2\ \mu A$ on all OFF channels<br>$V_{IS}=V_{DD}$ thru 1 kΩ | | | | | | | | | |
| | | $V_{DD}=5V$ | | | 1.5 | | | 1.5 | | 1.5 | V |
| | | $V_{DD}=10V$ | | | 3.0 | | | 3.0 | | 3.0 | V |
| | | $V_{DD}=15V$ | | | 4.0 | | | 4.0 | | 4.0 | V |
| $V_{IH}$ | High Level Input Voltage | $V_{DD}=5$ | | 3.5 | | 3.5 | | | 3.5 | | V |
| | | $V_{DD}=10$ | | 7 | | 7 | | | 7 | | V |
| | | $V_{DD}=15$ | | 11 | | 11 | | | 11 | | V |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** All voltages measured with respect to $V_{SS}$ unless otherwise specified.

## DC Electrical Characteristics (Note 2) (Continued)

| Symbol | Parameter | Conditions | | −40°C | | +25°C | | | +85°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Typ | Max | Min | Max | |
| $I_{IN}$ | Input Current | $V_{DD}=15V$, $V_{EE}=0V$<br>$V_{IN}=0V$ | | | −0.1 | | $-10^{-5}$ | −0.1 | | −1.0 | μA |
| | | $V_{DD}=15V$, $V_{EE}=0V$<br>$V_{IN}=15V$ | | | 0.1 | | $10^{-5}$ | 0.1 | | 1.0 | μA |
| $I_{DD}$ | Quiescent Device Current | $V_{DD}=5V$ | | | 20 | | | 20 | | 150 | μA |
| | | $V_{DD}=10V$ | | | 40 | | | 40 | | 300 | μA |
| | | $V_{DD}=15V$ | | | 80 | | | 80 | | 600 | μA |
| **Signal Inputs ($V_{IS}$) and Outputs ($V_{OS}$)** | | | | | | | | | | | |
| $R_{ON}$ | "ON" Resistance (Peak for $V_{EE} \le V_{IS} \le V_{DD}$) | $R_L=10\ k\Omega$ (any channel selected) | $V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$ | | 850 | | 270 | 1050 | | 1200 | Ω |
| | | | $V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$ | | 330 | | 120 | 400 | | 520 | Ω |
| | | | $V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$ | | 210 | | 80 | 240 | | 300 | Ω |
| $\Delta R_{ON}$ | Δ"ON" Resistance Between Any Two Channels | $R_L=10\ k\Omega$ (any channel selected) | $V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$ | | | | 10 | | | | Ω |
| | | | $V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$ | | | | 10 | | | | Ω |
| | | | $V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$ | | | | 5 | | | | Ω |
| | "OFF" Channel Leakage Current, any channel "OFF" | $V_{DD}=7.5V$, $V_{EE}=-7.5V$<br>$O/I=\pm7.5V$, $I/O=0V$ | | | ±50 | | ±0.01 | ±50 | | ±500 | nA |
| | "OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN) | Inhibit = 7.5V | CD4051 | | ±200 | | ±0.08 | ±200 | | ±2000 | nA |
| | | $V_{DD}=7.5V$, $V_{EE}=-7.5V$, $O/I=0V$ | CD4052 | | ±200 | | ±0.04 | ±200 | | ±2000 | nA |
| | | $I/O=\pm7.5V$ | CD4053 | | ±200 | | ±0.02 | ±200 | | ±2000 | nA |
| **Control Inputs A, B, C and Inhibit** | | | | | | | | | | | |
| $V_{IL}$ | Low Level Input Voltage | $V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to $V_{SS}$<br>$I_{IS}<2\ \mu A$ on all OFF Channels<br>$V_{IS}=V_{DD}$ thru 1 kΩ | | | | | | | | | |
| | | $V_{DD}=5V$ | | | 1.5 | | | 1.5 | | 1.5 | V |
| | | $V_{DD}=10V$ | | | 3.0 | | | 3.0 | | 3.0 | V |
| | | $V_{DD}=15V$ | | | 4.0 | | | 4.0 | | 4.0 | V |
| $V_{IH}$ | High Level Input Voltage | $V_{DD}=5$ | | 3.5 | | 3.5 | | | 3.5 | | V |
| | | $V_{DD}=10$ | | 7 | | 7 | | | 7 | | V |
| | | $V_{DD}=15$ | | 11 | | 11 | | | 11 | | V |
| $I_{IN}$ | Input Current | $V_{DD}=15V$, $V_{EE}=0V$<br>$V_{IN}=0V$ | | | −0.1 | | $-10^{-5}$ | −0.1 | | −1.0 | μA |
| | | $V_{DD}=15V$, $V_{EE}=0V$<br>$V_{IN}=15V$ | | | 0.1 | | $10^{-5}$ | 0.1 | | 1.0 | μA |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** All voltages measured with respect to $V_{SS}$ unless otherwise specified.

## AC Electrical Characteristics* $T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

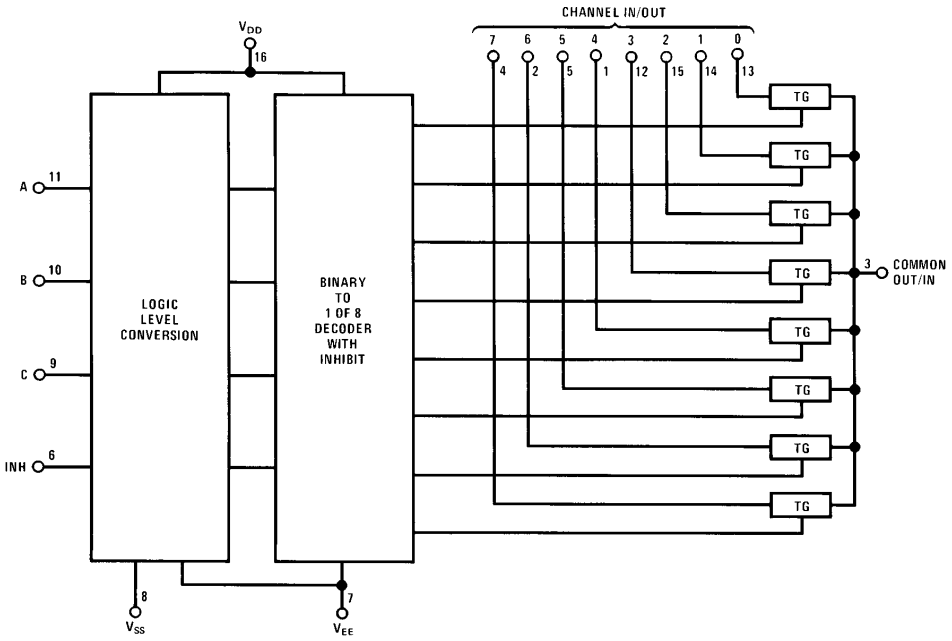
| Symbol | Parameter | Conditions | $V_{DD}$ | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PZH}$, $t_{PZL}$ | Propagation Delay Time from Inhibit to Signal Output (channel turning on) | $V_{EE} = V_{SS} = 0V$<br>$R_L = 1\ k\Omega$<br>$C_L = 50$ pF | 5V<br>10V<br>15V | | 600<br>225<br>160 | 1200<br>450<br>320 | ns<br>ns<br>ns |
| $t_{PHZ}$, $t_{PLZ}$ | Propagation Delay Time from Inhibit to Signal Output (channel turning off) | $V_{EE} = V_{SS} = 0V$<br>$R_L = 1\ k\Omega$<br>$C_L = 50$ pF | 5V<br>10V<br>15V | | 210<br>100<br>75 | 420<br>200<br>150 | ns<br>ns<br>ns |
| $C_{IN}$ | Input Capacitance<br>Control input<br>Signal Input (IN/OUT) | | | | <br>5<br>10 | <br>7.5<br>15 | <br>pF<br>pF |
| $C_{OUT}$ | Output Capacitance (common OUT/IN) | | | | | | |
| | CD4051<br>CD4052<br>CD4053 | $V_{EE} = V_{SS} = 0V$ | 10V<br>10V<br>10V | | 30<br>15<br>8 | | pF<br>pF<br>pF |
| $C_{IOS}$ | Feedthrough Capacitance | | | | 0.2 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance | | | | | | |
| | CD4051<br>CD4052<br>CD4053 | | | | 110<br>140<br>70 | | pF<br>pF<br>pF |
| **Signal Inputs ($V_{IS}$) and Outputs ($V_{OS}$)** | | | | | | | |
| | Sine Wave Response (Distortion) | $R_L = 10\ k\Omega$<br>$f_{IS} = 1$ kHz<br>$V_{IS} = 5\ V_{p-p}$<br>$V_{EE} = V_{SI} = 0V$ | 10V | | 0.04 | | % |
| | Frequency Response, Channel "ON" (Sine Wave Input) | $R_L = 1\ k\Omega$, $V_{EE} = 0V$, $V_{IS} = 5V_{p-p}$,<br>$20 \log_{10} V_{OS}/V_{IS} = -3$ dB | 10V | | 40 | | MHz |
| | Feedthrough, Channel "OFF" | $R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$,<br>$20 \log_{10} V_{OS}/V_{IS} = -40$ dB | 10V | | 10 | | MHz |
| | Crosstalk Between Any Two Channels (frequency at 40 dB) | $R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$<br>$20 \log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3) | 10V | | 3 | | MHz |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay Signal Input to Signal Output | $V_{EE} = V_{SS} = 0V$<br>$C_L = 50$ pF | 5V<br>10V<br>15V | | 25<br>15<br>10 | 55<br>35<br>25 | ns<br>ns<br>ns |
| **Control Inputs, A, B, C and Inhibit** | | | | | | | |
| | Control Input to Signal Crosstalk | $V_{EE} = V_{SS} = 0V$, $R_L = 10\ k\Omega$ at both ends of channel.<br>Input Square Wave Amplitude = 10V | 10V | | 65 | | mV (peak) |
| $t_{PHL}$,<br>$t_{PLH}$ | Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF") | $V_{EE} = V_{SS} = 0V$<br>$C_L = 50$ pF | 5V<br>10V<br>15V | | 500<br>180<br>120 | 1000<br>360<br>240 | ns<br>ns<br>ns |

*AC Parameters are guaranteed by DC correlated testing.

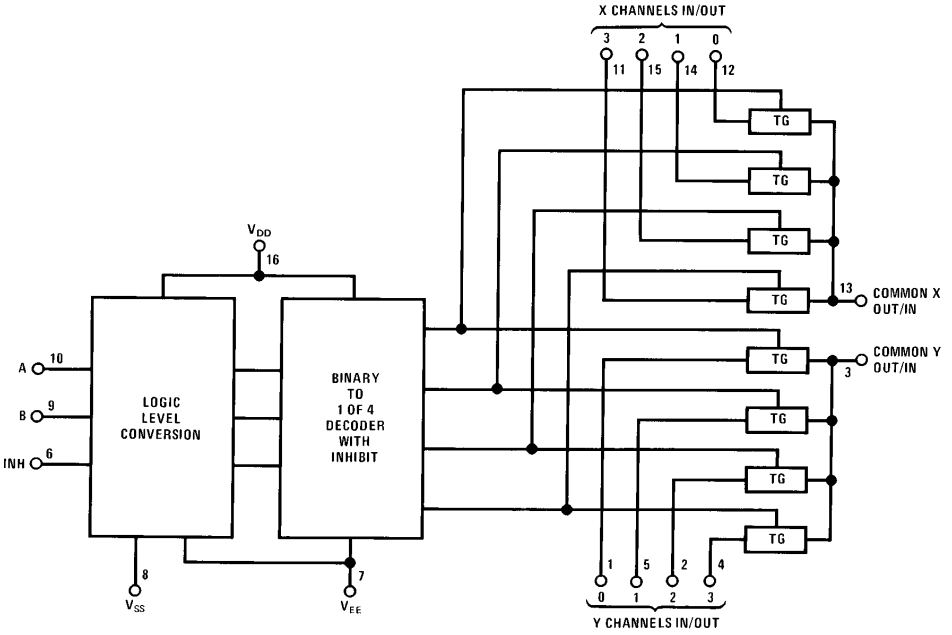
**Note 3:** A, B are two arbitrary channels with A turned "ON" and B "OFF".

## Block Diagrams

**CD4051BM/CD4051BC**




**CD4052BM/CD4052BC**

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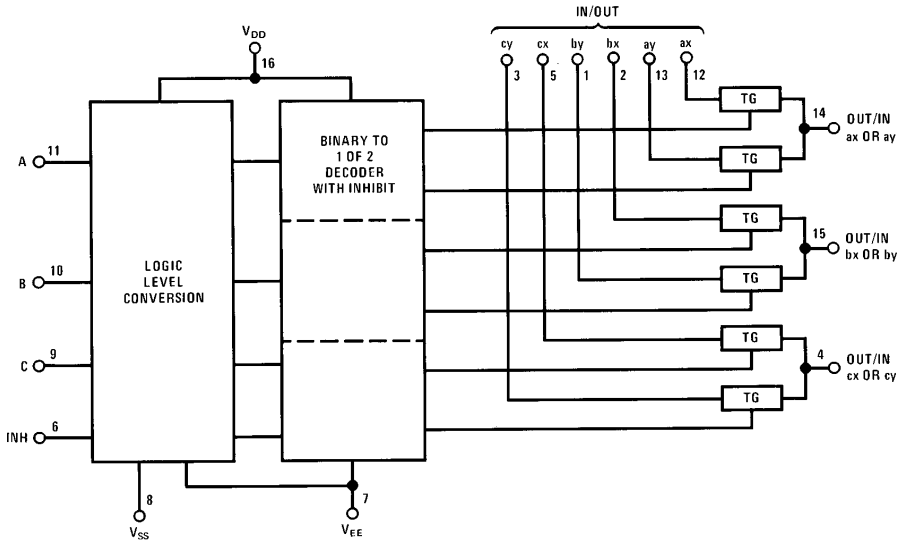
## Block Diagrams (Continued)

**CD4053BM/CD4053BC**

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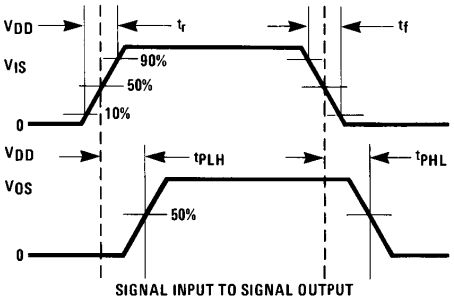
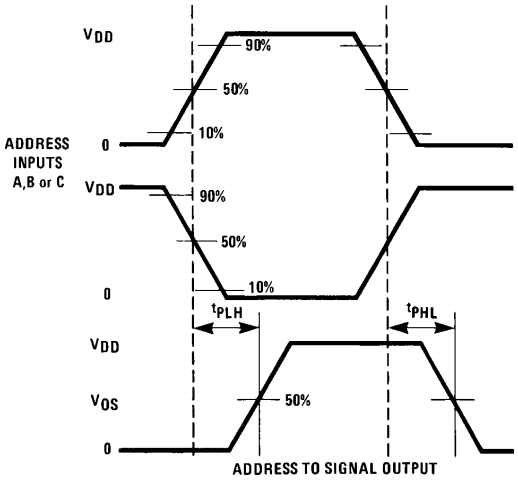
## Truth Table

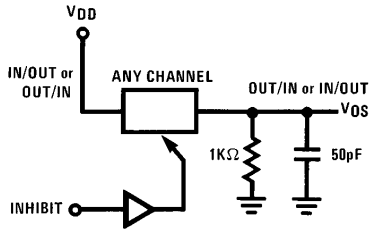
| INPUT STATES | | | | "ON" CHANNELS | | |
|---|---|---|---|---|---|---|
| INHIBIT | C | B | A | CD4051B | CD4052B | CD4053B |
| 0 | 0 | 0 | 0 | 0 | 0X, 0Y | cx, bx, ax |
| 0 | 0 | 0 | 1 | 1 | 1X, 1Y | cx, bx, ay |
| 0 | 0 | 1 | 0 | 2 | 2X, 2Y | cx, by, ax |
| 0 | 0 | 1 | 1 | 3 | 3X, 3Y | cx, by, ay |
| 0 | 1 | 0 | 0 | 4 | | cy, bx, ax |
| 0 | 1 | 0 | 1 | 5 | | cy, bx, ay |
| 0 | 1 | 1 | 0 | 6 | | cy, by, ax |
| 0 | 1 | 1 | 1 | 7 | | cy, by, ay |
| 1 | * | * | * | NONE | NONE | NONE |

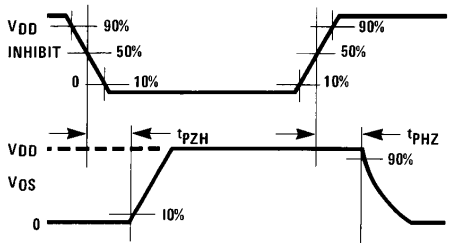
*Don't Care condition.

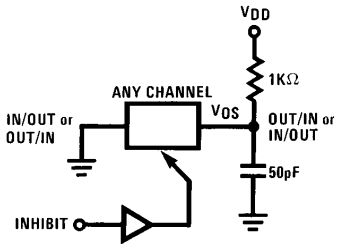
## Switching Time Waveforms

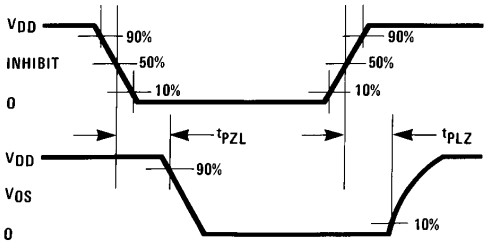
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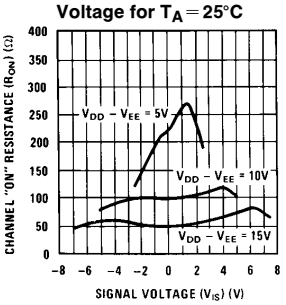
## Special Considerations

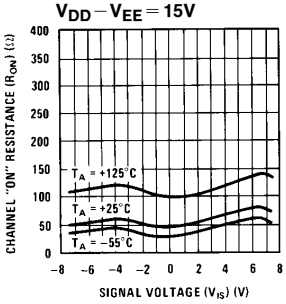
In certain applications the external load-resistor current may include both $V_{DD}$ and signal-line components. To avoid drawing $V_{DD}$ current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from $R_{ON}$ values shown). No $V_{DD}$ current will flow through $R_L$ if the switch current flows into OUT/IN pin.

## Typical Performance Characteristics

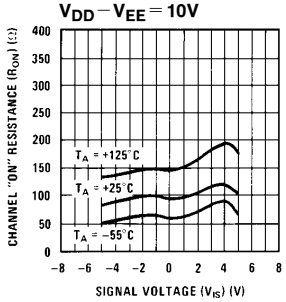
**"ON" Resistance vs Signal Voltage for $T_A = 25°C$**



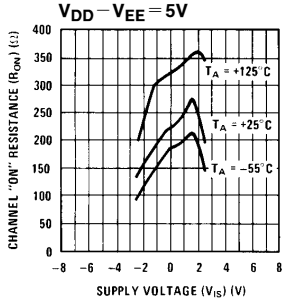

**"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$**




**"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$**

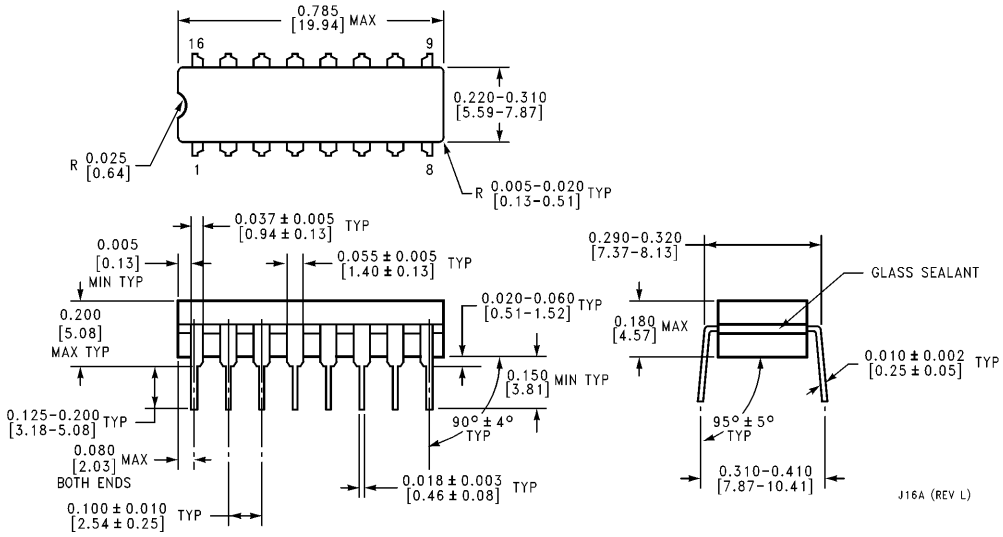



**"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$**

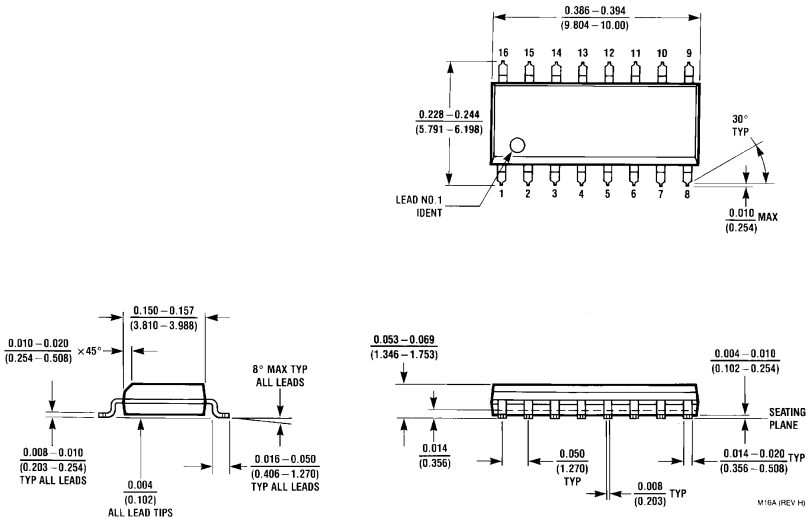



TL/F/5662–5

## Physical Dimensions inches (millimeters)

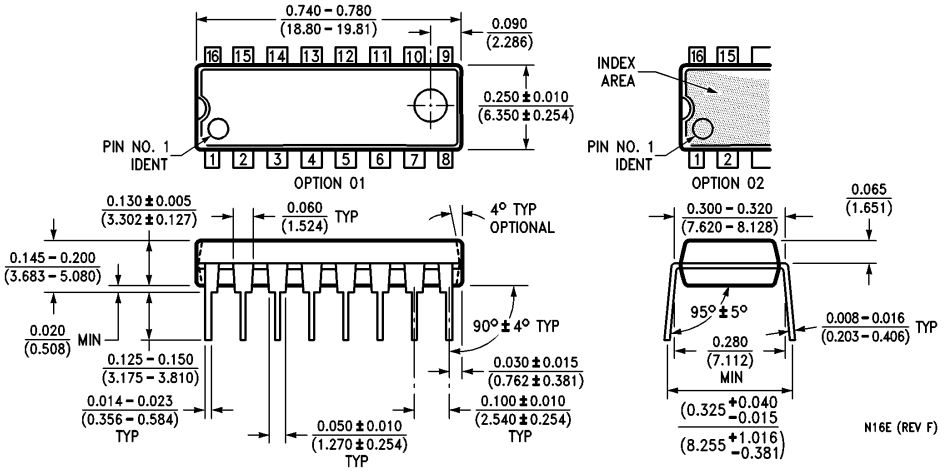



**Cavity Dual-In-Line Package (J)**
**Order Number CD4051BMJ, CD4051BCJ, CD4052BMJ,**
**CD4052BCJ, CD4053BMJ or CD4053BCJ**
**NS Package Number J16A**




**Small Outline Package (M)**
**Order Number CD4051BCM,**
**CD4052BCM or CD4053BCM**
**NS Package Number M16A**

## Physical Dimensions inches (millimeters) (Continued)




**Molded Dual-In-Line Package (N)**
**Order CD4051BM, CD4051BC,**
**CD4052BM, CD4052BC, CD4053BM, CD4053BC**
**NS Package Number N16E**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**National Semiconductor Corporation**
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

**National Semiconductor Europe**
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**
Tel: 81-043-299-2309
Fax: 81-043-299-2408