PCB   24
CATALYST

CAT93C46/56/57/66/86

1K/2K/2K/4K/16K-Bit Microwire Serial E²PROM

FEATURES

- **High Speed Operation:**
  - **– 93C46/56/57/66: 1MHz**
  - **– 93C86: 3MHz**
- **Low Power CMOS Technology**
- **1.8 to 6.0 Volt Operation**
- **Selectable x8 or x16 Memory Organization**
- **Self-Timed Write Cycle with Auto-Clear**
- **Hardware and Software Write Protection**

- **Power-Up Inadvertent Write Protection**
- **1,000,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Commercial, Industrial and Automotive Temperature Ranges**
- **Sequential Read (except 93C46)**
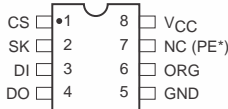- **Program Enable (PE) Pin (93C86 only)**

DESCRIPTION

The CAT93C46/56/57/66/86 are 1K/2K/2K/4K/16K-bit Serial E²PROM memory devices which are configured as either registers of 16 bits (ORG pin at V_{CC}) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46/56/57/66/86 are manufactured using Catalyst's advanced
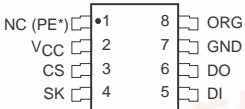
CMOS E²PROM floating gate technology. The devices are designed to endure 1,000,000 program/erase cycles and have a data retention of 100 years. The devices are available in 8-pin DIP, 8-pin SOIC or 8-pin TSSOP packages.
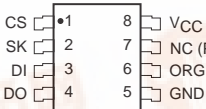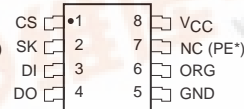
PIN CONFIGURATION

DIP Package (P)

CS 1	8 V_{CC}
SK 2	7 NC (PE*)
DI 3	6 ORG
DO 4	5 GND

SOIC Package (J)

NC (PE*) 1	8 ORG
V_{CC} 2	7 GND
CS 3	6 DO
SK 4	5 DI

SOIC Package (S)

CS 1	8 V_{CC}
SK 2	7 NC (PE*)
DI 3	6 ORG
DO 4	5 GND

SOIC Package (K)

CS 1	8 V_{CC}
SK 2	7 NC (PE*)
DI 3	6 ORG
DO 4	5 GND

TSSOP Package (U)

CS 1	8 V_{CC}
SK 2	7 NC (PE*)
DI 3	6 ORG
DO 4	5 GND

*Only For 93C86

93C46/56/57/66/86
F01

PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+1.8 to 6.0V Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection
PE*	Program Enable

Note: When the ORG pin is connected to VCC, the X16 organization is selected. When it is connected to ground, the X8 pin is selected. If the ORG pin is left unconnected, then an internal pullup device will select the X16 organization.

BLOCK DIAGRAM
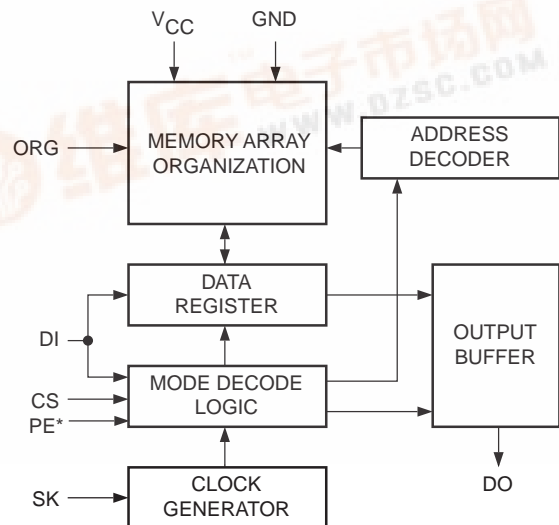
93C46/56/57/66/86 F02

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... –55°C to +125°C

Storage Temperature .... –65°C to +150°C

Voltage on any Pin with
Respect to Ground[1] .... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground .... –2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) .... 300°C

Output Short Circuit Current[2] .... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}[3]	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}[3]	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}[3]	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}[3][4]	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating Write)			3	mA	f_{SK} = 1MHz V_{CC} = 5.0V
I_{CC2}	Power Supply Current (Operating Read)			500	µA	f_{SK} = 1MHz V_{CC} = 5.0V
I_{SB1}	Power Supply Current (Standby) (x8 Mode)			10	µA	CS = 0V ORG=GND
I_{SB2}[5]	Power Supply Current (Standby) (x16Mode)			0	µA	CS=0V ORG=Float or V_{CC}
I_{LI}	Input Leakage Current			1	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current (Including ORG pin)			1	µA	V_{OUT} = 0V to V_{CC}, CS = 0V
V_{IL1}	Input Low Voltage	-0.1		0.8	V	4.5V≤V_{CC}<5.5V
V_{IH1}	Input High Voltage	2		V_{CC}+1	V	
V_{IL2}	Input Low Voltage	0		V_{CC}X0.2	V	1.8V≤V_{CC}<2.7V
V_{IH2}	Input High Voltage	V_{CC}X0.7		V_{CC}+1	V	
V_{OL1}	Output Low Voltage			0.4	V	4.5V≤V_{CC}<5.5V
V_{OH1}	Output High Voltage	2.4			V	I_{OL} = 2.1mA I_{OH} = -400µA
V_{OL2}	Output Low Voltage			0.2		1.8V≤V_{CC}<2.7V
V_{OH2}	Output High Voltage	V_{CC}-0.2			V	I_{OL} = 1mA I_{OH} = -100µA

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SB2})=0µA (<900nA) for 93C46/56/57/66, (I_{SB2})=2µA for 93C86.

PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C_{OUT}[3]	OUTPUT CAPACITANCE (DO)	5	pF	V_{OUT}=OV
C_{IN}[3]	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V_{IN}=OV

INSTRUCTION SET

Instruction	Device Type	Start Bit	Opcode	Address x8	Address x16	Data x8	Data x16	Comments	PE[2]
READ	93C46	1	10	A6-A0	A5-A0			Read Address AN–A0	
	93C56[1]	1	10	A8-A0	A7-A0				
	93C66	1	10	A8-A0	A7-A0				
	93C57	1	10	A7-A0	A6-A0				
	93C86	1	10	A10-A0	A9-A0				X
ERASE	93C46	1	11	A6-A0	A5-A0			Clear Address AN–A0	
	93C56[1]	1	11	A8-A0	A7-A0				
	93C66	1	11	A8-A0	A7-A0				
	93C57	1	11	A7-A0	A6-A0				
	93C86	1	11	A10-A0	A9-A0				I
WRITE	93C46	1	01	A6-A0	A5-A0	D7-D0	D15-D0	Write Address AN–A0	
	93C56[1]	1	01	A8-A0	A7-A0	D7-D0	D15-D0		
	93C66	1	01	A8-A0	A7-A0	D7-D0	D15-D0		
	93C57	1	01	A7-A0	A6-A0	D7-D0	D15-D0		
	93C86	1	01	A10-A0	A9-A0	D7-D0	D15-D0		I
EWEN	93C46	1	00	11XXXXX	11XXXX			Write Enable	
	93C56	1	00	11XXXXXXX	11XXXXXX				
	93C66	1	00	11XXXXXXX	11XXXXXX				
	93C57	1	00	11XXXXXX	11XXXXX				
	93C86	1	00	11XXXXXXXXX	11XXXXXXXX				X
EWDS	93C46	1	00	00XXXXX	00XXXX			Write Disable	
	93C56	1	00	00XXXXXXX	00XXXXXX				
	93C66	1	00	00XXXXXXX	00XXXXXX				
	93C57	1	00	00XXXXXX	00XXXXX				
	93C86	1	00	00XXXXXXXXX	00XXXXXXXX				X
ERAL	93C46	1	00	10XXXXX	10XXXX			Clear All Addresses	
	93C56	1	00	10XXXXXXX	10XXXXXX				
	93C66	1	00	10XXXXXXX	10XXXXXX				
	93C57	1	00	10XXXXXX	10XXXXX				
	93C86	1	00	10XXXXXXXXX	10XXXXXXXX				I
WRAL	93C46	1	00	01XXXXX	01XXXX	D7-D0	D15-D0	Write All Addresses	
	93C56	1	00	01XXXXXXX	01XXXXXX	D7-D0	D15-D0		
	93C66	1	00	01XXXXXXX	01XXXXXX	D7-D0	D15-D0		
	93C57	1	00	01XXXXXX	01XXXXX	D7-D0	D15-D0		
	93C86	1	00	01XXXXXXXXX	01XXXXXXXX	D7-D0	D15-D0		I

Note:
(1) Address bit A8 for 256x8 ORG and A7 for 128x16 ORG are "Don't Care" bits, but must be kept at either a "1" or "0" for READ, WRITE and ERASE commands.
(2) Applicable only to 93C86
(3) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS (93C46/56/57/66)

SYMBOL	PARAMETER	Limits						UNITS	Test Conditions
		V_{CC} = 1.8V-6V*		V_{CC} = 2.5V-6V		V_{CC} = 4.5V-5.5V			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CSS}	CS Setup Time	200		100		50		ns	C_L = 100pF
t_{CSH}	CS Hold Time	0		0		0		ns	
t_{DIS}	DI Setup Time	400		200		100		ns	
t_{DIH}	DI Hold Time	400		200		100		ns	
t_{PD1}	Output Delay to 1		1		0.5		0.25	µs	
t_{PD0}	Output Delay to 0		1		0.5		0.25	µs	
t_{HZ}[1]	Output Delay to High-Z		400		200		100	ns	
t_{EW}	Program/Erase Pulse Width		10		10		10	ms	
t_{CSMIN}	Minimum CS Low Time	1		0.5		0.25		µs	
t_{SKHI}	Minimum SK High Time	1		0.5		0.25		µs	
t_{SKLOW}	Minimum SK Low Time	1		0.5		0.25		µs	
t_{SV}	Output Delay to Status Valid		1		0.5		0.25	µs	
SK_{MAX}	Maximum Clock Frequency	DC	250	DC	500	DC	1000	KHZ	

* Preliminary data for 93C56/57/66

A.C. CHARACTERISTICS (93C86)

SYMBOL	PARAMETER	Limits						UNITS	Test Conditions
		V_{CC} = 1.8V-6V*		V_{CC} = 2.5V-6V		V_{CC} = 4.5V-5.5V			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CSS}	CS Setup Time	200		150		50		ns	C_L = 100pF
t_{CSH}	CS Hold Time	0		0		0		ns	
t_{DIS}	DI Setup Time	400		250		50		ns	
t_{DIH}	DI Hold Time	400		250		50		ns	
t_{PD1}	Output Delay to 1		1		0.5		0.1	µs	
t_{PD0}	Output Delay to 0		1		0.5		0.1	µs	
t_{HZ}[1]	Output Delay to High-Z		400		200		100	ns	
t_{EW}	Program/Erase Pulse Width		5		5		5	ms	
t_{CSMIN}	Minimum CS Low Time	1		0.5		0.1		µs	
t_{SKHI}	Minimum SK High Time	1		0.5		0.1		µs	
t_{SKLOW}	Minimum SK Low Time	1		0.5		0.1		µs	
t_{SV}	Output Delay to Status Valid		1		0.5		0.1	µs	
SK_{MAX}	Maximum Clock Frequency	DC	250	DC	1000	DC	3000	KHZ	

NOTE:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

DEVICE OPERATION

The CAT93C46/56(57)66/86 is a 1024/2048/4096/16,384-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46/56/57/66/86 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 9-bit instructions for 93C46; seven 10-bit instructions for 93C57; seven 11-bit instructions for 93C56 and 93C66; seven 13-bit instructions for 93C86; control the reading, writing and erase operations of the device. When organized as X8, seven 10-bit instructions for 93C46; seven 11-bit instructions for 93C57; seven 12-bit instructions for 93C56 and 93C66: seven 14-bit instructions for 93C86; control the reading, writing and erase operations of the device. The CAT93C46/56/57/66/86 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

Figure 1. Sychronous Data Timing
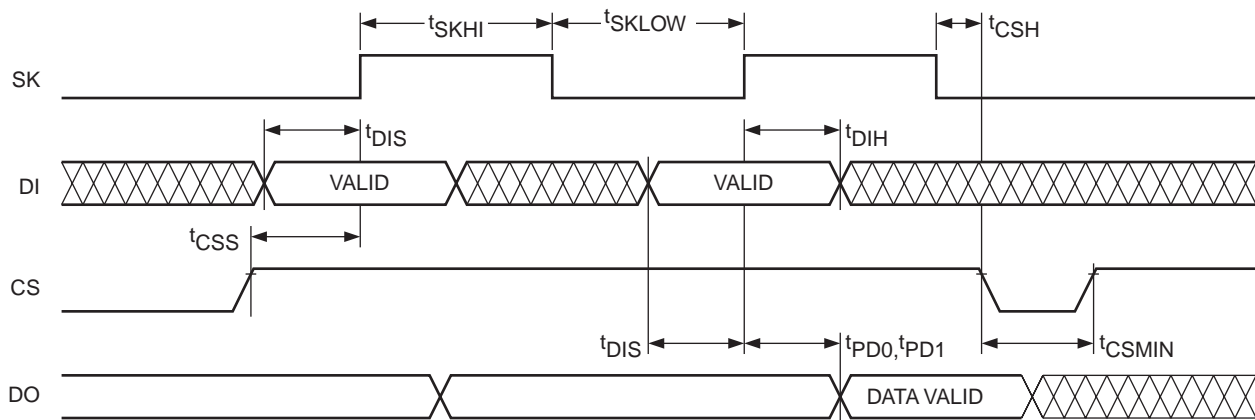
93C46/56/57/66/86 F03

Figure 2a. Read Instruction Timing (93C46)
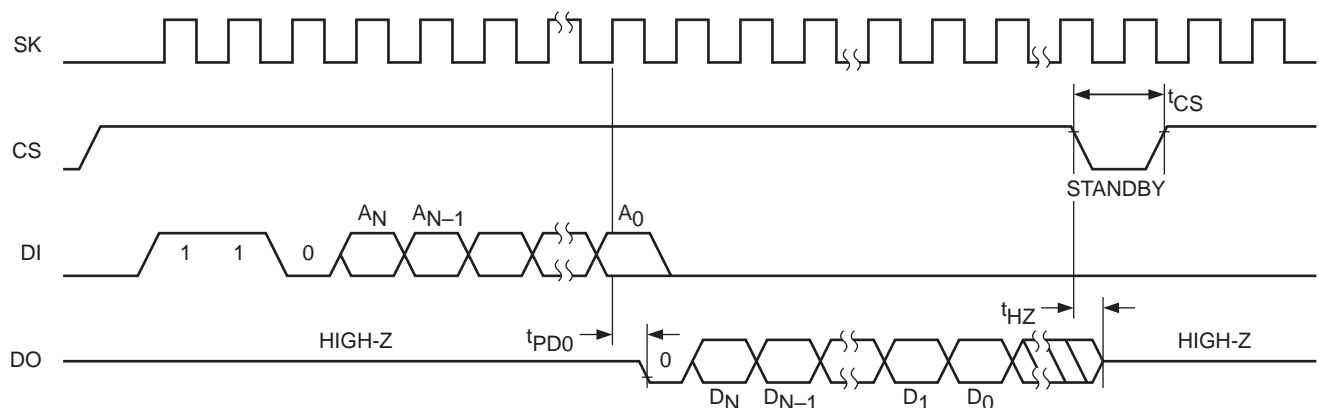
93C46/56/57/66/86 F04

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 6-bit (93C46)/ /7-bit (93C57)/ 8-bit (93C56 or 93C66)/10-bit (93C86) (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations).

Note: This note is applicable only to 93C86. The Write, Erase, Write all and Erase all instructions require PE=1. If PE is left floating, 93C86 is in Program Enabled mode. For Write Enable and Write Disable instruction PE=don't care.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46/ 56/57/66/86 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1})

For the 93C56/57/66/86, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/56/57/66/86 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

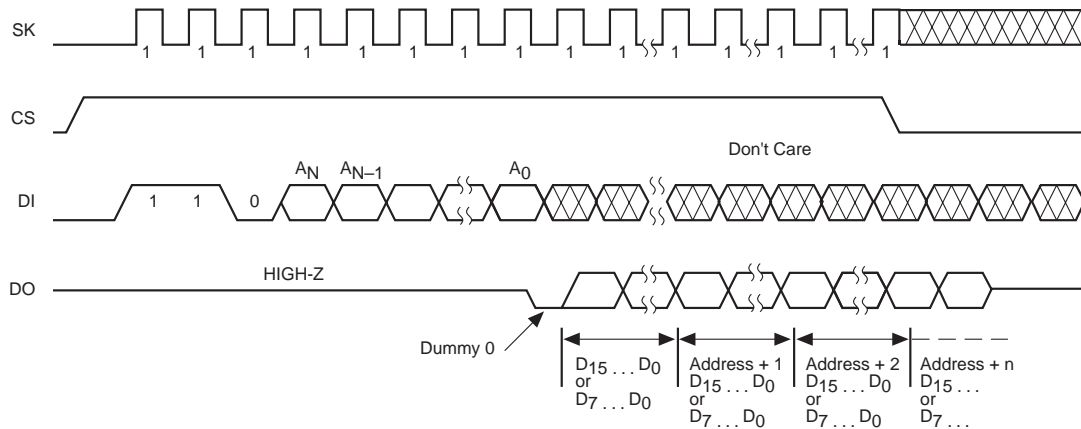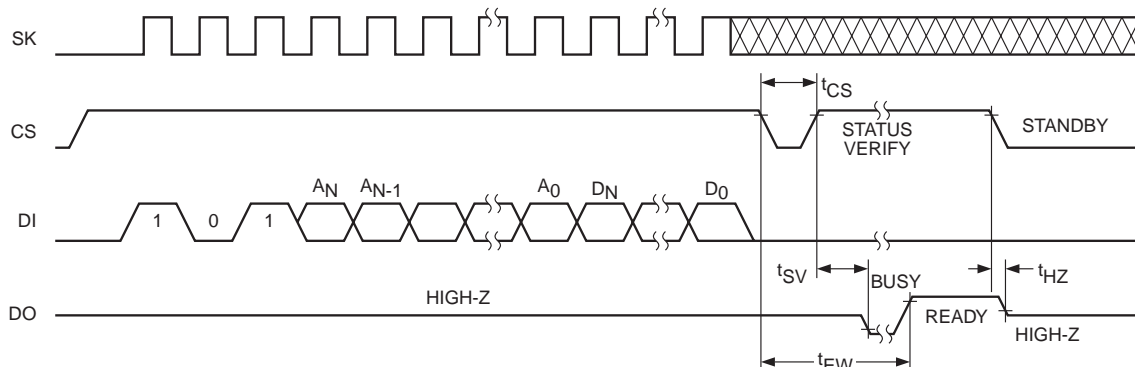**Figure 2b. Read Instruction Timing (93C56/57/66/86)**

Figure 3. Write Instruction Timing

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/56/57/66/86 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT93C46/56/57/66/86 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46/56/57/66/86 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/56/57/66/86 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46/56/57/66/86 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.
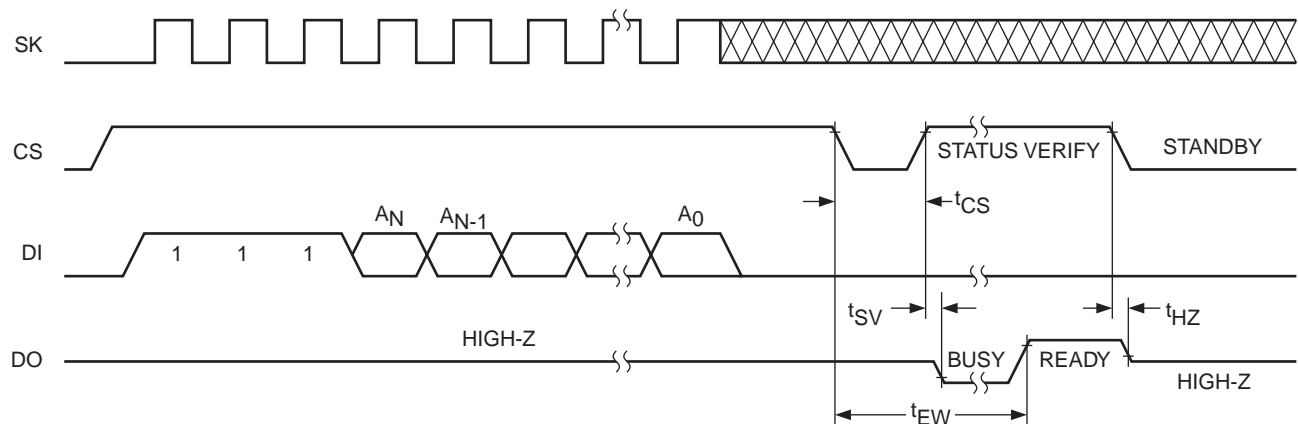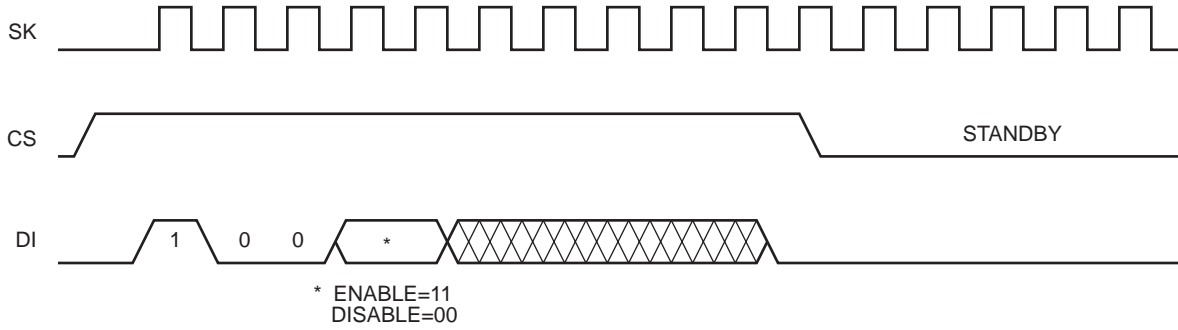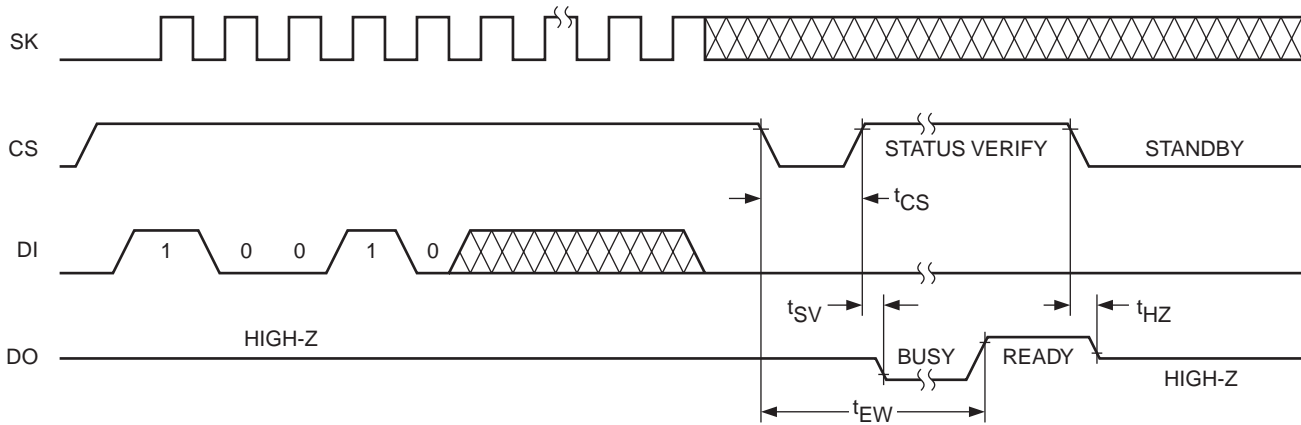
Figure 4. Erase Instruction Timing

93C46/56/57/66/86 F06

Figure 5. EWEN/EWDS Instruction Timing

SK

CS   STANDBY

DI   1   0   0   *

              * ENABLE=11
                DISABLE=00

Figure 6. ERAL Instruction Timing

SK

CS   STATUS VERIFY   STANDBY

                                                                t_{CS}

DI   1   0   0   1   0

                                        t_{SV} t_{HZ}

DO   HIGH-Z   BUSY   READY
                                                                        HIGH-Z

                                            t_{EW}

Figure 7. WRAL Instruction Timing

SK

CS   STATUS VERIFY   STANDBY

                                                                t_{CS}

DI   1   0   0   0   1 D_N D_0

                                                t_{SV} t_{HZ}

DO   BUSY   READY
                                                                        HIGH-Z

                                                    t_{EW}

ORDERING INFORMATION

Prefix	Device #		Suffix

CAT   93C46   S   I   -1.8   TE13

Optional Company ID

Product Number
93C46: 1K
93C56: 2K
93C57: 2K
93C66: 4K
93C86: 16K

Package
P = PDIP
S = SOIC (JEDEC)
J = SOIC (JEDEC)
K = SOIC (EIAJ)
U = TSSOP

Temperature Range
Blank = Commercial (0˚ - 70˚C)
I = Industrial (-40˚ - 85˚C)
A = Automotive (-40˚ - 105˚C)*

Operating Voltage
Blank (V_{cc}=2.5 to 6.0V)
1.8 (V_{cc}=1.8 to 6.0V)
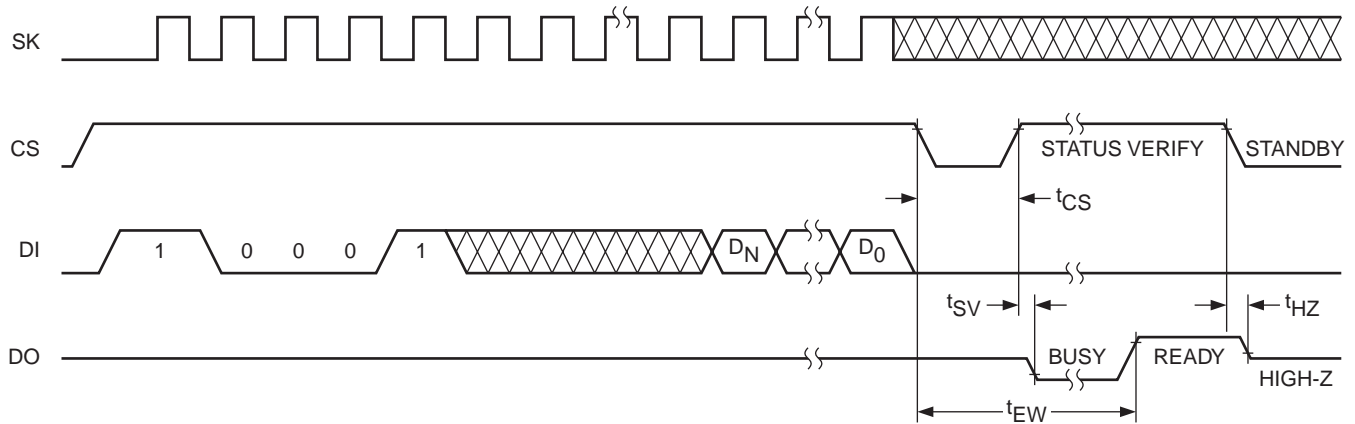
Tape & Reel
TE13: 2000/Reel
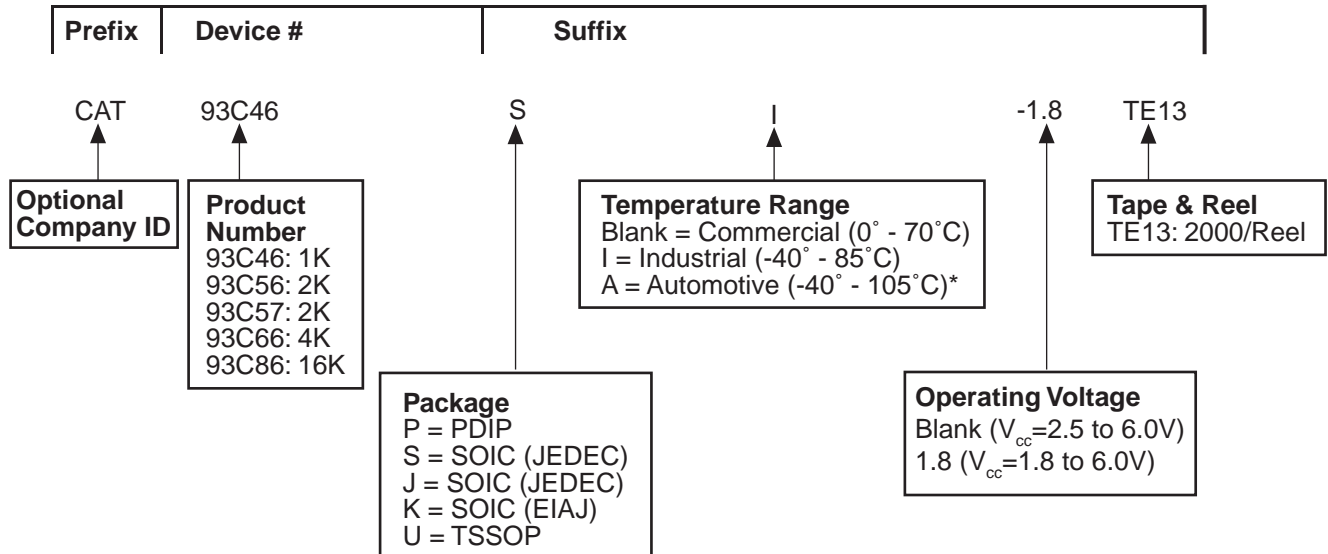
* -40˚ to +125˚C is available upon request

93C46/56/57/66/86 F10

Notes:
(1) The device used in the above example is a 93C46SI-1.8TE13 (SOIC, Industrial Temperature, 1.8 Volt to 6 Volt Operating Voltage, Tape & Reel)