LTC2053

Precision, Rail-to-Rail Input and Output, Zero-Drift Instrumentation Amplifier with Resistor-Programmable Gain

FEATURES

- **116dB CMRR Independent of Gain**
- **Maximum Offset Voltage: 10μV**
- **Maximum Offset Voltage Drift: 50nV/°C**
- **Rail-to-Rail Input**
- **Rail-to-Rail Output**
- **2-Resistor Programmable Gain**
- Supply Operation: 2.7V to ±5.5V
- Typical Noise: 2.5μV_{P-P} (0.01Hz to 10Hz)
- Typical Supply Current: 750μA
- Available in an MS8 and 3mm × 3mm × 0.8mm DFN Packages

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

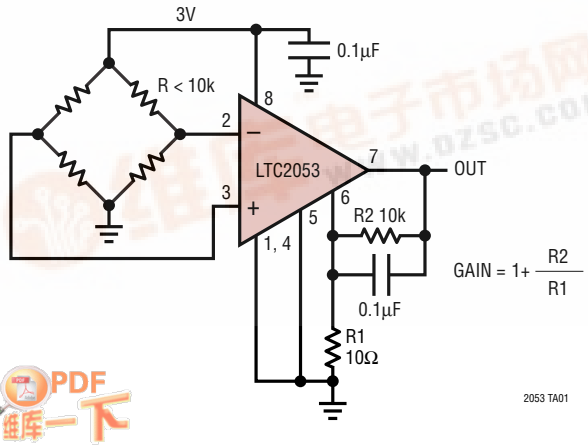
The LTC®2053 is a high precision instrumentation amplifier. The CMRR is typically 116dB with a single or dual 5V supply and is independent of gain. The input offset voltage is guaranteed below 10μV with a temperature drift of less than 50nV/°C. The LTC2053 is easy to use; the gain is adjustable with two external resistors, like a traditional op amp.

The LTC2053 uses charge balanced sampled data techniques to convert a differential input voltage into a single ended signal that is in turn amplified by a zero-drift operational amplifier.

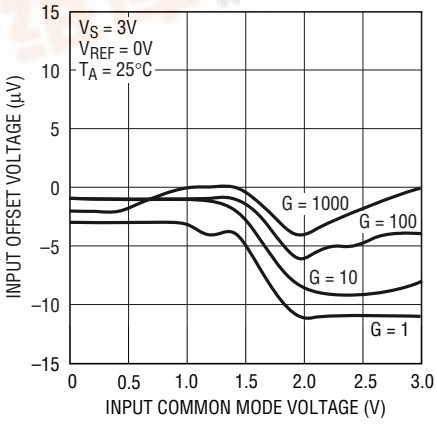
The differential inputs operate from rail-to-rail and the single ended output swings from rail-to-rail. The LTC2053 can be used in single supply applications, as low as 2.7V. It can also be used with dual ±5.5V supplies. The LTC2053 is available in an MS8 surface mount package. For space limited applications, the LTC2053 is available in a 3mm × 3mm × 0.8mm dual fine pitch leadless package (DFN).

TYPICAL APPLICATION

Differential Bridge Amplifier



Typical Input Referred Offset vs Input Common Mode Voltage (V_S = 3V)



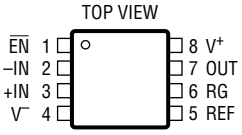
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 11V
Input Current ..... ±10mA
$|V_{IN}^+ - V_{REF}|$ 5.5V
$|V_{IN}^- - V_{REF}|$ 5.5V
Output Short Circuit Duration ..... Indefinite

Operating Temperature Range
LTC2053C ..... 0°C to 70°C
LTC2053I ..... –40°C to 85°C
LTC2053H ..... –40°C to 125°C
Storage Temperature Range
MS8 Package ..... –65°C to 150°C
DD Package ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

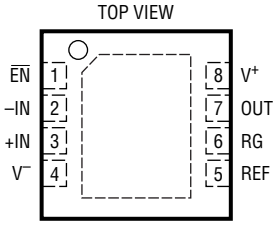
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LTC2053CMS8 LTC2053IMS8 LTC2053HMS8
MS8 PART MARKING
LTVT LTJY LTAFB



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 160°C/W
UNDERSIDE METAL INTERNALLY CONNECTED TO V^-
(PCB CONNECTION OPTIONAL)

ORDER PART NUMBER*
LTC2053CDD LTC2053IDD LTC2053HDD
DD PART MARKING
LAEQ

*The temperature grade (C, I, or H) of the LTC2053 in the DFN package is indicated on the shipping container.
Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, REF = 200mV. Output voltage swing is referenced to V^-. All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	A_V = 1	●		0.001	0.01	%
Gain Nonlinearity	A_V = 1	●		3	12	ppm
Input Offset Voltage (Note 2)	V_{CM} = 200mV			–5	±10	µV
Average Input Offset Drift (Note 2)	T_A = –40°C to 85°C T_A = 85°C to 125°C	● ●			±50 –1	nV/°C µV/°C
Average Input Bias Current (Note 3)	V_{CM} = 1.2V	●		4	10	nA
Average Input Offset Current (Note 3)	V_{CM} = 1.2V	●		1	3	nA
Input Noise Voltage	DC to 10Hz			2.5		μV_{P-P}
Common Mode Rejection Ratio (Notes 4, 5)	A_V = 1, V_{CM} = 0V to 3V, LTC2053C A_V = 1, V_{CM} = 0.1V to 2.9V, LTC2053I A_V = 1, V_{CM} = 0V to 3V, LTC2053I A_V = 1, V_{CM} = 0.1V to 2.9V, LTC2053H A_V = 1, V_{CM} = 0V to 3V, LTC2053H	● ● ● ● ●	105 105 95 100 90	113 113 113		dB dB dB dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, REF = 200mV. Output voltage swing is referenced to V^-. All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Rejection Ratio (Note 6)	V_S = 2.7V to 6V	●	110	116		dB
Output Voltage Swing High	R_L = 2k to V^- R_L = 10k to V^-	● ●	2.85 2.95	2.94 2.98		V V
Output Voltage Swing Low		●			20	mV
Supply Current	$V_{\overline{EN}} \leq$ 0.5V, No Load	●		0.75	1	mA
Supply Current, Shutdown	$V_{\overline{EN}} \geq$ 2.5V				10	µA
$\overline{EN}$ Pin Input Low Voltage, V_{IL}					0.5	V
$\overline{EN}$ Pin Input High Voltage, V_{IH}			2.5			V
$\overline{EN}$ Pin Input Current	$V_{\overline{EN}} = V^-$			–0.5	–10	µA
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		V/µs
Internal Sampling Frequency				3		kHz

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, REF = 200mV. Output voltage swing is referenced to V^-. All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	A_V = 1	●		0.001	0.01	%
Gain Nonlinearity	A_V = 1	●		3	10	ppm
Input Offset Voltage (Note 2)	V_{CM} = 200mV			–5	±10	µV
Average Input Offset Drift (Note 2)	T_A = –40°C to 85°C T_A = 85°C to 125°C	● ●			±50 –2.5	nV/°C µV/°C
Average Input Bias Current (Note 3)	V_{CM} = 1.2V	●		4	10	nA
Average Input Offset Current (Note 3)	V_{CM} = 1.2V	●		1	3	nA
Common Mode Rejection Ratio (Notes 4, 5)	A_V = 1, V_{CM} = 0V to 5V, LTC2053C A_V = 1, V_{CM} = 0.1V to 4.9V, LTC2053I A_V = 1, V_{CM} = 0V to 5V, LTC2053I A_V = 1, V_{CM} = 0.1V to 4.9V, LTC2053H A_V = 1, V_{CM} = 0V to 5V, LTC2053H	● ● ● ● ●	105 105 95 100 90	116 116 116		dB dB dB dB dB
Power Supply Rejection Ratio (Note 6)	V_S = 2.7V to 6V	●	110	116		dB
Output Voltage Swing High	R_L = 2k to V^- R_L = 10k to V^-	● ●	4.85 4.95	4.94 4.98		V V
Output Voltage Swing Low		●			20	mV
Supply Current	$V_{\overline{EN}} \leq$ 0.5V, No Load	●		0.85	1.1	mA
Supply Current, Shutdown	$V_{\overline{EN}} \geq$ 4.5V				10	µA
$\overline{EN}$ Pin Input Low Voltage, V_{IL}					0.5	V
$\overline{EN}$ Pin Input High Voltage, V_{IH}			4.5			V
$\overline{EN}$ Pin Input Current	$V_{\overline{EN}} = V^-$			–1	–10	µA
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		V/µs
Internal Sampling Frequency				3		kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = –5V, REF = 0V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	A_V = 1	●		0.001	0.01	%
Gain Nonlinearity	A_V = 1	●		3	10	ppm
Input Offset Voltage (Note 2)	V_{CM} = 0V			10	±20	µV
Average Input Offset Drift (Note 2)	T_A = –40°C to 85°C T_A = 85°C to 125°C	● ●		 –1	±50 –2.5	nV/°C µV/°C
Average Input Bias Current (Note 3)	V_{CM} = 1V	●		4	10	nA
Average Input Offset Current (Note 3)	V_{CM} = 1V	●		1	3	nA
Common Mode Rejection Ratio (Notes 4, 5)	A_V = 1, V_{CM} = –5V to 5V, LTC2053C A_V = 1, V_{CM} = –4.9V to 4.9V, LTC2053I A_V = 1, V_{CM} = –5V to 5V, LTC2053I A_V = 1, V_{CM} = –4.9V to 4.9V, LTC2053H A_V = 1, V_{CM} = –5V to 5V, LTC2053H	● ● ● ● ●	105 105 95 100 90	118 118 118		dB dB dB dB dB
Power Supply Rejection Ratio (Note 6)	V_S = 2.7V to 11V	●	110	116		dB
Maximum Output Voltage Swing	R_L = 2k to GND, LTC2053C, LTC2053I R_L = 10k to GND, LTC2053C, LTC2053I, LTC2053H R_L = 2k to GND, LTC2053H	● ● ●	±4.5 ±4.6 ±4.4	±4.8 ±4.9 ±4.8		V V V
Supply Current	$V_{\overline{EN}} \leq$ –4.5V, No Load	●		0.95	1.3	mA
Supply Current, Shutdown	$V_{\overline{EN}} \geq$ 4.5V				20	µA
$\overline{EN}$ Pin Input Low Voltage, V_{IL}					–4.5	V
$\overline{EN}$ Pin Input High Voltage, V_{IH}			4.5			V
$\overline{EN}$ Pin Input Current	$V_{\overline{EN}} = V^-$			–3	–20	µA
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		V/µs
Internal Sampling Frequency				3		kHz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

Note 3: If the total source resistance is less than 10k, no DC errors result from the input bias currents or the mismatch of the input bias currents or the mismatch of the resistances connected to –IN and +IN.

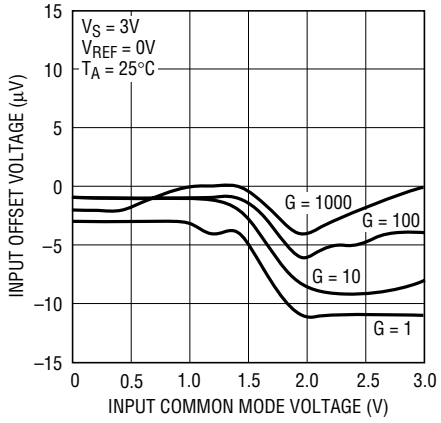
Note 4: The CMRR with a voltage gain, A_V, larger than 10 is 120dB (typ).

Note 5: At temperatures above 70°C, the common mode rejection ratio lowers when the common mode input voltage is within 100mV of the supply rails.

Note 6: The power supply rejection ratio (PSRR) measurement accuracy depends on the proximity of the power supply bypass capacitor to the device under test. Because of this, the PSRR is 100% tested to relaxed limits at final test. However, their values are guaranteed by design to meet the data sheet limits.

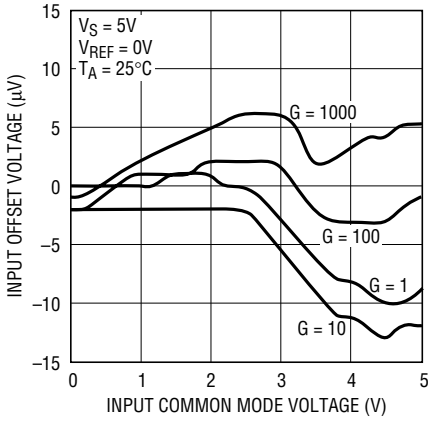
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage vs Input Common Mode Voltage



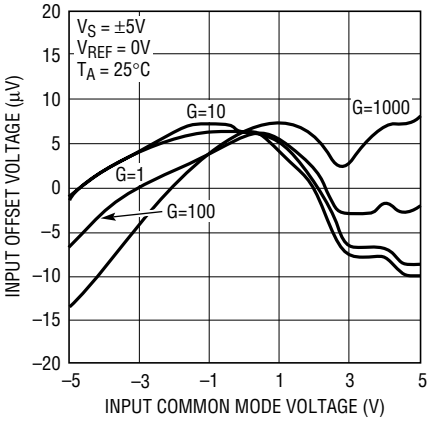
2053 G01

Input Offset Voltage vs Input Common Mode Voltage



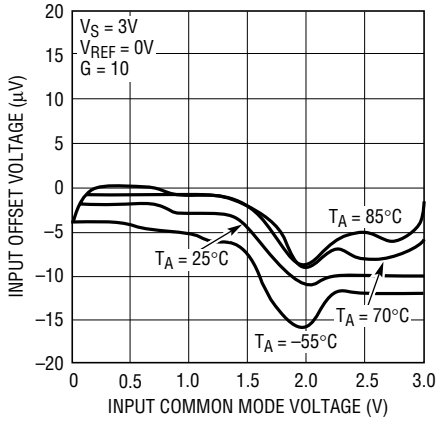
2053 G02

Input Offset Voltage vs Input Common Mode Voltage



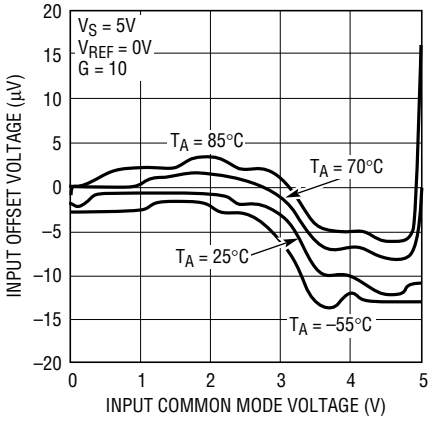
2053 G03

Input Offset Voltage vs Input Common Mode Voltage



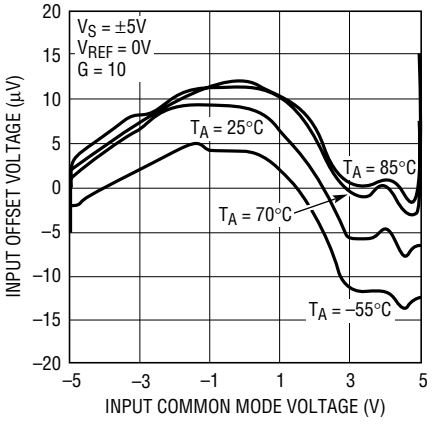
2053 G04

Input Offset Voltage vs Input Common Mode Voltage



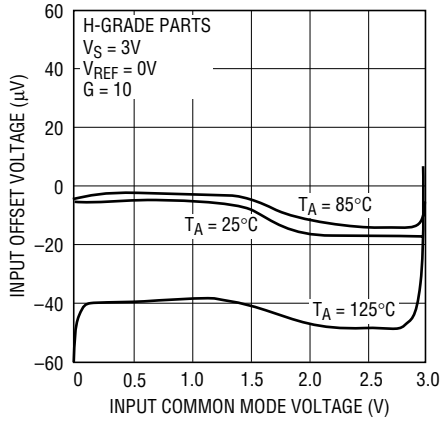
2053 G05

Input Offset Voltage vs Input Common Mode Voltage



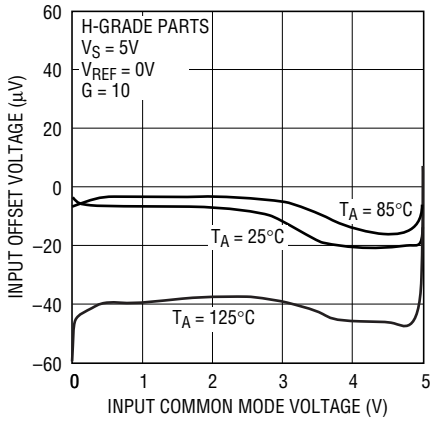
2053 G06

Input Offset Voltage vs Input Common Mode Voltage



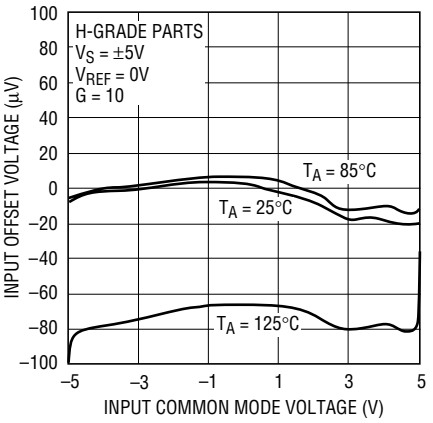
2053 G07

Input Offset Voltage vs Input Common Mode Voltage



2053 G08

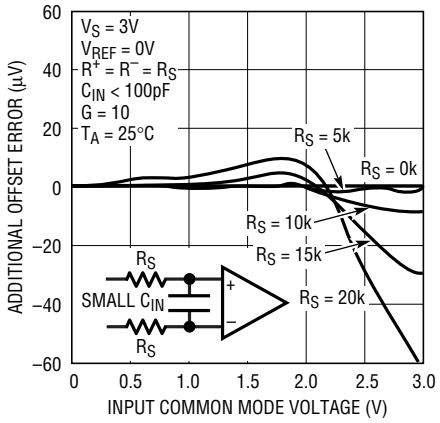
Input Offset Voltage vs Input Common Mode Voltage



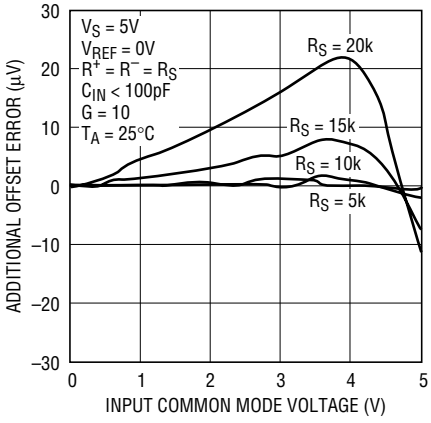
2053 G09

TYPICAL PERFORMANCE CHARACTERISTICS

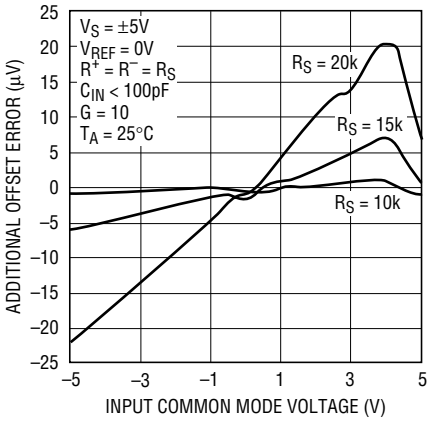
Error Due to Input R_S vs Input Common Mode (C_{IN} < 100pF)



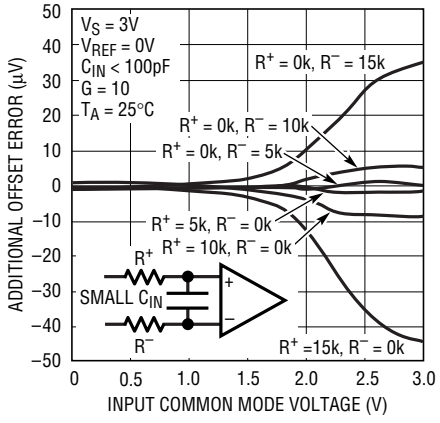
Error Due to Input R_S vs Input Common Mode (C_{IN} < 100pF)



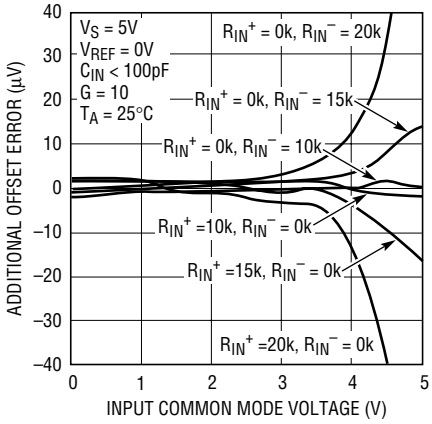
Error Due to Input R_S vs Input Common Mode (C_{IN} < 100pF)



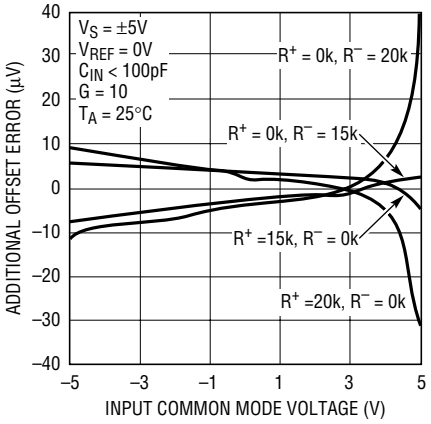
Error Due to Input R_S Mismatch vs Input Common Mode (C_{IN} < 100pF)



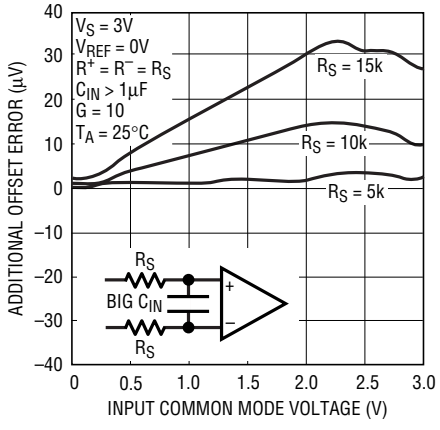
Error Due to Input R_S Mismatch vs Input Common Mode (C_{IN} < 100pF)



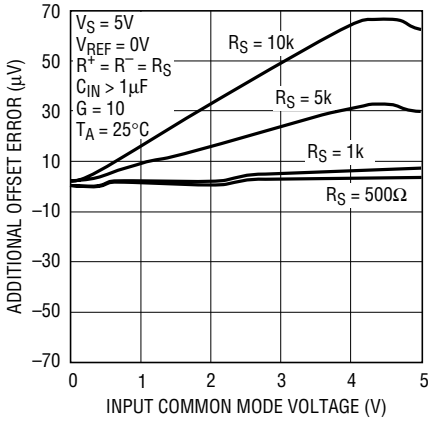
Error Due to Input R_S Mismatch vs Input Common Mode (C_{IN} < 100pF)



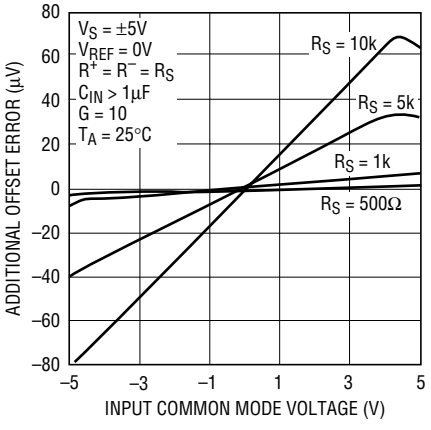
Error Due to Input R_S vs Input Common Mode (C_{IN} > 1µF)



Error Due to Input R_S vs Input Common Mode (C_{IN} > 1µF)

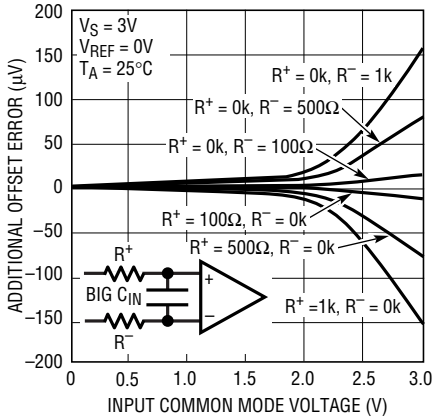


Error Due to Input R_S vs Input Common Mode (C_{IN} > 1µF)

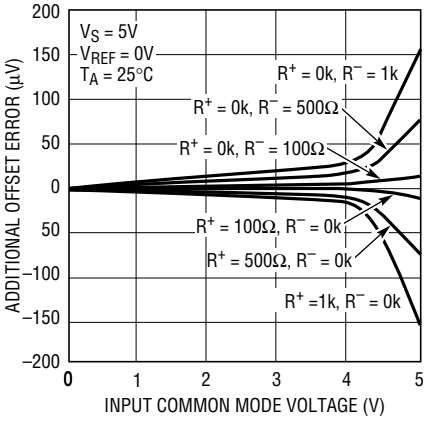


TYPICAL PERFORMANCE CHARACTERISTICS

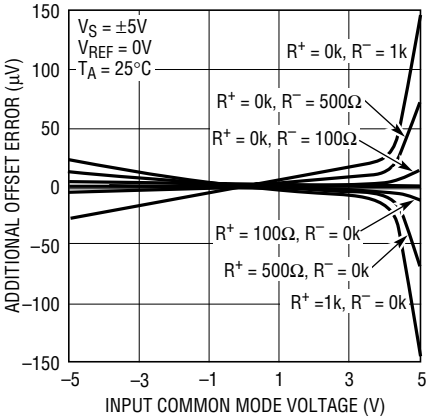
Error Due to Input R_S Mismatch vs Input Commom Mode (C_{IN} >1µF)



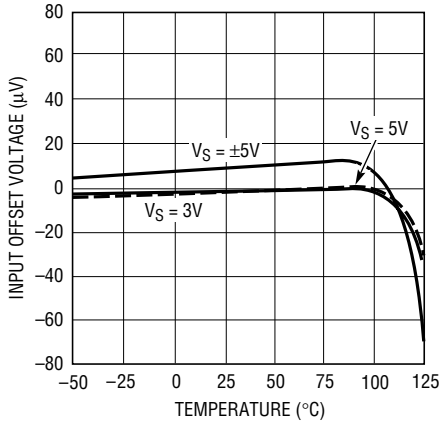
Error Due to Input R_S Mismatch vs Input Commom Mode (C_{IN} >1µF)



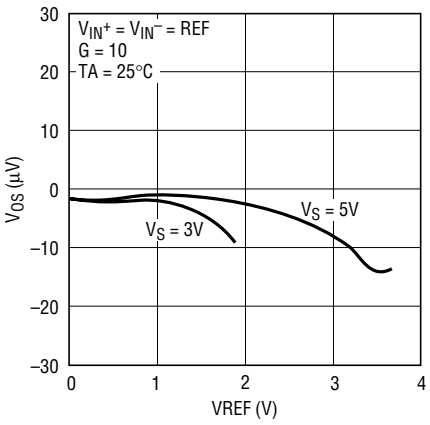
Error Due to Input R_S Mismatch vs Input Commom Mode (C_{IN} >1µF)



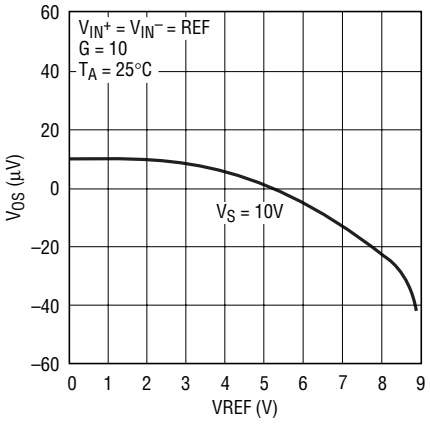
Offset Voltage vs Temperature



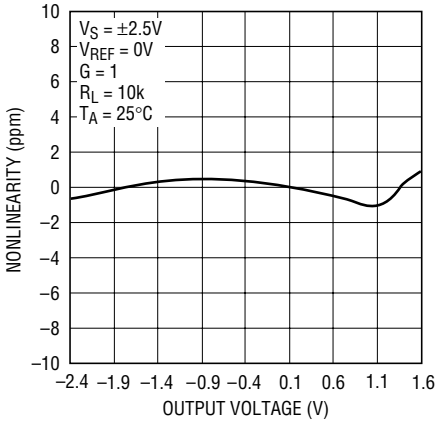
V_{OS} vs REF (Pin 5)



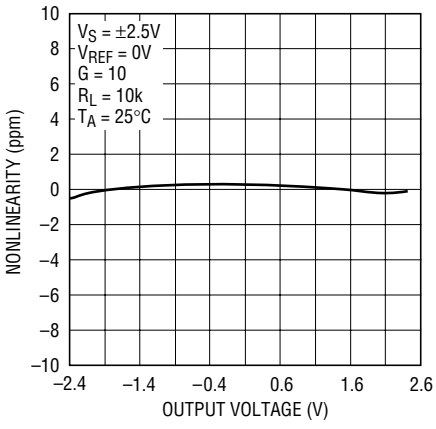
V_{OS} vs REF (Pin 5)



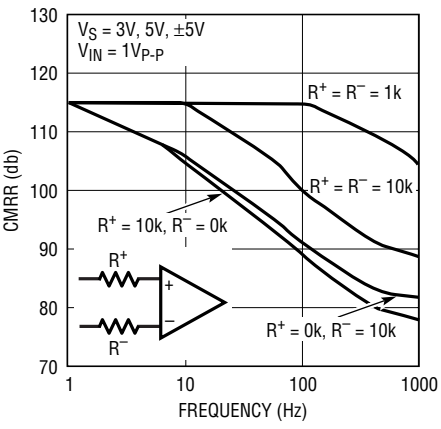
Gain Nonlinearity, G = 1



Gain Nonlinearity, G = 10

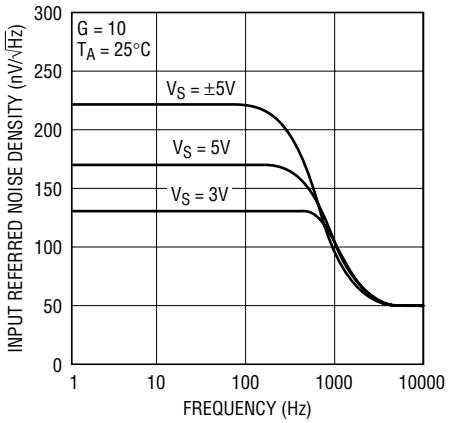


CMRR vs Frequency

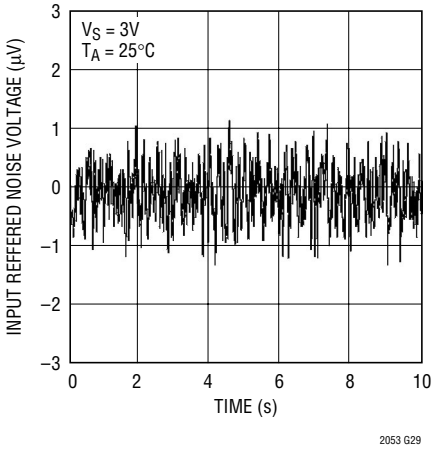


TYPICAL PERFORMANCE CHARACTERISTICS

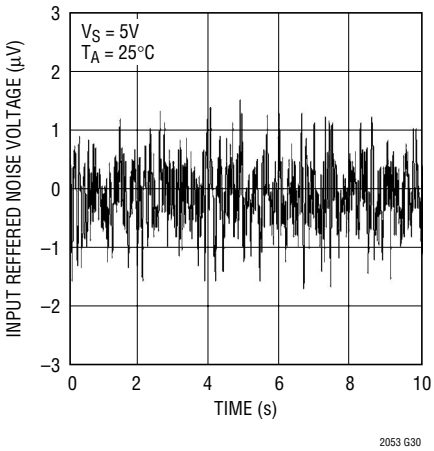
Input Voltage Noise Density vs Frequency



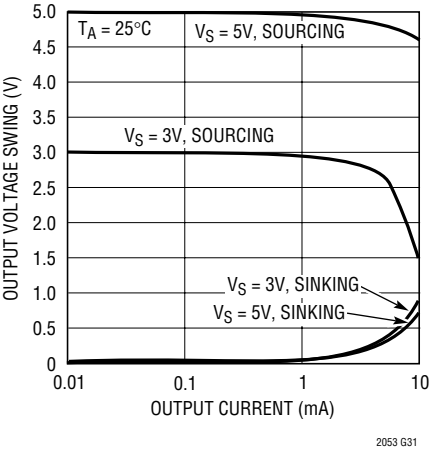
Input Referred Noise in 10Hz Bandwidth



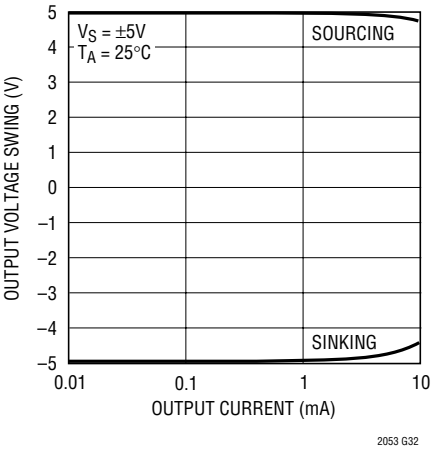
Input Referred Noise in 10Hz Bandwidth



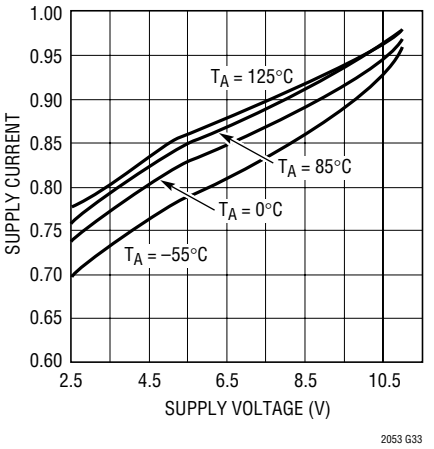
Output Voltage Swing vs Output Current



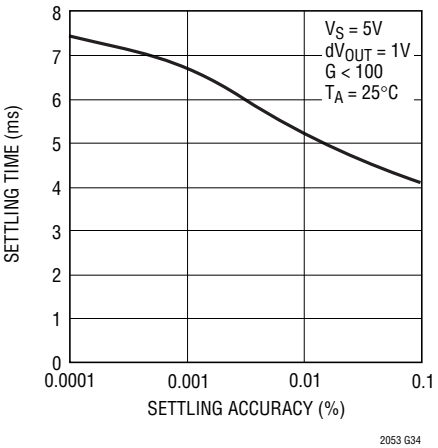
Output Voltage Swing vs Output Current



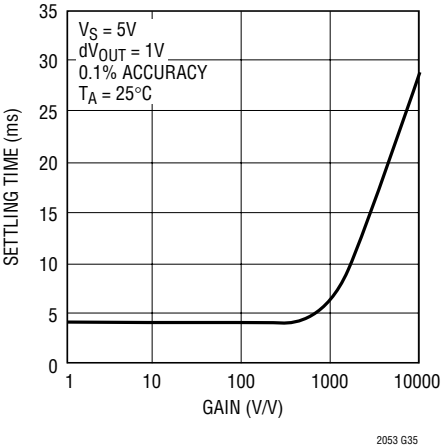
Supply Current vs Supply Voltage



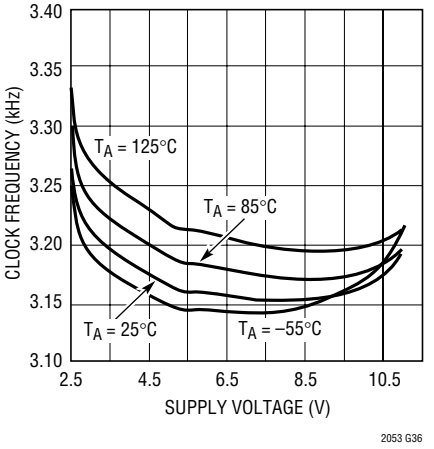
Low Gain Settling Time vs Settling Accuracy



Settling Time vs Gain



Internal Clock Frequency vs Supply Voltage



PIN FUNCTIONS

$\overline{EN}$ (Pin 1): Active Low Enable Pin.

–IN (Pin 2): Inverting Input.

+IN (Pin 3): Noninverting Input.

V^- (Pin 4): Negative Supply.

REF (Pin 5): Voltage Reference (V_{REF}) for Amplifier Output.

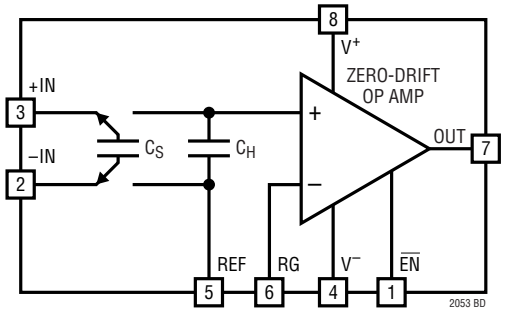
RG (Pin 6): Inverting Input of Internal Op Amp. With a resistor, R2, connected between the OUT pin and the RG pin and a resistor, R1, between the RG pin and the REF pin, the DC gain is given by 1 + R2 / R1.

OUT (Pin 7): Amplifier Output.

V_{OUT} = GAIN ($V_{+IN} – V_{–IN}$) + V_{REF}

V^+ (Pin 8): Positive Supply.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Theory of Operation

The LTC2053 uses an internal capacitor (C_S) to sample a differential input signal riding on a DC common mode voltage (see Block Diagram). This capacitor's charge is transferred to a second internal hold capacitor (C_H) translating the common mode of the input differential signal to that of the REF pin. The resulting signal is amplified by a zero-drift op amp in the noninverting configuration. The RG pin is the negative input of this op amp and allows external programmability of the DC gain. Simple filtering can be realized by using an external capacitor across the feedback resistor.

Input Voltage Range

The input common mode voltage range of the LTC2053 is rail-to-rail. However, the following equation limits the size of the differential input voltage:

$V^- \leq (V_{+IN} – V_{–IN}) + V_{REF} \leq V^+ – 1.3$

Where V_{+IN} and $V_{–IN}$ are the voltages of the +IN and –IN pins respectively, V_{REF} is the voltage at the REF pin and V^+ is the positive supply voltage.

For example, with a 3V single supply and a 0V to 100mV differential input voltage, V_{REF} must be between 0V and 1.6V.

±5 Volt Operation

When using the LTC2053 with supplies over 5.5V, care must be taken to limit the maximum difference between any of the input pins (+IN or –IN) and the REF pin to 5.5V; if not, the device will be damaged. For example, if rail-to-rail input operation is desired when the supplies are at ±5V, the REF pin should be 0V, ±0.5V. As a second example, if V^+ is 10V and V^- and REF are at 0V, the inputs should not exceed 5.5V.

APPLICATIONS INFORMATION

Settling Time

The sampling rate is 3kHz and the input sampling period during which C_S is charged to the input differential voltage V_{IN} is approximately 150µs. First assume that on each input sampling period, C_S is charged fully to V_{IN}. Since $C_S = C_H$ (= 1000pF), a change in the input will settle to N bits of accuracy at the op amp noninverting input after N clock cycles or 333µs(N). The settling time at the OUT pin is also affected by the settling of the internal op amp. Since the gain bandwidth of the internal op amp is typically 200kHz, the settling time is dominated by the switched capacitor front end for gains below 100 (see Typical Performance Characteristics).

Input Current

Whenever the differential input V_{IN} changes, C_H must be charged up to the new input voltage via C_S. This results in an input charging current during each input sampling period. Eventually, C_H and C_S will reach V_{IN} and, ideally, the input current would go to zero for DC inputs.

In reality, there are additional parasitic capacitors which disturb the charge on C_S every cycle even if V_{IN} is a DC voltage. For example, the parasitic bottom plate capacitor on C_S must be charged from the voltage on the REF pin to the voltage on the –IN pin every cycle. The resulting input charging current decays exponentially during each input sampling period with a time constant equal to R_SC_S. **If the voltage disturbance due to these currents settles before the end of the sampling period, there will be no errors due to source resistance or the source resistance mismatch between –IN and +IN. With R_S less than 10k, no DC errors occur due to this input current.**

In the Typical Performance Characteristics section of this data sheet, there are curves showing the additional error from non-zero source resistance in the inputs. If there are no large capacitors across the inputs, the amplifier is less sensitive to source resistance and source resistance mismatch. When large capacitors are placed across the inputs, the input charging currents described above result in larger DC errors, especially with source resistor mismatches.

Power Supply Bypassing

The LTC2053 uses a sampled data technique and therefore contains some clocked digital circuitry. It is therefore sensistive to supply bypassing. For single or dual supply operation, a 0.1µF ceramic capacitor must be connected between Pin 8 (V^+) and Pin 4 ($V^–$) with leads as short as possible.

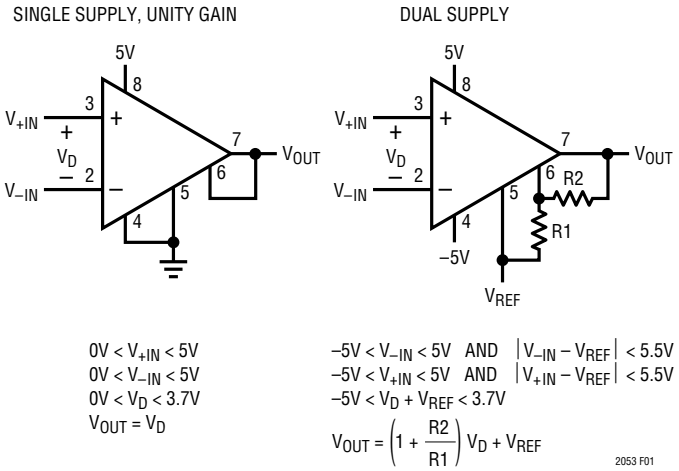
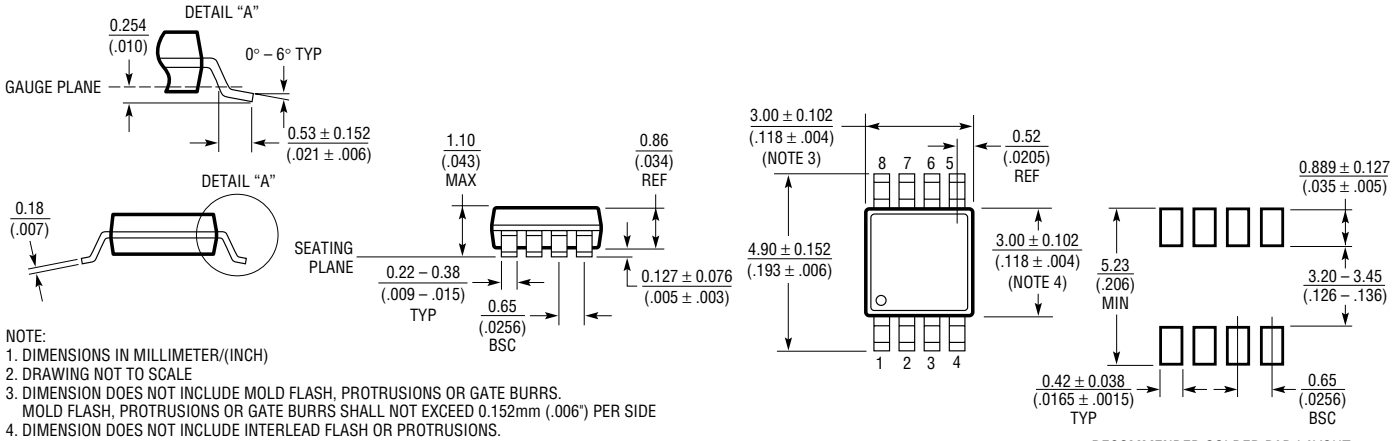


Figure 1

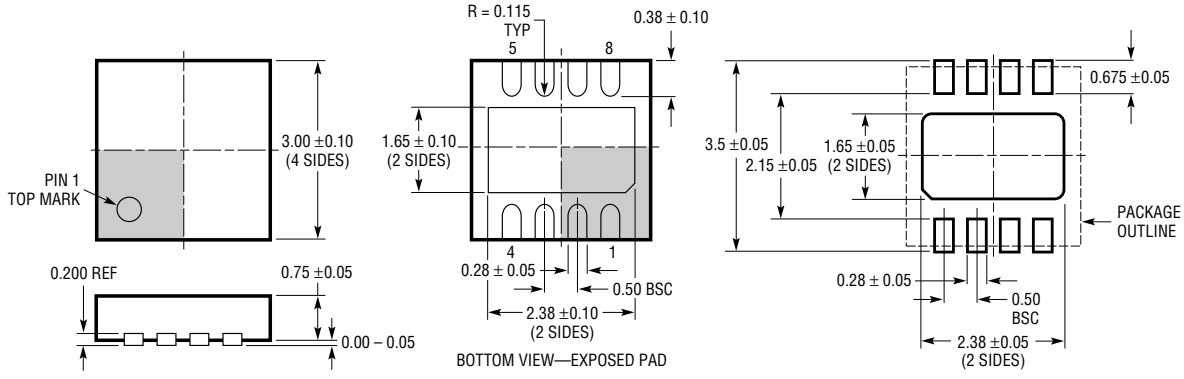
PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

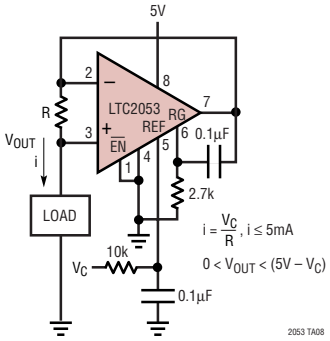
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



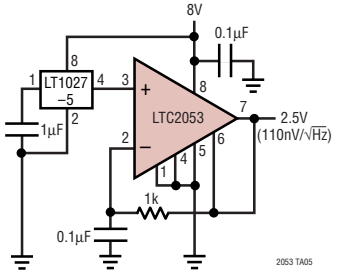
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

TYPICAL APPLICATIONS

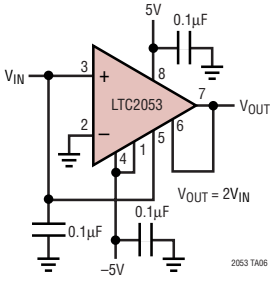
Precision Current Source



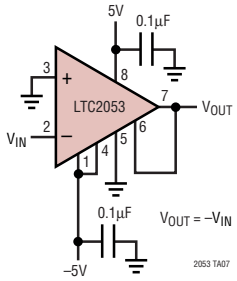
Precision ÷2 (Low Noise 2.5V Reference)



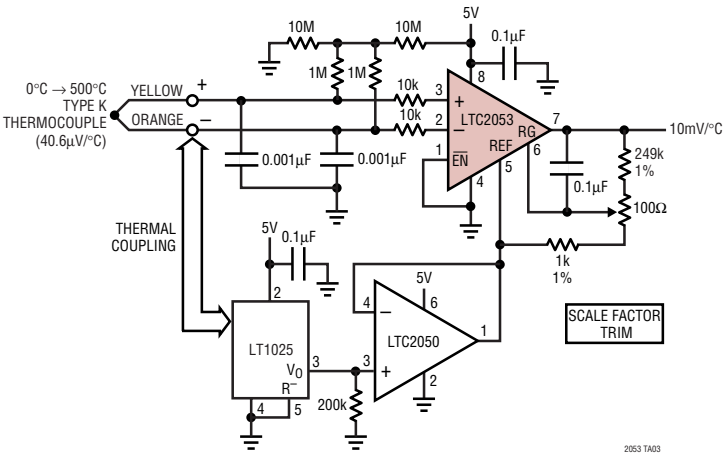
Precision Doubler (General Purpose)



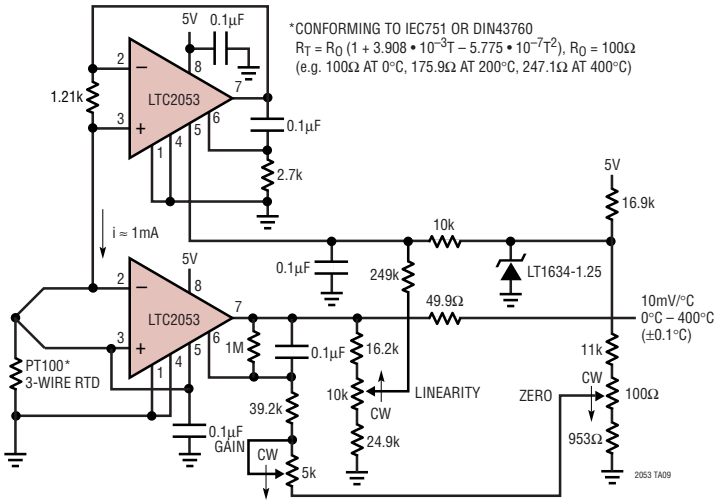
Precision Inversion (General Purpose)



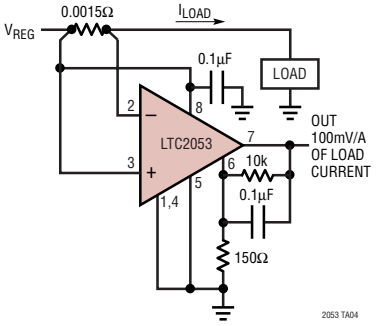
Differential Thermocouple Amplifier



Linearized Platinum RTD Amplifier



High Side Power Supply Current Sense



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1167	Single Resistor Gain Programmable, Precision Instrumentation Amplifier	Single Gain Set Resistor: G = 1 to 10,000, Low Noise: 7.5nV√Hz
LTC2050	Zero-Drift Operation Amplifier	SOT-23 Package
LTC2051	Dual Zero-Drift Operational Amplifier	MS8 Package
LTC6800	Single Supply, Zero Drift, Rail-to-Rail Input and Output Instrumentation Amplifier	MS8 Package, 100µV Max V_{OS}, 250nV/°C Max Drift