

### features

- Window-Watchdog With Programmable Delay and Window Ratio
- 6-Pin SOT-23 Package
- Supply Current of 9  $\mu\text{A}$  (Typ)
- Power On Reset Generator With a Fixed Delay Time of 25 ms
- Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, 5 V
- Open-Drain Reset Output
- Temperature Range . . .  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

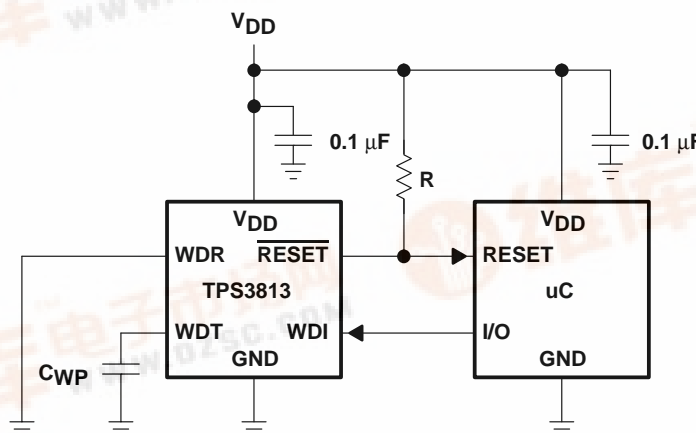
### description

The TPS3813 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power on,  $\overline{\text{RESET}}$  is asserted when supply voltage ( $V_{\text{DD}}$ ) becomes higher than 1.1 V. There after, the supervisory circuit monitors  $V_{\text{DD}}$  and keeps  $\overline{\text{RESET}}$  active as long as  $V_{\text{DD}}$  remains below the threshold voltage ( $V_{\text{IT}}$ ). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time,  $t_{\text{d}}$  = 25 ms typical, starts after  $V_{\text{DD}}$  has risen above the threshold voltage ( $V_{\text{IT}}$ ). When the supply voltage drops below the threshold voltage ( $V_{\text{IT}}$ ), the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage ( $V_{\text{IT}}$ ) set by an internal voltage divider.

For safety critical applications the TPS3813 family incorporates a so-called window-watchdog with programmable delay and window ratio. The upper limit of the watchdog time-out can be set by either connecting WDT to GND,  $V_{\text{DD}}$ , or using an external capacitor. The lower limit and thus the window ratio is set by connecting WDR to GND or  $V_{\text{DD}}$ . The supervised processor now needs to trigger the TPS3813 within this window not to assert a  $\overline{\text{RESET}}$ .

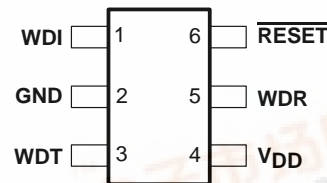
### typical operating circuit



### typical applications

- Applications Using DSPs, Microcontrollers, or Microprocessors
- Safety Critical Systems
- Automotive Systems
- Heating Systems

TPS3813  
DBV PACKAGE  
(TOP VIEW)



ACTUAL SIZE  
3,00 mm x 3,00 mm

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



# TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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## description continued

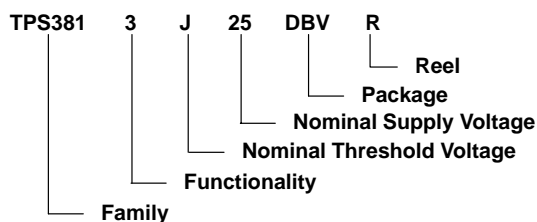
The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 6-pin SOT–23 package.

The TPS3813 devices are characterized for operation over a temperature range of –40°C to 85°C.

PACKAGE INFORMATION

| T <sub>A</sub> | DEVICE NAME   | THRESHOLD VOLTAGE | MARKING |
|----------------|---------------|-------------------|---------|
| –40°C to 85°C  | TPS3813J25DBV | 2.25 V            | PCDI    |
|                | TPS3813L30DBV | 2.64 V            | PEZI    |
|                | TPS3813K33DBV | 2.93 V            | PFAI    |
|                | TPS3813I50DBV | 4.55 V            | PFBI    |

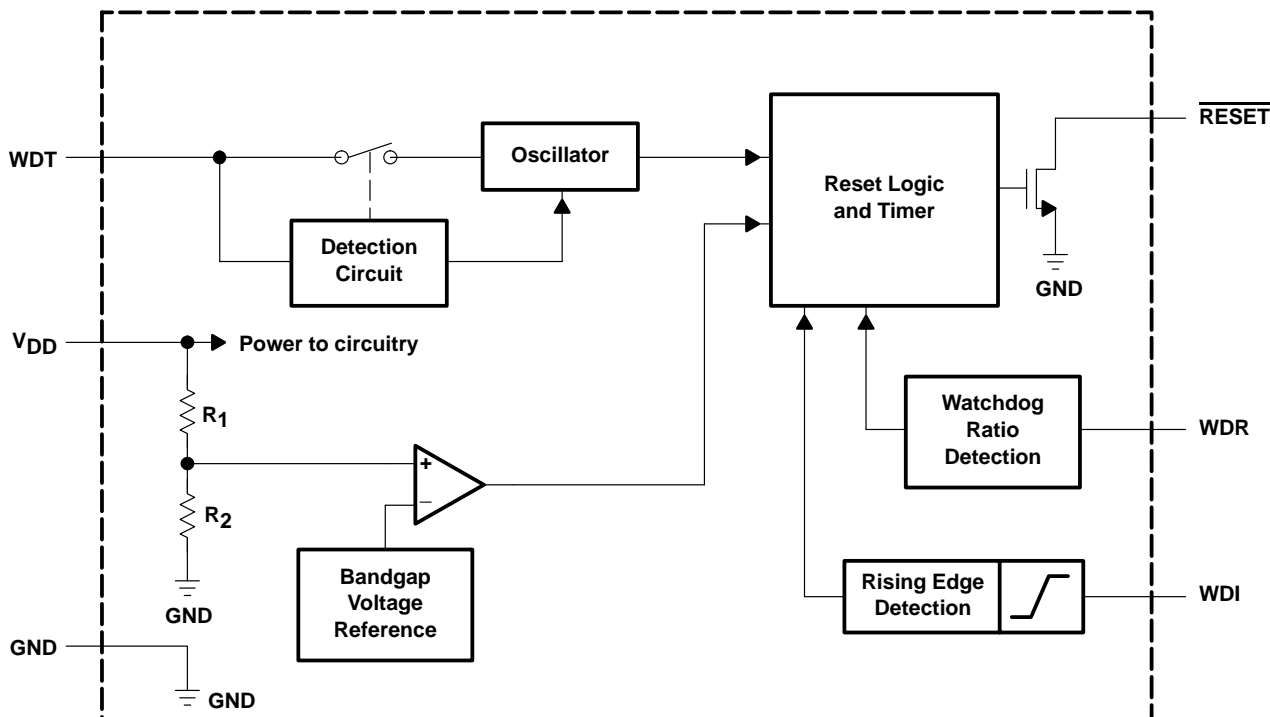
## ordering information



TPS3813  
FUNCTION/TRUTH TABLE

| V <sub>DD</sub> > V <sub>IT</sub> | $\overline{\text{RESET}}$ |
|-----------------------------------|---------------------------|
| 0                                 | L                         |
| 1                                 | H                         |

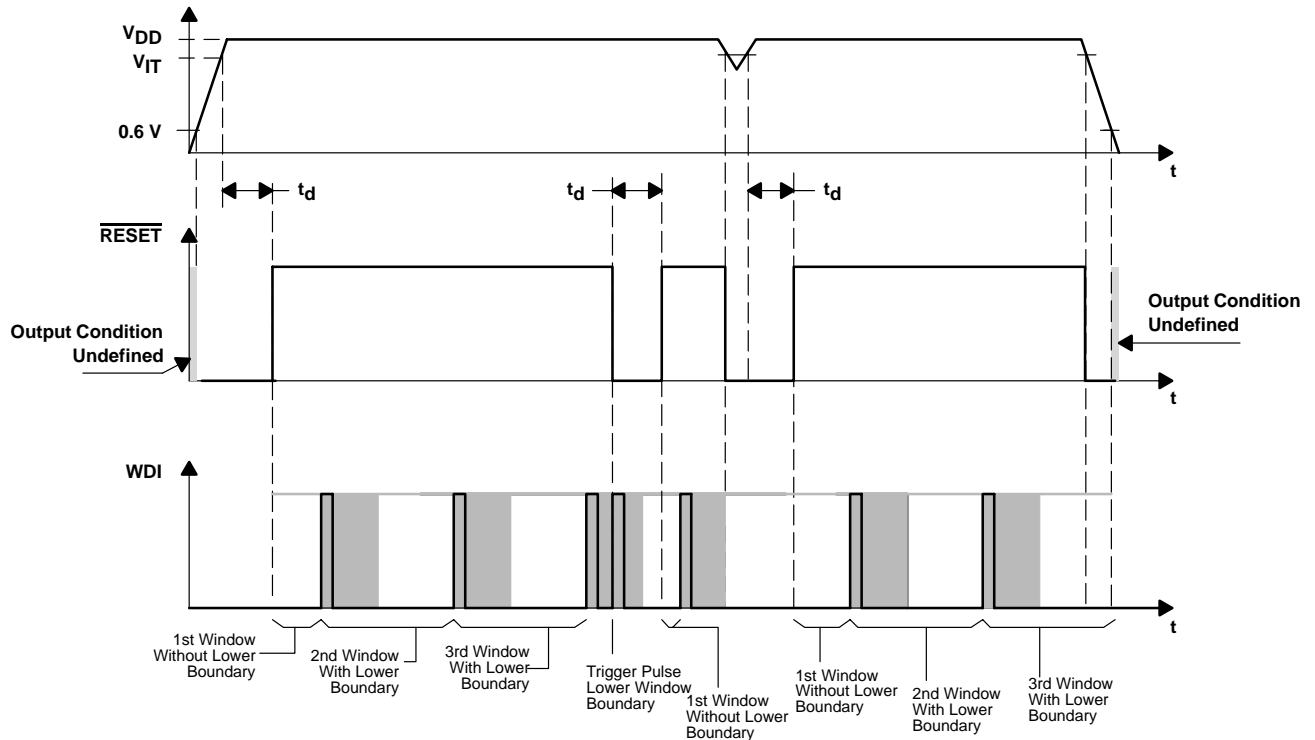
## functional schematic



# TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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## timing diagram



The lower boundary of the watchdog window starts with the rising edge of the WDI trigger pulse. At the same time, all internal timers will be reset. If an external capacitor is used, the lower boundary is impacted due to the different oscillator frequency. This is described in more detail in the following section. The timing diagram and especially the shaded boundary is prepared in a nonreal ratio scale to better visualize the description.

## Terminal Functions

| TERMINAL NAME             | NO. | I/O | DESCRIPTION                            |
|---------------------------|-----|-----|--|
| GND                       | 2   | I   | Ground                                 |
| $\overline{\text{RESET}}$ | 6   | O   | Open-drain reset output                |
| $V_{DD}$                  | 4   | I   | Supply voltage and supervising input   |
| WDI                       | 1   | I   | Watchdog timer input                   |
| WDR                       | 5   | I   | Selectable watchdog window ratio input |
| WDT                       | 3   | I   | Programmable watchdog delay input      |

# TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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## detailed description

### implemented window-watchdog settings

There are two different ways to set up the watchdog window. The first way is to use the implemented timing which is a default setting. Or, the default settings can be activated by wiring the WDT and WDR pin to  $V_{DD}$  or GND. There is a total of four different timings available with these settings. They are listed in the table below.

| SELECTED OPERATION MODE |                | WINDOW FRAME | LOWER WINDOW FRAME |
|-------------------------|----------------|--------------|--------------------|
| WDT = 0 V               | WDR = 0 V      | Max = 0.3 s  | Max = 9.46 ms      |
|                         |                | Typ = 0.25 s | Typ = 7.86 ms      |
|                         |                | Min = 0.2 s  | Min = 6.27 ms      |
|                         | WDR = $V_{DD}$ | Max = 0.3 s  | Max = 2.43 ms      |
|                         |                | Typ = 0.25 s | Typ = 2 ms         |
|                         |                | Min = 0.2 s  | Min = 1.58 ms      |
| WDT = $V_{DD}$          | WDR = 0 V      | Max = 3 s    | Max = 93.8 ms      |
|                         |                | Typ = 2.5 s  | Typ = 78.2 ms      |
|                         |                | Min = 2 s    | Min = 62.5 ms      |
|                         | WDR = $V_{DD}$ | Max = 3 s    | Max = 23.5 ms      |
|                         |                | Typ = 2.5 s  | Typ = 19.6 ms      |
|                         |                | Min = 2 s    | Min = 15.6 ms      |

To visualize the values named in the table, a timing diagram was prepared. It is used to describe the upper and lower boundary settings. For an application, the important boundaries are the  $t_{boundary,max}$  and  $t_{window,min}$ . Within these values, the watchdog timer should be retriggered to avoid a timeout condition or a boundary violation in the event of a trigger pulse in the lower boundary. The values in the table above are typical and worst case conditions. They are valid over the whole temperature range of  $-40^{\circ}C$  to  $85^{\circ}C$ .

In the shaded area of Figure 1, it cannot be predicted if the device will detect a violation or not and release a reset. This is also the case between the boundary tolerance of  $t_{boundary,min}$  and  $t_{boundary,max}$  as well as between  $t_{window,min}$  and  $t_{window,max}$ . It is important to set up the trigger pulses accordingly to avoid violations in these areas.

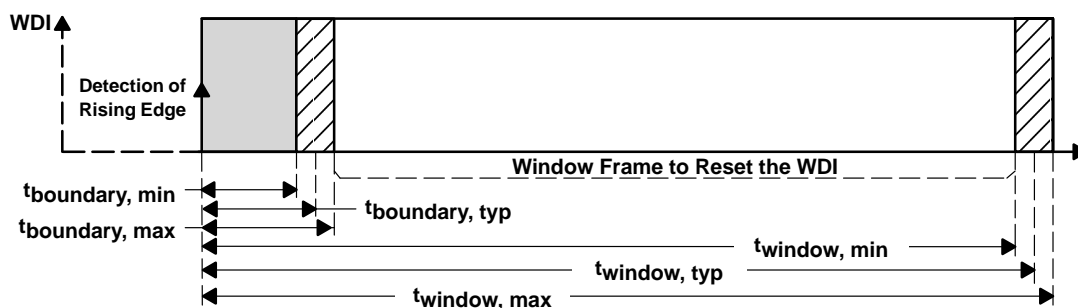


Figure 1. Upper and Lower Boundary Visualization

# TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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## detailed description (continued)

### timing rules of window-watchdog

After the reset of the supervisor is released, the lower boundary of the first WDI window is disabled. However, after the first WDI pulse low-to-high transition is detected, the lower boundary function of the window is enabled. All further WDI pulses will need to fit into the configured window frame.

### programmable window-watchdog by using an external capacitor

The upper boundary of the watchdog timer can be set by an external capacitor connected between the WDT pin and GND. Common consumer electronic capacitors can be used to implement this feature. They should have low ESR and low tolerances since the tolerances have to be considered if the calculations are performed. The first formula is used to calculate the upper window frame. After calculating the upper window frame, the lower boundary can be calculated. As in the last example, the most important values are the  $t_{\text{boundary,max}}$  and  $t_{\text{window,min}}$ . The trigger pulse has to fit into this window frame.

The external capacitor should have a value between a minimum of 47 pF and a maximum of 63 nF.

| SELECTED OPERATION MODE                     |                                     | WINDOW FRAME  |
|---|-------------------------------------|---|
| WDT = external capacitor $C_{\text{(ext)}}$ | WDR = 0 V and WDR = $V_{\text{DD}}$ | $t_{\text{window,max}} = 1.25 \times t_{\text{window,typ}}$ |
|   |                                     | $t_{\text{window,min}} = 0.75 \times t_{\text{window,typ}}$ |

$$t_{\text{window,typ}} = \left( \frac{C_{\text{(ext)}}}{15.55 \text{ pF}} + 1 \right) \times 6.25 \text{ ms}$$

### lower boundary calculation

The lower boundary can be calculated based on the values given in the switching characteristics. Additionally, facts have to be taken into account to verify that the lower boundary is where it is expected. Since the internal oscillator of the window watchdog is running free, any rising edge at the WDI pin will be taken into account at the next internal clock cycle. This happens regardless of the external source. Since the shift between internal and external clock is not known, it is best to consider the worst case condition for calculating this value.

| SELECTED OPERATION MODE                     |                       | LOWER BOUNDARY OF FRAME                                  |
|---|-----------------------|--|
| WDT = external capacitor $C_{\text{(ext)}}$ | WDR = 0 V             | $t_{\text{boundary,max}} = t_{\text{window,max}} / 23.5$ |
|   |                       | $t_{\text{boundary,typ}} = t_{\text{window,typ}} / 25.8$ |
|   |                       | $t_{\text{boundary,min}} = t_{\text{window,min}} / 28.7$ |
|   | WDR = $V_{\text{DD}}$ | $t_{\text{boundary,max}} = t_{\text{window,max}} / 51.6$ |
|   |                       | $t_{\text{boundary,typ}} = t_{\text{window,typ}} / 64.5$ |
|   |                       | $t_{\text{boundary,min}} = t_{\text{window,min}} / 92.7$ |

### watchdog software considerations

To benefit from the window watchdog feature and help the watchdog timer monitor the software execution more closely, it is recommended that the watchdog be set and reset at different points in the program rather than pulsing the watchdog input periodically by using the prescaler of a microcontroller or DSP. Furthermore, the watchdog trigger pulses should be set to different timings inside the window frame to release a defined reset, if the program should hang in any subroutine. This allows the window watchdog to detect timeouts of the trigger pulse as well as pulses that distort the lower boundary.

# TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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## detailed description (continued)

### application example

A typical application example (see Figure 2) is used to describe the function of the watchdog in more detail.

To configure the window watchdog function, two pins are provided by the TPS3813. These pins set the window timeout and ratio.

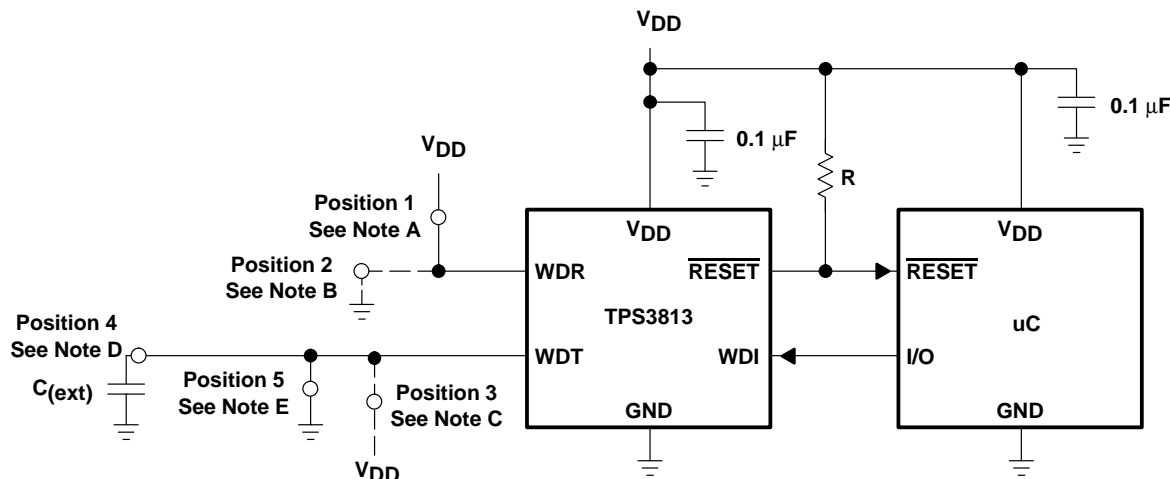
The window watchdog ratio is a fixed ratio, which determines the lower boundary of the window frame. It can be configured in two different frame sizes.

If the window watchdog ratio pin (WDR) is set to  $V_{DD}$ , Position 1 in Figure 2, then the lower window frame is a value based on a ratio calculation of the overall window timeout size: For the watchdog timeout pin (WDT) connected to GND, it is a ratio of 1:124.9, for WDT connected to  $V_{DD}$ , it is a ratio of 1:127.7, and for an external capacitor connected to WDT, it is a ratio of 1:64.5.

If the window watchdog ratio pin (WDR) is set to GND, Position 2, the lower window frame will be a value based on a ratio calculation of the overall window timeout size: For the watchdog timeout pin (WDT) connected to GND, it will be a ratio of 1:31.8, for WDT connected to  $V_{DD}$  it will be 1:32, and for an external capacitor connected to WDT it will be 1:25.8.

The watchdog timeout can be set in two fixed timings of 0.25 seconds and 2.5 seconds for the window or can be programmed by connecting an external capacitor with a low leakage current at WDT.

Example: If the watchdog timeout pin (WDT) is connected to  $V_{DD}$ , the timeout will be 2.5 seconds. If the window watchdog ratio pin (WDR) is set in this configuration to a ratio of 1:127.7 by connecting the pin to  $V_{DD}$ , the lower boundary is 19.6 ms.



- NOTES:
- A. Watchdog window ratio
  - B. Watchdog window ratio
  - C. Watchdog timeout set to typical 2.5 sec
  - D. Watchdog timeout programmed by external capacitor
  - E. Watchdog timeout set to typical 0.25 sec

Figure 2. Application Example

# TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

|  |                              |
|--|------------------------------|
| Supply voltage, $V_{DD}$ (see Note 1)                          | 7 V                          |
| All other pins (see Note 1)                                    | -0.3 V to 7 V                |
| Maximum low output current, $I_{OL}$                           | 5 mA                         |
| Maximum high output current, $I_{OH}$                          | -5 mA                        |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )  | $\pm 20$ mA                  |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ ) | $\pm 20$ mA                  |
| Continuous total power dissipation                             | See Dissipation Rating Table |
| Operating free-air temperature range, $T_A$                    | -40°C to 85°C                |
| Storage temperature range, $T_{stg}$                           | -65°C to 150°C               |
| Soldering temperature  | 260°C                        |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than  $t = 1000$ h continuously.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A < 25^\circ\text{C}$ | DERATING FACTOR                | $T_A = 70^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ |
|---------|--------------------------|--------------------------------|--------------------------|--------------------------|
|         | POWER RATING             | ABOVE $T_A = 25^\circ\text{C}$ | POWER RATING             | POWER RATING             |
| DBV     | 437 mW                   | 3.5 mW/°C                      | 280 mW                   | 227 mW                   |

## recommended operating conditions at specified temperature range

|  | MIN                 | MAX            | UNIT |
|--|---------------------|----------------|------|
| Supply voltage, $V_{DD}$                                 | 2                   | 6              | V    |
| Input voltage, $V_I$                                     | 0                   | $V_{DD} + 0.3$ | V    |
| High-level input voltage, $V_{IH}$                       | $0.7 \times V_{DD}$ |                | V    |
| Low-level input voltage, $V_{IL}$                        | $0.3 \times V_{DD}$ |                | V    |
| Input transition rise and fall rate, $\Delta t/\Delta V$ | 100                 |                | ns/V |
| Pulse width of WDI trigger pulse, $t_w$                  | 50                  |                | ns   |
| Operating free-air temperature range, $T_A$              | -40                 | 85             | °C   |

# TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                           |   | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNIT |    |
|-------------------------------------|---|--|--|------|------|------|----|
| V <sub>OL</sub>                     | Low-level output voltage                            | V <sub>DD</sub> = 2 V to 6 V, I <sub>OL</sub> = 500 μA                       |  |      | 0.2  | V    |    |
|                                     |   | V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 2 mA                              |  |      | 0.4  |      |    |
|                                     |   | V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 4 mA                                |  |      | 0.4  |      |    |
| Power up reset voltage (see Note 2) |   | V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 50 μA                             |  |      | 0.2  | V    |    |
| V <sub>IT</sub>                     | Negative-going input threshold voltage (see Note 3) | T <sub>A</sub> = -40°C – 85°C  | TPS3813J25   | 2.2  | 2.25 | 2.3  | V  |
|                                     |   |  | TPS3813L30   | 2.58 | 2.64 | 2.7  |    |
|                                     |   |  | TPS3813K33   | 2.87 | 2.93 | 3    |    |
|                                     |   |  | TPS3813I50   | 4.45 | 4.55 | 4.65 |    |
| V <sub>hys</sub>                    | Hysteresis  |  | TPS3813J25   | 30   |      | mV   |    |
|                                     |   |  | TPS3813L30   | 35   |      |      |    |
|                                     |   |  | TPS3813K33   | 40   |      |      |    |
|                                     |   |  | TPS3813I50   | 60   |      |      |    |
| I <sub>IH</sub>                     | High-level input current                            | WDI, WDR   | WDI = V <sub>DD</sub> = 6 V, WDR = V <sub>DD</sub> = 6 V                       |      | -25  | 25   | nA |
|                                     |   | WDT  | WDT = V <sub>DD</sub> = 6 V, V <sub>DD</sub> > V <sub>IT</sub><br>RESET = High |      | -100 | 100  |    |
| I <sub>IL</sub>                     | Low-level input current                             | WDI, WDR   | WDI = 0 V, WDR = 0 V, V <sub>DD</sub> = 6 V                                    |      | -25  | 25   | nA |
|                                     |   | WDT  | WDT = 0 V, V <sub>DD</sub> > V <sub>IT</sub> , RESET = High                    |      | -100 | 100  |    |
| I <sub>OH</sub>                     | High-level output current                           | V <sub>DD</sub> = V <sub>IT</sub> + 0.2 V, V <sub>OH</sub> = V <sub>DD</sub> |  |      | 25   | nA   |    |
| I <sub>DD</sub>                     | Supply current                                      | V <sub>DD</sub> = 2 V output unconnected                                     |  | 9    | 13   | μA   |    |
|                                     |   | V <sub>DD</sub> = 5 V output unconnected                                     |  | 20   | 25   |      |    |
| C <sub>i</sub>                      | Input capacitance                                   | V <sub>I</sub> = 0 V to V <sub>DD</sub>                                      |  | 5    |      | pF   |    |

NOTES: 2. The lowest supply voltage at which RESET becomes active. t<sub>r</sub> V<sub>DD</sub> ≥ 15 μs/V.  
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near to the supply terminals.

## timing requirements at R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = -40°C to 85°C

| PARAMETER      | TEST CONDITIONS                | MIN  | TYP | MAX | UNIT |
|----------------|--------------------------------|--|-----|-----|------|
| t <sub>w</sub> | Pulse width at V <sub>DD</sub> | V <sub>DD</sub> = V <sub>IT-</sub> + 0.2 V, V <sub>DD</sub> = V <sub>IT-</sub> - 0.2 V |     | 3   | μs   |

## switching characteristics at R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = -40°C to 85°C

| PARAMETER             |  | TEST CONDITIONS   | MIN  | TYP        | MAX  | UNIT |    |
|-----------------------|--|---|--|------------|------|------|----|
| t <sub>d</sub>        | Delay time   | V <sub>DD</sub> ≥ V <sub>IT</sub> + 0.2 V, See timing diagram | 20   | 25         | 30   | ms   |    |
| t <sub>t(out)</sub>   | Watchdog time-out                                  | Upper limit   | WDT = 0 V  | 0.2        | 0.25 | 0.3  | s  |
|                       |  |   | WDT = V <sub>DD</sub>  | 2          | 2.5  | 3    |    |
|                       |  |   | WDT = programmable (see Note 4)  | See Note 5 |      |      | ms |
| Watchdog window ratio |  | WDR = 0 V, WDT = 0 V  | 1:31.8   |            |      |      |    |
|                       |  | WDR = 0 V, WDT = V <sub>DD</sub>                              | 1:32   |            |      |      |    |
|                       |  | WDR = 0 V, WDT = programmable                                 | 1:25.8   |            |      |      |    |
|                       |  | WDR = V <sub>DD</sub> , WDT = 0 V                             | 1:124.9  |            |      |      |    |
|                       |  | WDR = V <sub>DD</sub> , WDT = V <sub>DD</sub>                 | 1:127.7  |            |      |      |    |
|                       |  | WDR = V <sub>DD</sub> , WDT = programmable                    | 1:64.5   |            |      |      |    |
| t <sub>PHL</sub>      | Propagation (delay) time, high-to-low-level output | V <sub>DD</sub> to RESET delay                                | V <sub>IL</sub> = V <sub>IT</sub> - 0.2 V, V <sub>IH</sub> = V <sub>IT</sub> + 0.2 V | 30         | 50   | μs   |    |

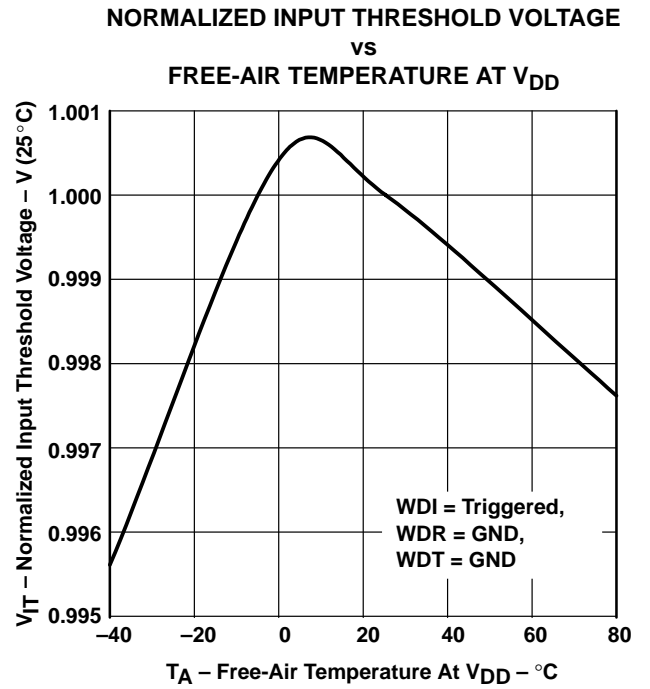
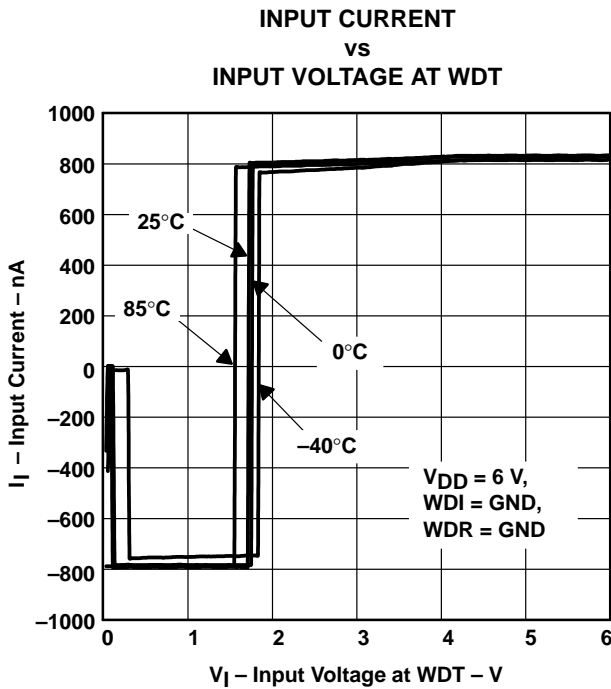
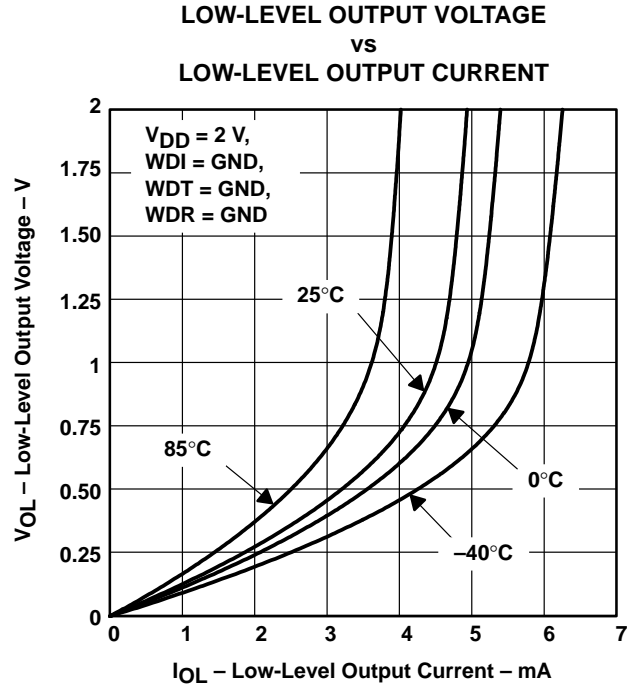
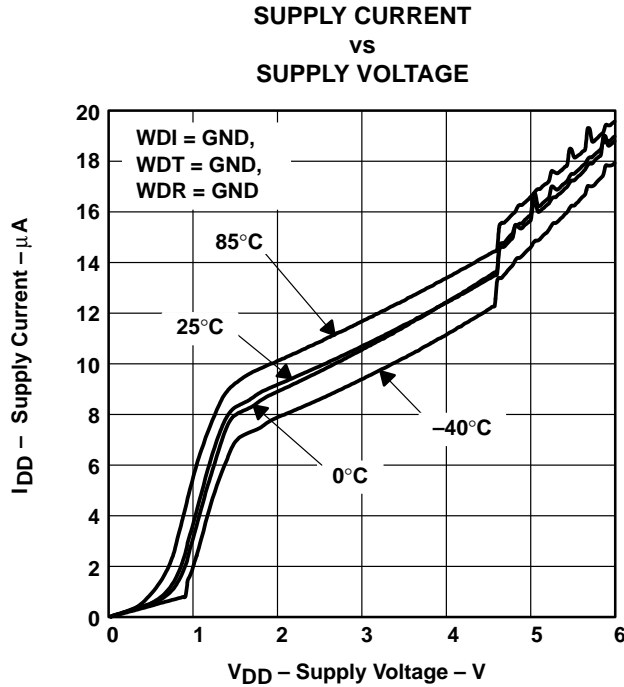
NOTES: 4. 155 pF < C<sub>(ext)</sub> < 63 nF  
5. (C<sub>(ext)</sub> ÷ 15.55 pF + 1) × 6.25 ms



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## TYPICAL CHARACTERISTICS



# TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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## TYPICAL CHARACTERISTICS

MINIMUM PULSE DURATION AT  $V_{DD}$   
vs  
 $V_{DD}$  THRESHOLD OVERDRIVE VOLTAGE

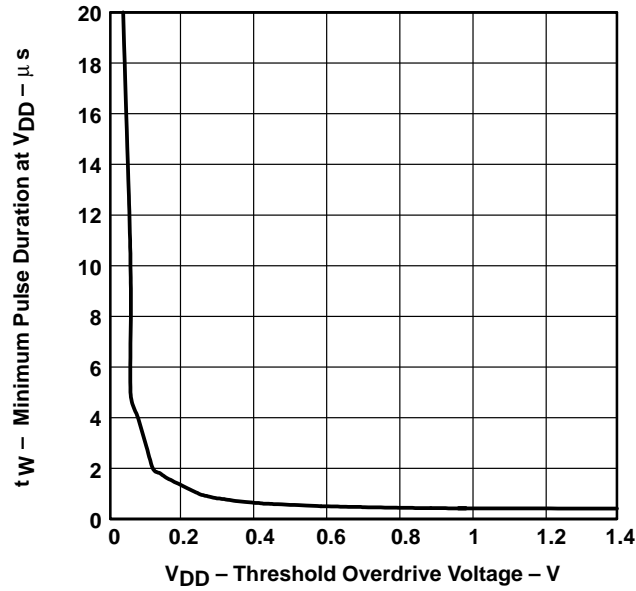


Figure 7

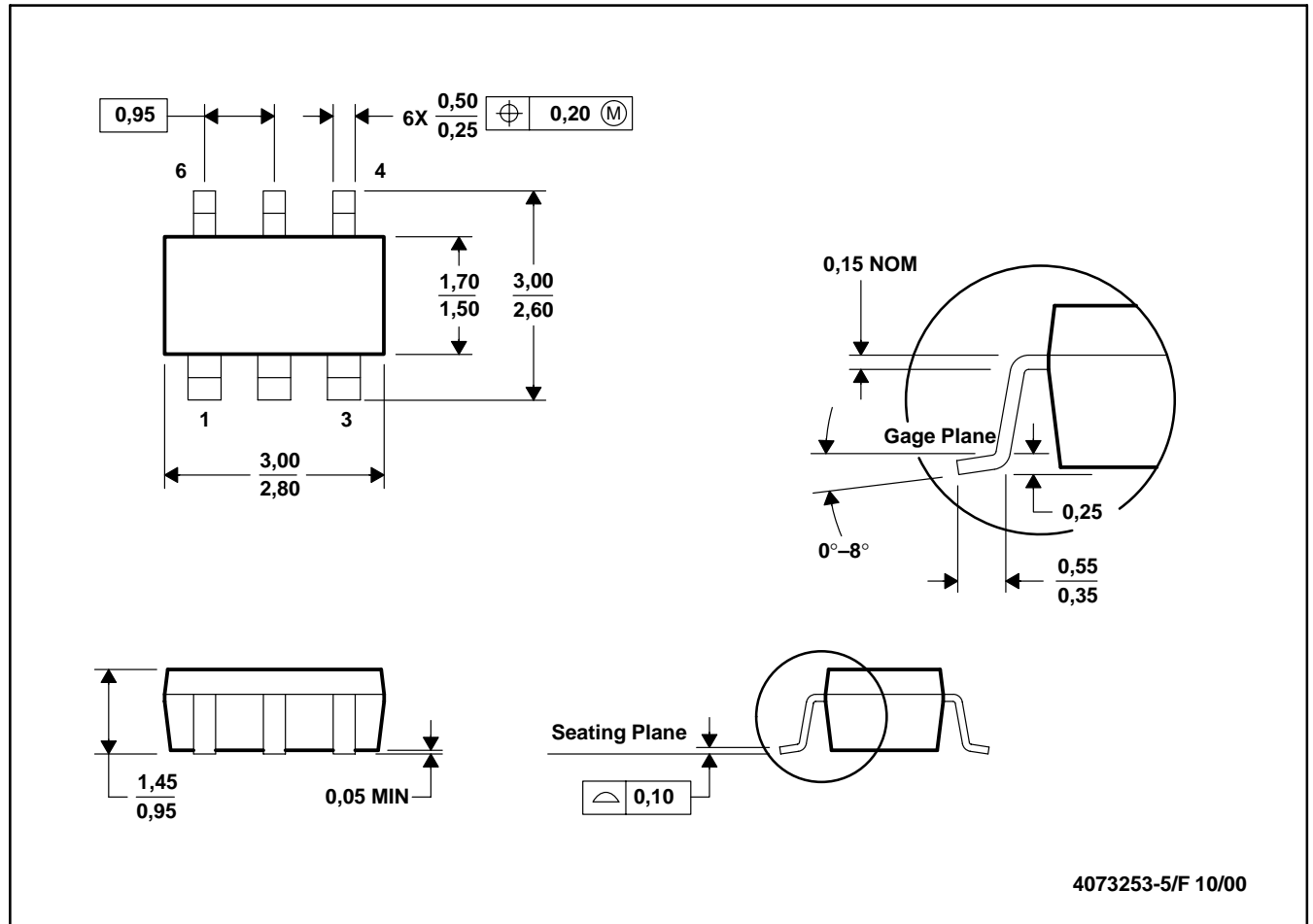
TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50  
 PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

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MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Leads 1, 2, 3 are wider than leads 4, 5, 6 for package orientation.

## IMPORTANT NOTICE

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TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

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