

# SN54AHCT573 SN74AHCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS243L – OCTOBER 1995 – REVISED JANUARY 2000

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

## description

The 'AHCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

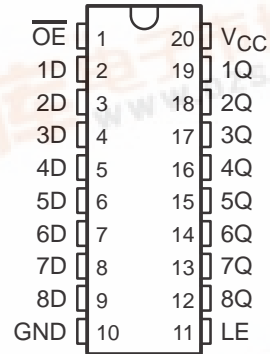
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

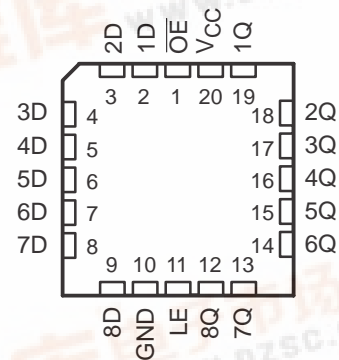
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT573 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHCT573 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54AHCT573 ... J OR W PACKAGE  
SN74AHCT573 ... DB, DGV, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT573 ... FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each latch)

| INPUTS          |    |   | OUTPUT |
|-----------------|----|---|--------|
| $\overline{OE}$ | LE | D | Q      |
| L               | H  | H | H      |
| L               | H  | L | L      |
| L               | L  | X | $Q_0$  |
| H               | X  | X | Z      |

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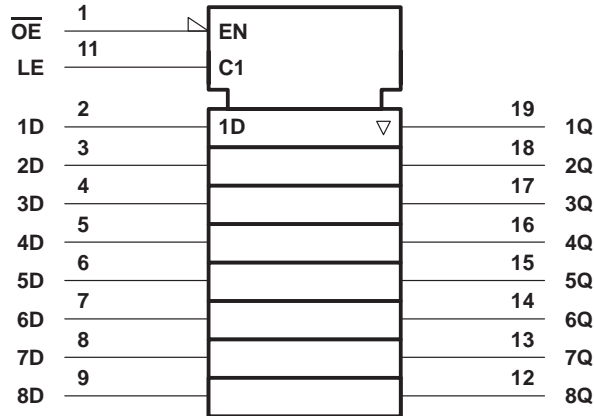


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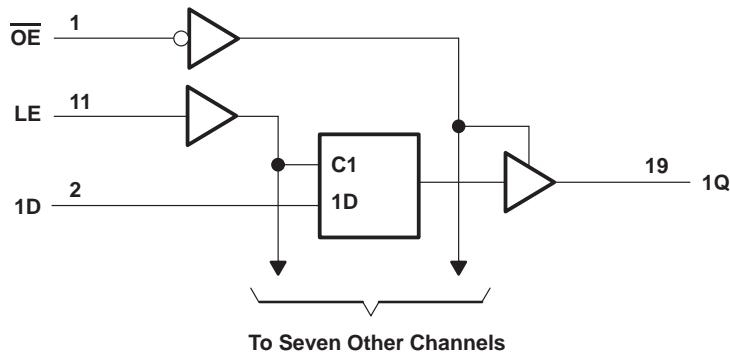
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|  |                            |
|--|----------------------------|
| Supply voltage range, $V_{CC}$                                 | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                        | –0.5 V to 7 V              |
| Output voltage range, $V_O$ (see Note 1)                       | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                    | –20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) | ±20 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )     | ±25 mA                     |
| Continuous current through $V_{CC}$ or GND                     | ±75 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 2):         |                            |
| DB package   | 70°C/W                     |
| DGV package  | 92°C/W                     |
| DW package   | 58°C/W                     |
| N package  | 69°C/W                     |
| PW package   | 83°C/W                     |
| Storage temperature range, $T_{stg}$                           | –65°C to 150°C             |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

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## recommended operating conditions (see Note 3)

|                 |                                    | SN54AHCT573 |                 | SN74AHCT573 |                 | UNIT |
|-----------------|------------------------------------|-------------|-----------------|-------------|-----------------|------|
|                 |                                    | MIN         | MAX             | MIN         | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     | 4.5         | 5.5             | 4.5         | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | 2           |                 | 2           |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            |             | 0.8             |             | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      | 0           | 5.5             | 0           | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     | 0           | V <sub>CC</sub> | 0           | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          |             | -8              |             | -8              | mA   |
| I <sub>OL</sub> | Low-level output current           |             | 8               |             | 8               | mA   |
| Δt/Δv           | Input transition rise or fall rate |             | 20              |             | 20              | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     | -55         | 125             | -40         | 85              | °C   |

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER          | TEST CONDITIONS   | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |       | SN54AHCT573 |      | SN74AHCT573 |     | UNIT |
|--------------------|---|-----------------|-----------------------|-----|-------|-------------|------|-------------|-----|------|
|                    |   |                 | MIN                   | TYP | MAX   | MIN         | MAX  | MIN         | MAX |      |
| V <sub>OH</sub>    | I <sub>OH</sub> = -50 μA                                    | 4.5 V           | 4.4                   | 4.5 |       | 4.4         |      | 4.4         | V   |      |
|                    | I <sub>OH</sub> = -8 mA                                     |                 | 3.94                  |     |       | 3.8         |      | 3.8         |     |      |
| V <sub>OL</sub>    | I <sub>OL</sub> = 50 μA                                     | 4.5 V           |                       |     | 0.1   |             |      | 0.1         | V   |      |
|                    | I <sub>OL</sub> = 8 mA                                      |                 |                       |     | 0.36  |             | 0.44 | 0.44        |     |      |
| I <sub>I</sub>     | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 0 V to 5.5 V    |                       |     | ±0.1  |             | ±1*  | ±1          | μA  |      |
| I <sub>OZ</sub>    | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |     | ±0.25 |             | ±2.5 | ±2.5        | μA  |      |
| I <sub>CC</sub>    | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |     | 4     |             | 40   | 40          | μA  |      |
| ΔI <sub>CC</sub> † | One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  | 5.5 V           |                       |     | 1.35  |             | 1.5  | 1.5         | mA  |      |
| C <sub>i</sub>     | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             |                       | 2.5 | 10    |             |      | 10          | pF  |      |
| C <sub>o</sub>     | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5 V             |                       | 3   |       |             |      |             | pF  |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

## timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

|                 |                             | T <sub>A</sub> = 25°C |     | SN54AHCT573 |     | SN74AHCT573 |     | UNIT |
|-----------------|-----------------------------|-----------------------|-----|-------------|-----|-------------|-----|------|
|                 |                             | MIN                   | MAX | MIN         | MAX | MIN         | MAX |      |
| t <sub>w</sub>  | Pulse duration, LE high     | 5                     |     | 5           |     | 5           |     | ns   |
| t <sub>su</sub> | Setup time, data before LE↓ | 3.5                   |     | 3.5         |     | 3.5         |     | ns   |
| t <sub>h</sub>  | Hold time, data after LE↓   | 1.5                   |     | 1.5         |     | 1.5         |     | ns   |

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER   | FROM (INPUT)    | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |       |     | SN54AHCT573 |     | SN74AHCT573 |     | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|-------|-----|-------------|-----|-------------|-----|------|
|             |                 |             |                      | MIN                      | TYP   | MAX | MIN         | MAX | MIN         | MAX |      |
| $t_{PLH}$   | D               | Q           | $C_L = 15\text{ pF}$ | 4.2*                     | 6*    | 1*  | 6.5*        | 1   | 6.5         | ns  |      |
| $t_{PHL}$   |                 |             |                      | 5.1*                     | 7*    | 1*  | 9*          | 1   | 9           |     |      |
| $t_{PLH}$   | LE              | Q           | $C_L = 15\text{ pF}$ | 4.7*                     | 6.5*  | 1*  | 7.5*        | 1   | 7.5         | ns  |      |
| $t_{PHL}$   |                 |             |                      | 5.6*                     | 7.5*  | 1*  | 9*          | 1   | 9           |     |      |
| $t_{PZH}$   | $\overline{OE}$ | Q           | $C_L = 15\text{ pF}$ | 4.1*                     | 6.5*  | 1*  | 7*          | 1   | 7           | ns  |      |
| $t_{PZL}$   |                 |             |                      | 5.5*                     | 7.5*  | 1*  | 10*         | 1   | 10          |     |      |
| $t_{PHZ}$   | $\overline{OE}$ | Q           | $C_L = 15\text{ pF}$ | 5.5*                     | 8*    | 1*  | 11*         | 1   | 11          | ns  |      |
| $t_{PLZ}$   |                 |             |                      | 5.4*                     | 8*    | 1*  | 9.5*        | 1   | 9.5         |     |      |
| $t_{PLH}$   | D               | Q           | $C_L = 50\text{ pF}$ | 5.2                      | 7     | 1   | 7.5         | 1   | 7.5         | ns  |      |
| $t_{PHL}$   |                 |             |                      | 6.1                      | 8     | 1   | 10          | 1   | 10          |     |      |
| $t_{PLH}$   | LE              | Q           | $C_L = 50\text{ pF}$ | 5.7                      | 7.5   | 1   | 8.5         | 1   | 8.5         | ns  |      |
| $t_{PHL}$   |                 |             |                      | 6.6                      | 8.5   | 1   | 10          | 1   | 10          |     |      |
| $t_{PZH}$   | $\overline{OE}$ | Q           | $C_L = 50\text{ pF}$ | 5.1                      | 7.5   | 1   | 8           | 1   | 8           | ns  |      |
| $t_{PZL}$   |                 |             |                      | 6.5                      | 8.5   | 1   | 11          | 1   | 11          |     |      |
| $t_{PHZ}$   | $\overline{OE}$ | Q           | $C_L = 50\text{ pF}$ | 6.7                      | 9     | 1   | 12          | 1   | 12          | ns  |      |
| $t_{PLZ}$   |                 |             |                      | 6.4                      | 9     | 1   | 10.5        | 1   | 10.5        |     |      |
| $t_{sk(o)}$ |                 |             | $C_L = 50\text{ pF}$ |                          | 1.5** |     |             |     | 1.5         | ns  |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

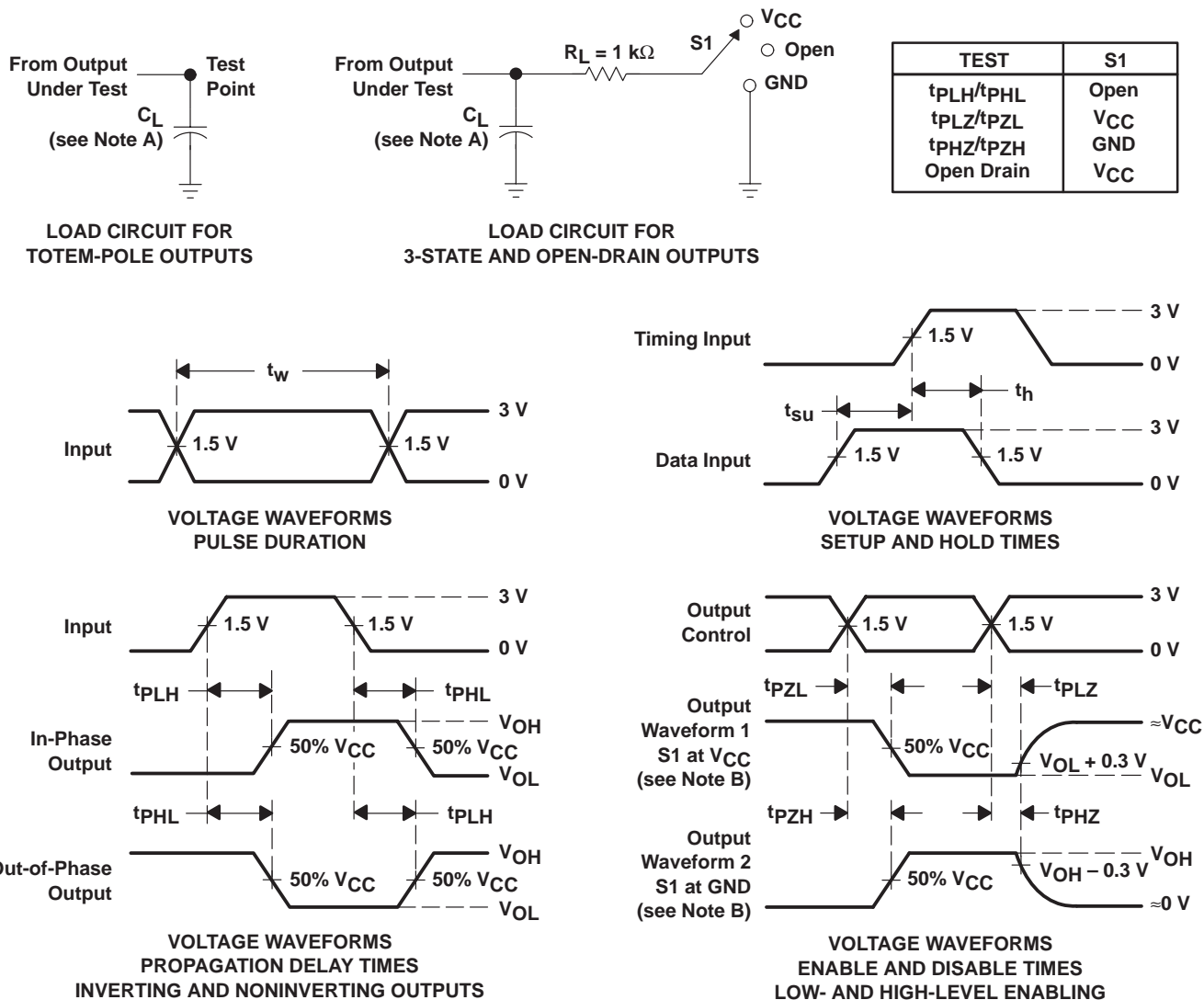
## operating characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

| PARAMETER                              | TEST CONDITIONS             | TYP | UNIT |
|--|-----------------------------|-----|------|
| $C_{pd}$ Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 16  | pF   |

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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