3N200

Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 500 MHz

Applications

- RF amplifier, mixer, and IF amplifier in military and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

RCA-3N200♦ is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS▲ pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N200 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N200 make it useful for a wide variety of rf-amplifier applications at frequencies up to 500 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N200 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N200 is hermetically sealed in the metal JEDEC TO-72 package.

▲ Metal-Oxide-Semiconductor.
♦ Formerly developmental type TA7684

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥1/32 inch from seating surface for 10 seconds max.	265	°C

*In accordance with JEDEC registration data format (JS-9 RDF-19A)

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- Wide dynamic range permits large-signal handling before overload
- Dual-gate permits simplified agc circuitry
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance — g_{fs} = 15,000 μmho (typ.)
- High unneutralized RF power gain — G_{ps} = 12.5 dB (typ.) at 400 MHz = 19 dB (typ.) at 200 MHz
- Low VHF noise figure — 3.9 dB (typ.) at 400 MHz 3.0 dB (typ.) at 200 MHz

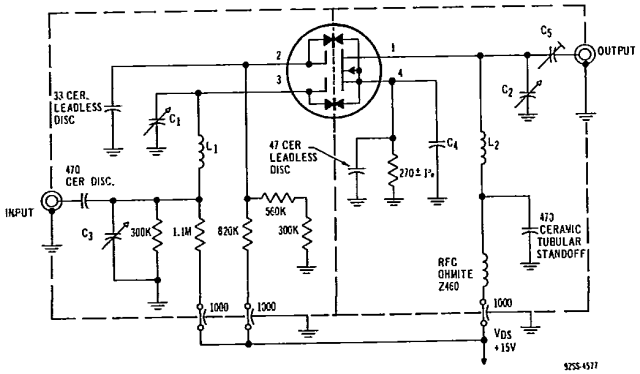
3N200

ELECTRICAL CHARACTERISTICS at T_A = 25°C unless otherwise specified		SYMBOLS	TEST CONDITIONS		LIMITS Min.	Typ.	Max.	UNITS
* Gate No. 1-to-Source Cutoff Voltage		$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G2S} = +4 V		-0.1	-1	-3	V
* Gate No. 2-to-Source Cutoff Voltage		$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G1S} = 0		-0.1	-1	-3	V
* Gate No. 1-Terminal Forward Current		I_{G1SSF}	V_{G1S} = +1 V, V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Gate No. 1-Terminal Reverse Current		I_{G1SSR}	V_{G1S} = -6 V, V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Gate No. 2-Terminal Forward Current		I_{G2SSF}	V_{G2S} = +6 V, V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Gate No. 2-Terminal Reverse Current		I_{G2SSR}	V_{G2S} = -6 V, V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Zero-Bias Drain Current		I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V		0.5	5.0	12	mA
* Forward Transconductance (Gate No. 1-to-Drain)		g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V	f = 1 kHz	10,000	15,000	20,000	μmho
Small-Signal, Short-Circuit Input Capacitance†		C_{iss}		f = 1 MHz	4.0	6.0	8.5	pF
* Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦		C_{rss}			0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance		C_{oss}			–	2.0	–	pF
* Power Gain (see Fig. 1)		G_{PS}		f = 400 MHz	10	12.5	–	dB
Noise Figure (see Fig. 1)		NF			–	3.9	6.0	dB
* Bandwidth		BW			28	–	38	MHz
* Gate-to-Source Forward Breakdown Voltage	Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	V_{G2S} = V_{DS} = 0	6.5	–	13	V
	Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} = V_{DS} = 0				
* Gate-to-Source Reverse Breakdown Voltage	Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	V_{G2S} = V_{DS} = 0	-6.5	–	-13	V
	Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} = V_{DS} = 0				

†Capacitance between Gate No. 1 and all other terminals.
♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.
*In accordance with JEDEC registration data format (JS-9 RDF-19A)

OPERATING CONSIDERATIONS

The flexible leads of the 3N200 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.



All resistances in ohms
All capacitances in pF

C_1, C_2: 1.3-5.4 pF variable air capacitor: Hammerland Mac 5 type or equivalent

C_3: 1.9-13.8 pF variable air capacitor: Hammerland Mac 15 type or equivalent

C_4: Approx. 300 pF - capacitance formed between socket cover & chassis

C_5: 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent

L_1, L_2: Inductance to tune circuit

Fig. 1 - 400 MHz power gain and noise figure test circuit

3N200

Typical Characteristics

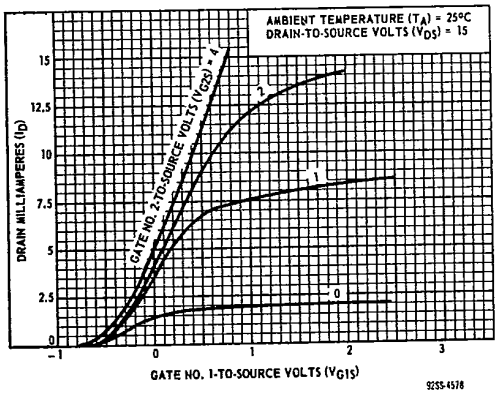


Fig. 2-I_D vs. V_{G1S}

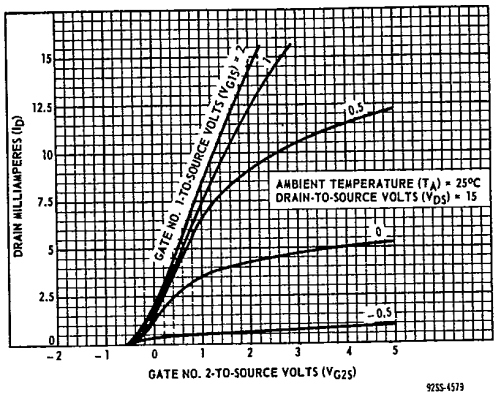


Fig. 3-I_D vs. V_{G2S}

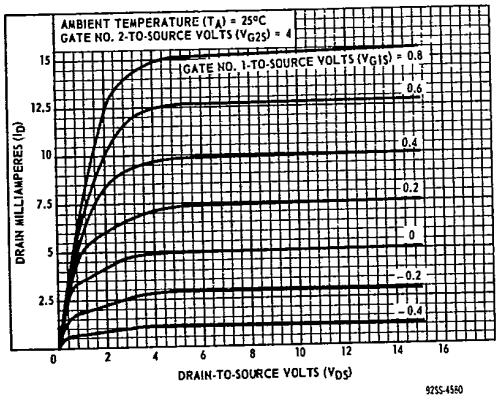


Fig. 4-I_D vs. V_{DS}

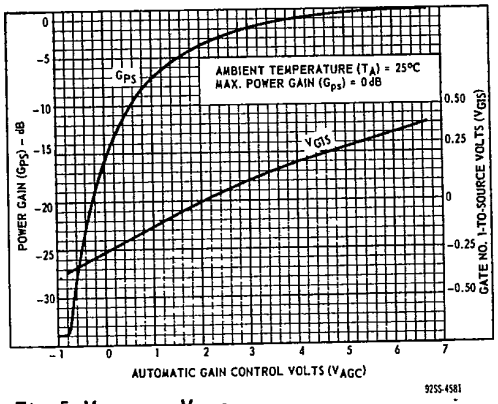


Fig. 5-V_{AGC} vs. V_{G1S}

y and s Parameters vs. Frequency

TEST CONDITIONS: Drain-to-Source Volts (V_{DS}) = 15, Drain Milliamperes (I_D) = 10, Gate No. 2-to-Source Volts (V_{G2S}) = 4

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz)					UNITS
		100	200	300	400	500	
Maximum Available Power Gain	MAG	32	24	17.5	13	10	dB
Maximum Usable Power Gain (Unneutralized)*	MUG	32	24	17.5	13	10	dB
Y Parameters							
Input Conductance	g_{is}	0.25	0.8	2.0	3.6	6.2	mmho
Input Susceptance	b_{is}	3.4	5.8	8.5	11.2	15.5	mmho
Magnitude of Forward Transadmittance	$\|y_{fs}\|$	15.3	15.3	15.4	15.5	16.3	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	−15	−25	−35	−47	−60	degrees
Output Conductance	g_{os}	0.15	0.3	0.5	0.8	1.1	mmho
Output Susceptance	b_{os}	1.5	2.7	3.6	4.25	5.0	mmho
Magnitude of Reverse Transadmittance	$\|y_{rs}\|$	0.012	0.025	0.06	0.14	0.26	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	−60	−25	0	14	20	degrees
S Parameters							
Magnitude of Input Reflection Coeff.	$\|s_{is}\|$	0.97	0.90	0.84	0.78	0.70	
Angle of Input Reflection Coeff.	$\angle s_{is}$	−20	−32	−55	−68	−82	degrees
Magnitude of Forward Transmission Coeff.	$\|s_{fs}\|$	1.50	1.40	1.25	1.1	0.9	
Angle of Forward Transmission Coeff.	$\angle s_{fs}$	153	133	112	90	70	degrees
Mangitude of Output Reflection Coeff.	$\|s_{os}\|$	0.985	0.95	0.93	0.92	0.91	
Angle of Output Reflection Coeff.	$\angle s_{os}$	−7.5	−16	−22	−28	−34	degrees
Magnitude of Reverse Transmission Coeff.	$\|s_{rs}\|$	0.001	0.0025	0.005	0.010	0.0165	
Angle of Reverse Transmission Coeff.	$\angle s_{rs}$	100	125	141	150	142	degrees

*Limited only by practical design considerations

Typical y Parameters vs. V_{DS}

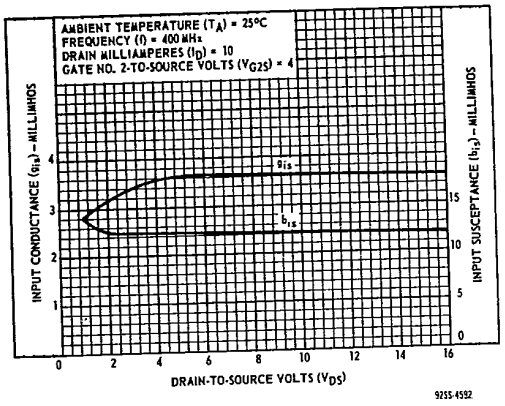


Fig. 6 - y_{is} vs. V_{DS}

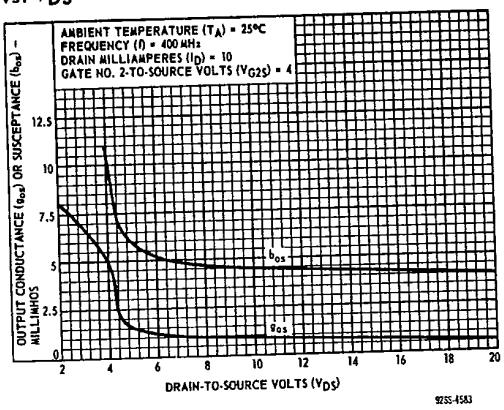


Fig. 7 - y_{os} vs. V_{DS}

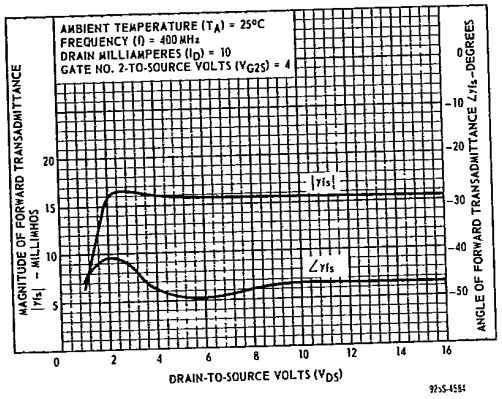


Fig. 8 - y_{fs} vs. V_{DS}

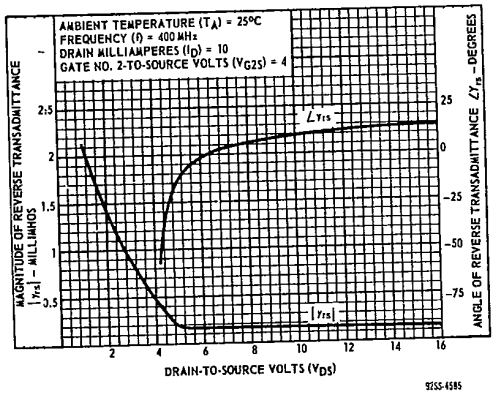


Fig. 9 - y_{rs} vs. V_{DS}

Typical y Parameters vs I_D

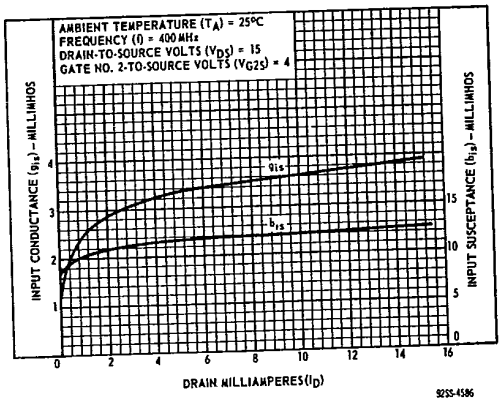


Fig. 10 - y_{is} vs. I_D

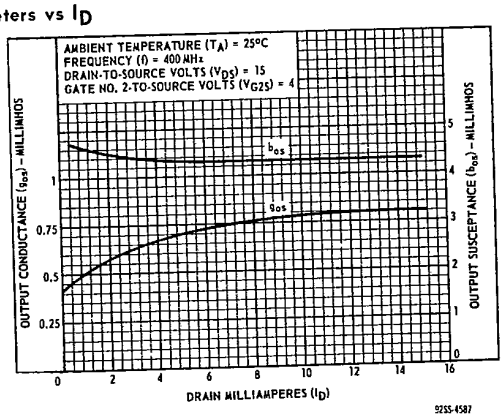


Fig. 11 - y_{os} vs. I_D

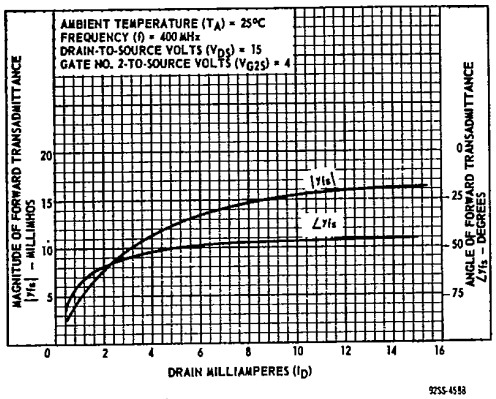


Fig. 12 - y_{fs} vs. I_D

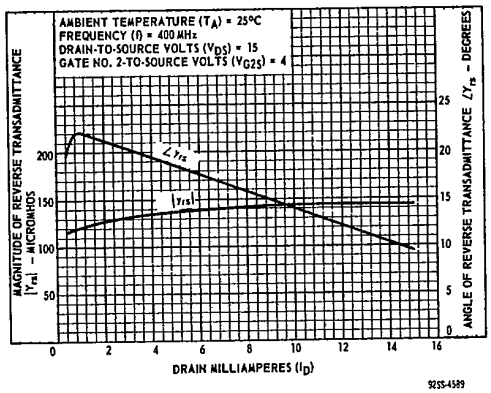


Fig. 13 - y_{rs} vs. I_D

Typical y Parameters vs. V_{G2S}

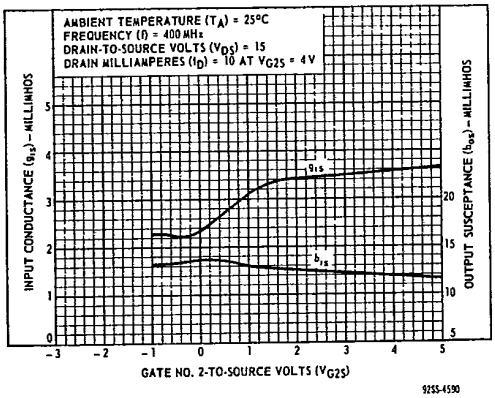


Fig. 14 - y_{is} vs. V_{G2S}

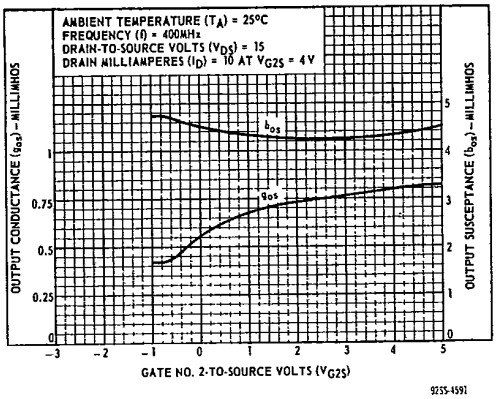


Fig. 15 - y_{os} vs. V_{G2S}

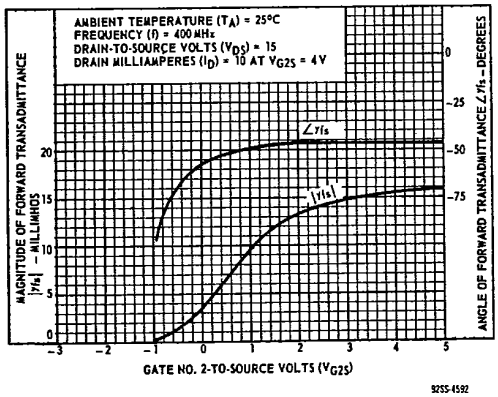


Fig. 16 - y_{fs} vs. V_{G2S}

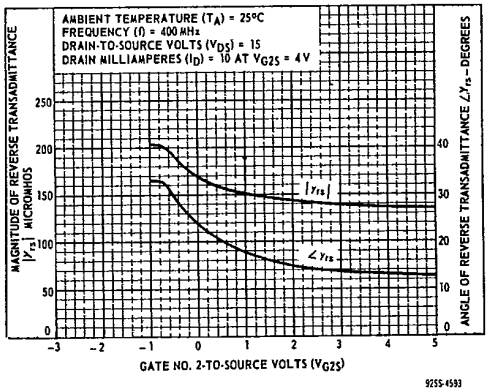


Fig. 17 - y_{rs} vs. V_{G2S}

3N200

Typical Characteristics

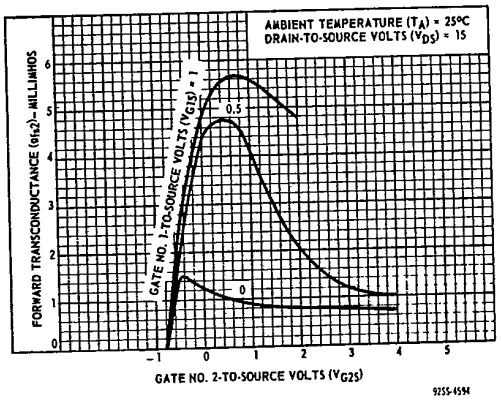


Fig. 18 - g_{fs2} vs. V_{G2S}

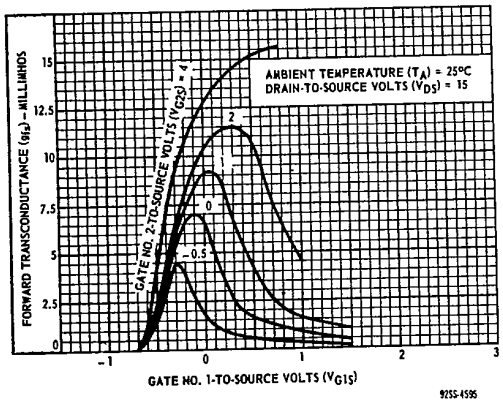


Fig. 19 - g_{fs} vs. V_{G1S}

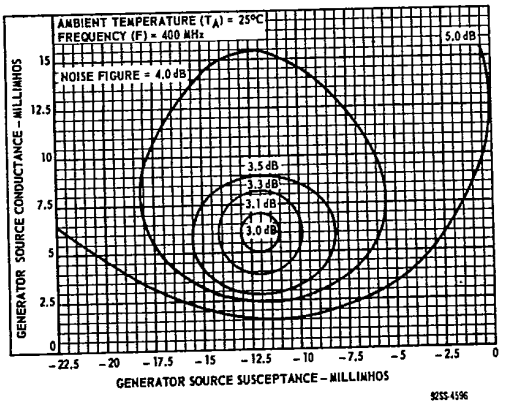
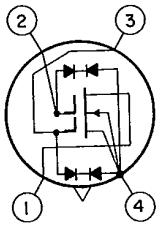


Fig. 20 - Noise figure vs. generator source admittance

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE