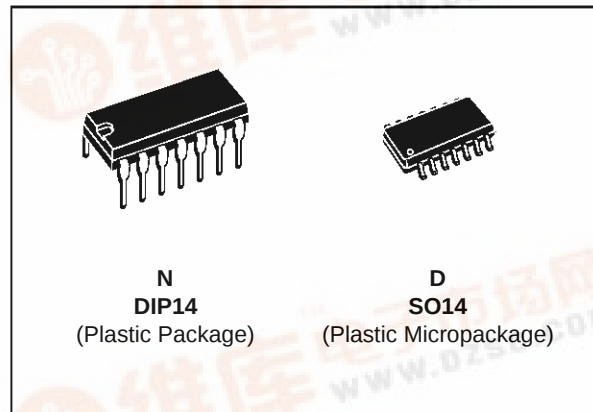




TS3V914

3V RAIL TO RAIL CMOS QUAD OPERATIONAL AMPLIFIER

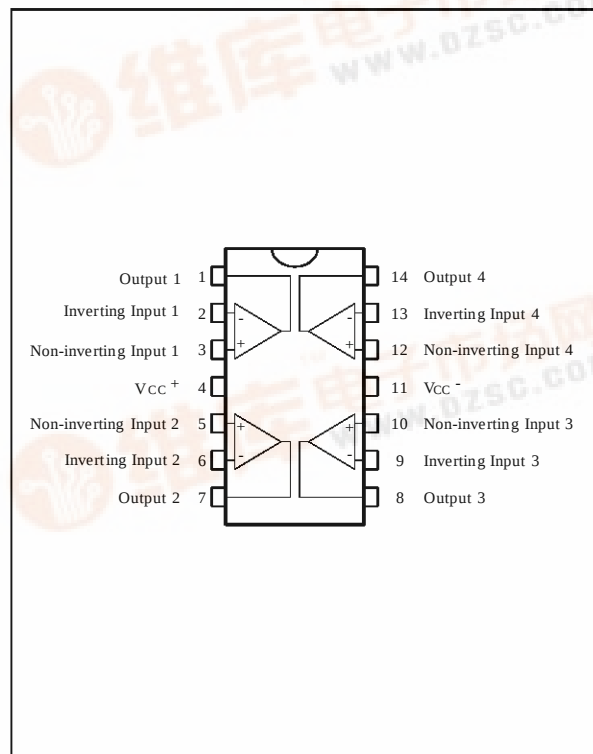
- DEDICATED TO 3.3V APPLICATIONS AND BATTERY-SUPPLIED (fully specified at $V_{CC} = 3V$ and $5V$)
- **RAIL TO RAIL** INPUT AND OUTPUT VOLTAGE RANGES
- SINGLE (OR DUAL) SUPPLY OPERATION FROM **2.7V TO 16V**
- EXTREMELY LOW INPUT BIAS CURRENT : **1pA** TYP
- LOW INPUT OFFSET VOLTAGE : 5mV max.
- SPECIFIED FOR **600Ω** AND **100Ω** LOADS
- LOW SUPPLY CURRENT : 200μA/Ampli
- **SPICE MACROMODEL** INCLUDED IN THIS SPECIFICATION



ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V914I/AI	-40, +125°C	•	•

PIN CONNECTIONS (top view)



DESCRIPTION

The TS3V914 is a RAIL TO RAIL quad CMOS operational amplifier designed to operate with a single 3V supply voltage.

The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^- .

The output reaches :

- $V_{CC}^- + 50mV$ $V_{CC}^+ - 50mV$ with $R_L = 10k\Omega$
- $V_{CC}^- + 350mV$ $V_{CC}^+ - 350mV$ with $R_L = 600\Omega$

This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 200μA/amp. ($V_{CC} = 3V$).

Source and sink output current capability is typically 40mA (at $V_{CC} = 3V$), fixed by an internal limitation circuit.

SGS-THOMSON is offering a dual op-amp with the same features : TS3V912.

SCHEMATIC DIAGRAM (1/4 TS3V914)



Notes :

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC} , +0.3V.

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2.7 to 16	V
V _{icm}	Common Mode Input Voltage Range	V _{CC} ⁻ -0.2 to V _{CC} ⁺ +0.2	V

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L, C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	TS3V914I/AI			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($V_{ic} = V_o = V_{CC}/2$) $T_{min.} \leq T_{amb} \leq T_{max.}$			10 5 12 7	mV
DV_{io}	Input Offset Voltage Drift		5		$\mu V/^\circ C$
I_{io}	Input Offset Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1	100 200	pA
I_{ib}	Input Bias Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1	150 300	pA
I_{CC}	Supply Current (per amplifier, $A_{VCL} = 1$, no load) $T_{min.} \leq T_{amb} \leq T_{max.}$		200	300 400	μA
CMR	Common Mode Rejection Ratio $V_{ic} = 0$ to $3V$, $V_o = 1.5V$		70		dB
SVR	Supply Voltage Rejection Ratio ($V_{CC}^+ = 2.7$ to $3.3V$, $V_o = V_{CC}/2$)	40	70		dB
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_o = 1.2V$ to $1.8V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	3 2	10		V/mV
V_{OH}	High Level Output Voltage ($V_{id} = 1V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 10k\Omega$ 2.9 $R_L = 600\Omega$ 2.3 $R_L = 100\Omega$	2.96 2.6 2		V
V_{OL}	Low Level Output Voltage ($V_{id} = -1V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$	50 300 900	100 400	mV
I_o	Output Short Circuit Current ($V_{id} = \pm 1V$) Source ($V_o = V_{CC}^-$) Sink ($V_o = V_{CC}^+$)		40 40		mA
GBP	Gain Bandwidth Product ($A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$)		0.8		MHz
SR^+	Positive Slew Rate $A_{VCL} = 1$, $R_L = 10k\Omega$, $V_i = 1.3V$ to $1.7V$, $C_L = 100pF$		0.5		V/ μs
SR^-	Negative Slew Rate		0.4		V/ μs
ϕ_m	Phase Margin		30		Degrees
e_n	Equivalent Input Noise Voltage ($R_s = 100\Omega$, $f = 1kHz$)		30		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation ($f = 1kHz$)		120		dB

Note 1 : Maximum values including unavoidable inaccuracies of the industrial test.

TS3V914

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, R_L, C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	TS3V914I/AI			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($V_{ic} = V_o = V_{CC}/2$) $T_{min.} \leq T_{amb} \leq T_{max.}$			10 5 12 7	mV
DV_{io}	Input Offset Voltage Drift		5		$\mu V/^\circ C$
I_{io}	Input Offset Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1	100 200	pA
I_{ib}	Input Bias Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1	150 300	pA
I_{CC}	Supply Current (per amplifier, $A_{VCL} = 1$, no load) $T_{min.} \leq T_{amb} \leq T_{max.}$		230	350 450	μA
CMR	Common Mode Rejection Ratio $V_{ic} = 1.5$ to $3.5V$, $V_o = 2.5V$	50	75		dB
SVR	Supply Voltage Rejection Ratio ($V_{CC}^+ = 3$ to $5V$, $V_o = V_{CC}/2$)	50	80		dB
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_o = 1.5V$ to $3.5V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	10 7	30		V/mV
V_{OH}	High Level Output Voltage ($V_{id} = 1V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 10k\Omega$ 4.90 $R_L = 600\Omega$ 4.25 $R_L = 100\Omega$	4.95 4.65 3.7		V
V_{OL}	Low Level Output Voltage ($V_{id} = -1V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$	50 350 1400	100 500	mV
I_o	Output Short Circuit Current ($V_{id} = \pm 1V$) Source ($V_o = V_{CC}^-$) Sink ($V_o = V_{CC}^+$)	45 45	60 60		mA
GBP	Gain Bandwidth Product ($A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$)		0.9		MHz
SR^+	Positive Slew Rate $A_{VCL} = 1$, $R_L = 10k\Omega$, $V_i = 1V$ to $4V$, $C_L = 100pF$		0.8		V/ μs
SR^-	Negative Slew Rate		0.5		V/ μs
ϕ_m	Phase Margin		30		Degrees

Note 1 : Maximum values including unavoidable inaccuracies of the industrial test.

TYPICAL CHARACTERISTICS

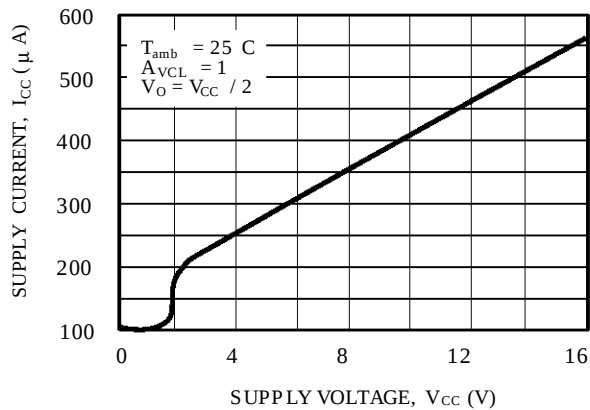
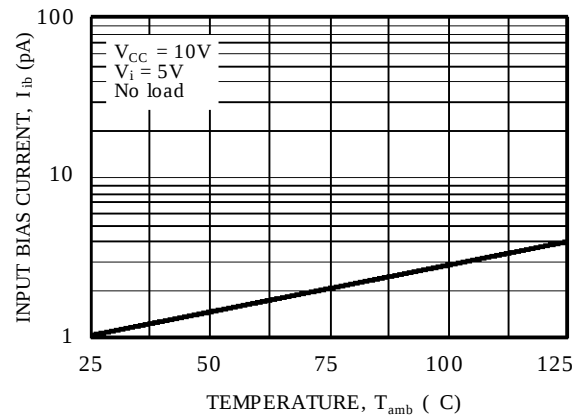
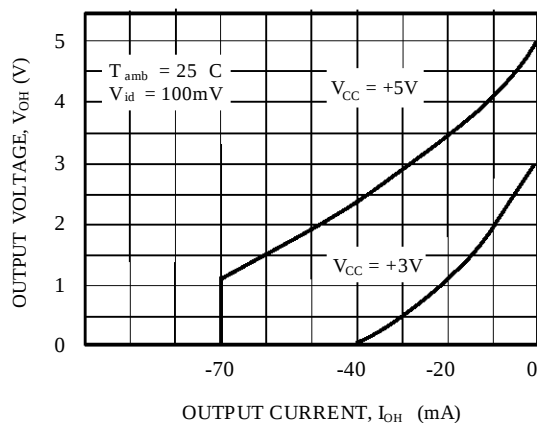
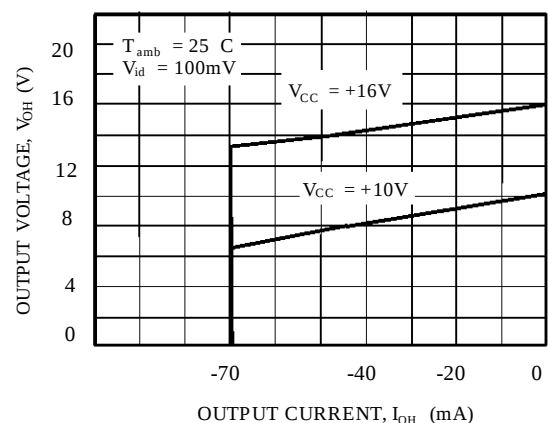
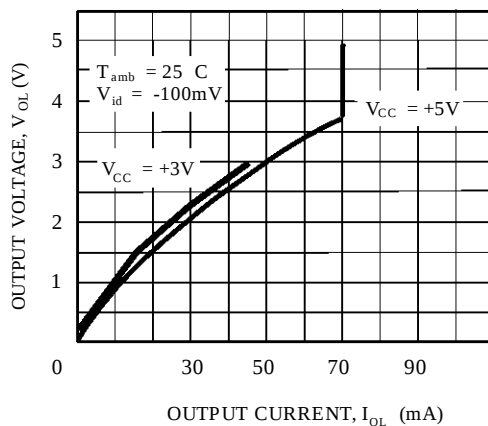
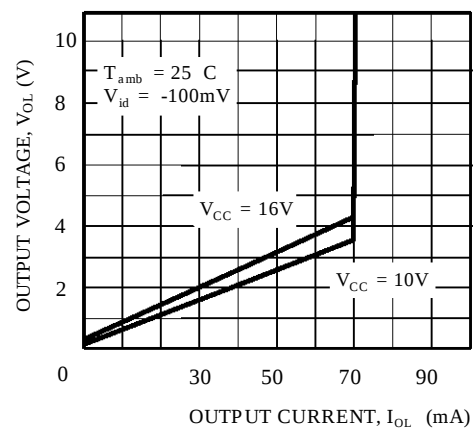
Figure 1 : Supply Current (each amplifier) versus Supply Voltage**Figure 2 :** Input Bias Current versus Temperature**Figure 3a :** High Level Output Voltage versus High Level Output Current**Figure 3b :** High Level Output Voltage versus High Level Output Current**Figure 4a :** Low Level Output Voltage versus Low Level Output Current**Figure 4b :** Low Level Output Voltage versus Low Level Output Current

Figure 5a : Open Loop Frequency Response and Phase Shift

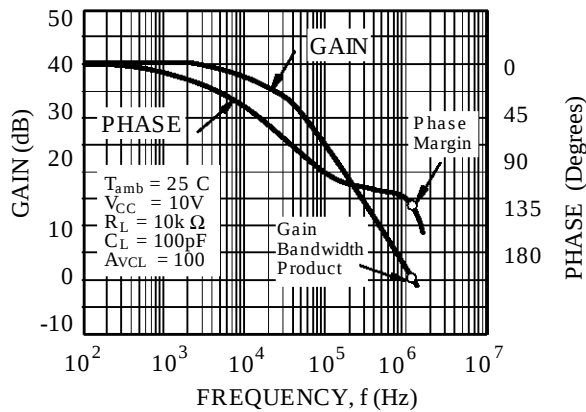


Figure 5b : Open Loop Frequency Response and Phase Shift

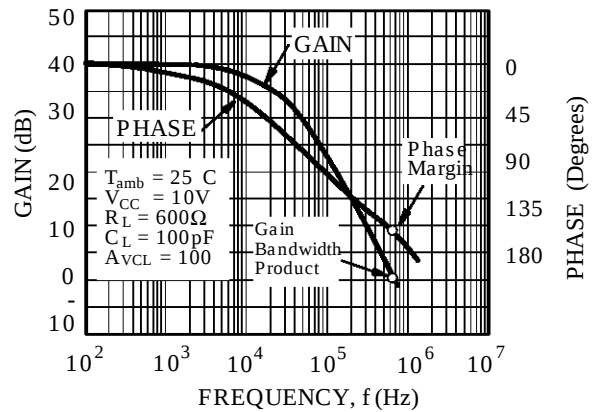


Figure 6a : Gain Bandwidth Product versus Supply Voltage

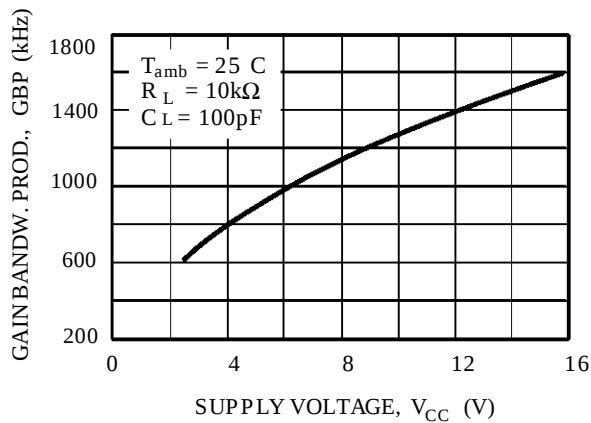


Figure 6b : Gain bandwidth Product versus Supply Voltage

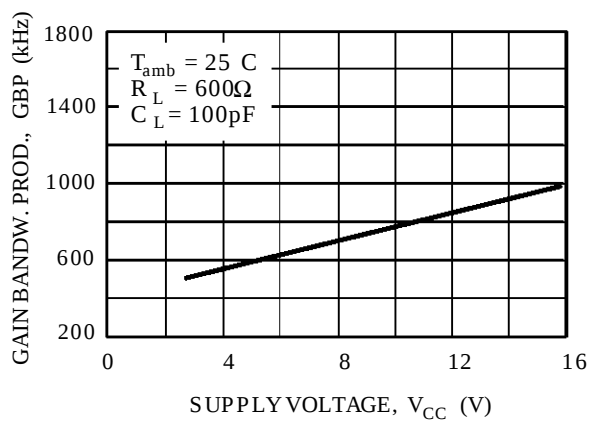


Figure 7a : Phase Margin versus Supply Voltage

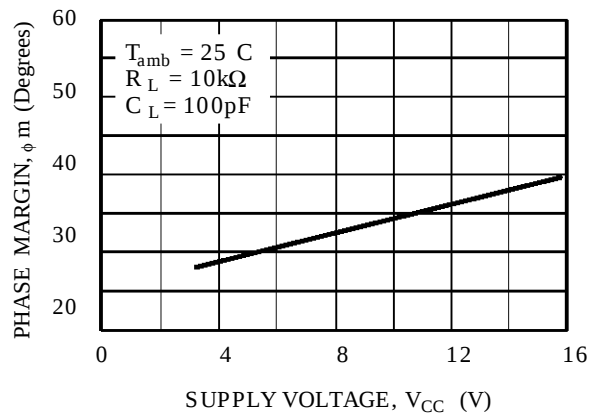


Figure 7b : Phase Margin versus Supply Voltage

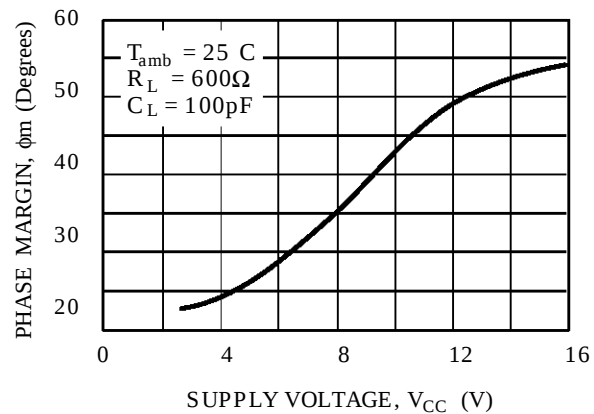
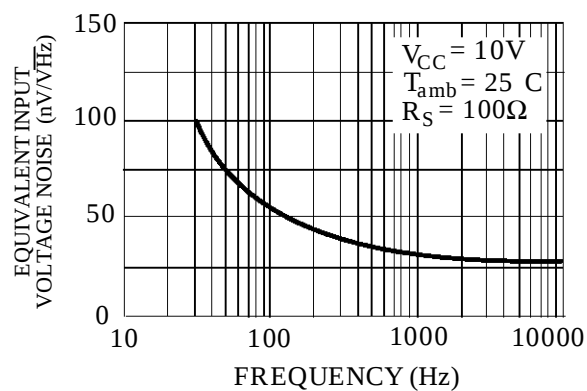
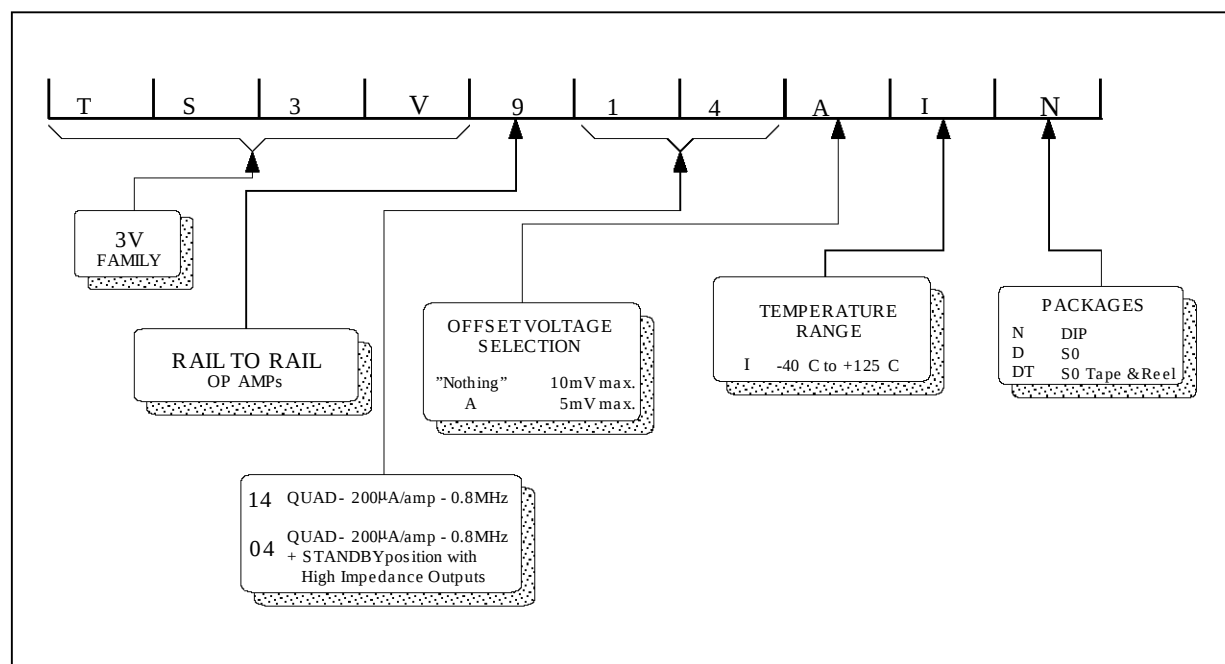


Figure 8 : Input Voltage Noise versus Frequency**ORDERING INFORMATION**

TS3V914

MACROMODEL

- RAIL TO RAIL INPUT AND OUTPUT VOLTAGE RANGES
- **STANDBY POSITION : REDUCED CONSUMPTION (1 μ A) AND HIGH IMPEDANCE OUTPUTS**
- SINGLE (OR DUAL) SUPPLY OPERATION FROM **2.7V TO 16V** ($\pm 1.35V$ to $\pm 8V$)
- EXTREMELY LOW INPUT BIAS CURRENT : **1pA TYP**
- LOW INPUT OFFSET VOLTAGE : **1.5mV max.**
- SPECIFIED FOR **600 Ω** AND **100 Ω** LOADS
- LOW SUPPLY CURRENT : 400 μ A/Ampli
- SPEED : 1.3MHz - 1.3V/ μ s

Applies to : TS3V914I,AI,BI

** Standard Linear Ics Macromodels, 1993.

** CONNECTIONS :

* 1 INVERTING INPUT

* 2 NON-INVERTING INPUT

* 3 OUTPUT

* 4 POSITIVE POWER SUPPLY

* 5 NEGATIVE POWER SUPPLY

.SUBCKT TS3V914_3 1 3 2 4 5 (analog)

.MODEL MDTH D IS=1E-8 KF=6.564344E-14 CJO=10F

* INPUT STAGE

CIP 2 5 1.000000E-12

CIN 1 5 1.000000E-12

EIP 10 5 2 5 1

EIN 16 5 1 5 1

RIP 10 11 6.500000E+00

RIN 15 16 6.500000E+00

RIS 11 15 1.271505E+01

DIP 11 12 MDTH 400E-12

DIN 15 14 MDTH 400E-12

VOFP 12 13 DC 0.000000E+00

VOFN 13 14 DC 0

IPOL 13 5 4.000000E-05

CPS 11 15 2.125860E-08

DINN 17 13 MDTH 400E-12

VIN 17 5 0.000000E+00

DINR 15 18 MDTH 400E-12

VIP 4 18 0.000000E+00

FCP 4 5 VOFP 5.000000E+00

FCN 5 4 VOFN 5.000000E+00

* AMPLIFYING STAGE

FIP 5 19 VOFP 2.750000E+02

FIN 5 19 VOFN 2.750000E+02

RG1 19 5 1.916825E+05

RG2 19 4 1.916825E+05

CC 19 29 2.200000E-08

HZTP 30 29 VOFP 1.3E+03

HZTN 5 30 VOFN 1.3E+03

DOPM 19 22 MDTH 400E-12

DONM 21 19 MDTH 400E-12

HOPM 22 28 VOUT 3800

VIPM 28 4 150

HONM 21 27 VOUT 3800

VINM 5 27 150

EOUT 26 23 19 5 1

VOUT 23 5 0

ROUT 26 3 75

COU 3 5 1.000000E-12

DOP 19 68 MDTH 400E-12

VOP 4 25 1.724

HSCP 68 25 VSCP1 0.8E8

DON 69 19 MDTH 400E-12

VON 24 5 1.7419107

HSCN 24 69 VSCN1 0.8E+08

VSCTHP 60 61 0.0875

** VSCTHP = le seuil au dessus de vio

* 500

** c.a.d 275U-000U dus a l'offset

DSCP1 61 63 MDTH 400E-12

VSCP1 63 64 0

ISCP 64 0 1.000000E-8

DSCP2 0 64 MDTH 400E-12

DSCN2 0 74 MDTH 400E-12

ISCN 74 0 1.000000E-8

VSCN1 73 74 0

DSCN1 71 73 MDTH 400E-12

VSCTHN 71 70 -0.55

** VSCTHN = le seuil au dessous de vio

* 2000

** c.a.d -375U-000U dus a l'offset

ESCP 60 0 2 1 500

ESCN 70 0 2 1 -2000

.ENDS

Applies to : TS3V914I,AI,BI

** Standard Linear Ics Macromodels, 1993.

** CONNECTIONS :

* 1 INVERTING INPUT

* 2 NON-INVERTING INPUT

* 3 OUTPUT

* 4 POSITIVE POWER SUPPLY

* 5 NEGATIVE POWER SUPPLY

* 6 STANDBY

.SUBCKT TS3V914_5 1 3 2 4 5 (analog)

.MODEL MDTH D IS=1E-8 KF=6.564344E-14 CJO=10F

* INPUT STAGE

CIP 2 5 1.000000E-12

CIN 1 5 1.000000E-12

EIP 10 5 2 5 1

EIN 16 5 1 5 1

RIP 10 11 6.500000E+00

RIN 15 16 6.500000E+00

RIS 11 15 7.322092E+00

DIP 11 12 MDTH 400E-12

DIN 15 14 MDTH 400E-12

VOFP 12 13 DC 0.000000E+00

VOFN 13 14 DC 0

IPOL 13 5 4.000000E-05

CPS 11 15 2.498970E-08

DINN 17 13 MDTH 400E-12

VIN 17 5 0.000000E+00

DINR 15 18 MDTH 400E-12

VIP 4 18 0.000000E+00

FCP 4 5 VOFP 5.750000E+00

FCN 5 4 VOFN 5.750000E+00

ISTB0 5 4 500N

* AMPLIFYING STAGE

FIP 5 19 VOFP 4.400000E+02

FIN 5 19 VOFN 4.400000E+02

RG1 19 5 4.904961E+05

RG2 19 4 4.904961E+05

CC 19 29 2.200000E-08

HZTP 30 29 VOFP 1.8E+03

HZTN 5 30 VOFN 1.8E+03

DOPM 19 22 MDTH 400E-12

DONM 21 19 MDTH 400E-12

HOPM 22 28 VOUT 3800

VIPM 28 4 230

HONM 21 27 VOUT 3800

VINM 5 27 230

EOUT 26 23 19 5 1

VOUT 23 5 0

ROUT 26 3 82

COUT 3 5 1.000000E-12

DOP 19 68 MDTH 400E-12

VOP 4 25 1.724

HSCP 68 25

VSCP1 0.8E+08

DON 69 19 MDTH 400E-12

VON 24 5 1.7419107

HSCN 24 69

VSCN1 0.8E+08

VSCTHP 60 61 0.0875

** VSCTHP = le seuil au dessus de vio

* 500

** c.a.d 275U-000U dus a l'offset

DSCP1 61 63 MDTH 400E-12

VSCP1 63 64 0

ISCP 64 0 1.000000E-8

DSCP2 0 64 MDTH 400E-12

DSCN2 0 74 MDTH 400E-12

ISCN 74 0 1.000000E-8

VSCN1 73 74 0

DSCN1 71 73 MDTH 400E-12

VSCTHN 71 70 -0.55

** VSCTHN = le seuil au dessous de vio

* 2000

** c.a.d -375U-000U dus a l'offset

ESCP 60 0 2 1 500

ESCN 70 0 2 1 -2000

.ENDS

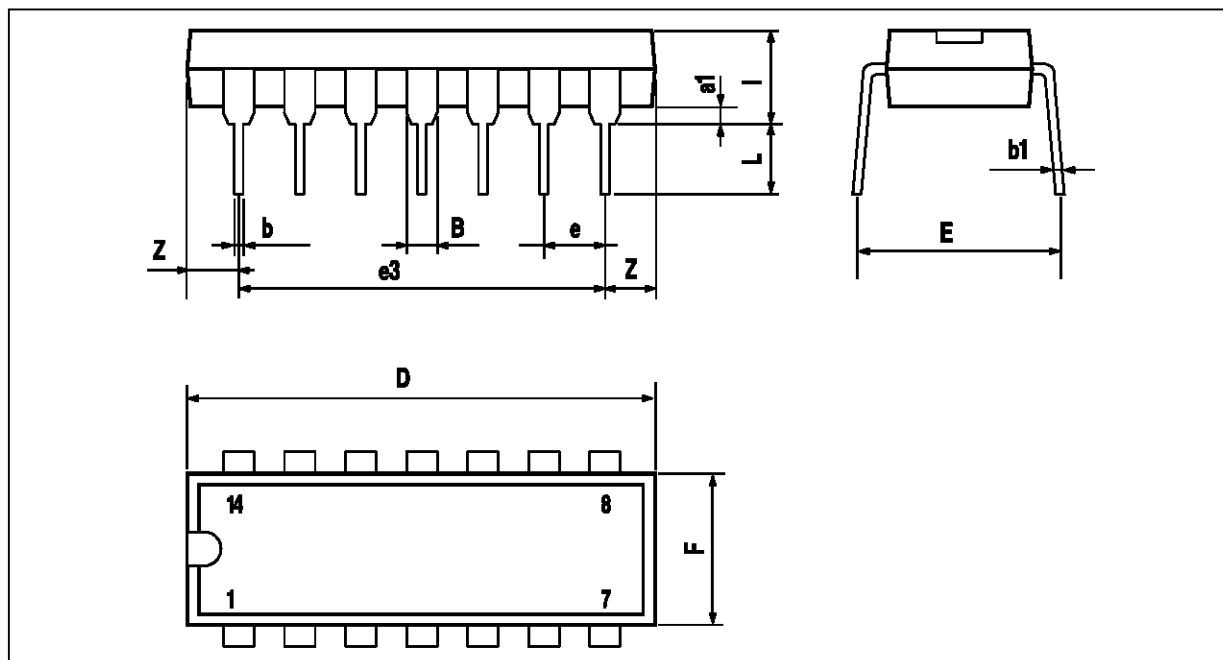
ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L, C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$
(unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	$R_L = 10k\Omega$	10	V/mV
I_{CC}	No load, per operator	100	μA
V_{icm}		-0.2 to 3.2	V
V_{OH}	$R_L = 600\Omega$	2.6	V
V_{OL}	$R_L = 600\Omega$	300	mV
I_{sink}	$V_O = 3V$	40	mA
I_{source}	$V_O = 0V$	40	mA
GBP	$R_L = 10k\Omega$, $C_L = 100pF$, $F = 100kHz$	0.8	MHz
SR	$R_L = 10k\Omega$, $C_L = 100pF$	0.5	V/ μs
$\varnothing m$		30	Degrees

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP



PM-DIP14.EPS

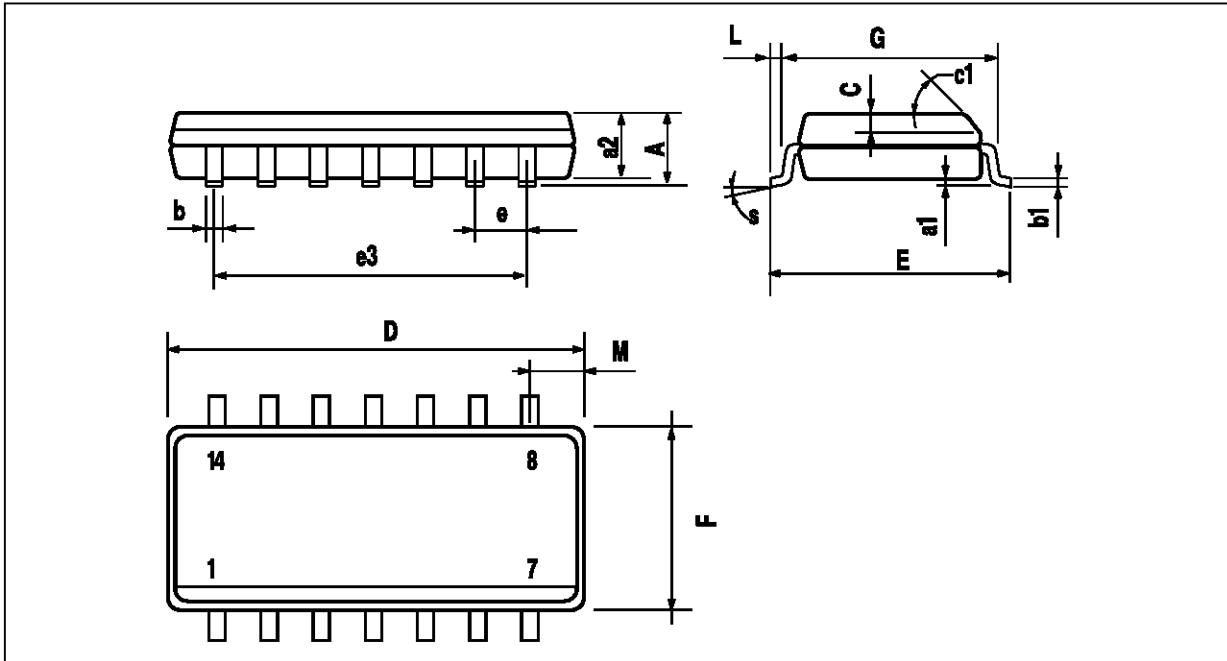
Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

DIP14.TBL

TS3V914

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC MICROPACKAGE (SO)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.334
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

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