# 4008B
## 4-BIT BINARY FULL ADDER

**DESCRIPTION** — The 4008B is a 4-Bit Binary Full Adder with two 4-bit Data Inputs ($A_0$–$A_3$, $B_0$–$B_3$); a Carry Input ($C_0$), four Sum Outputs ($S_0$-$S_3$) and a Carry Output ($C_4$).

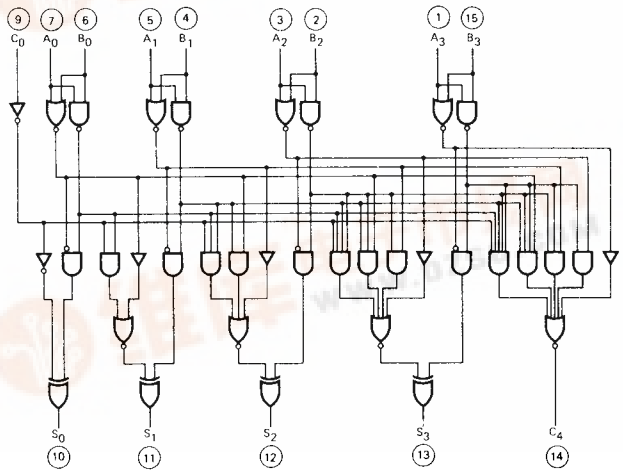
The 4008B uses full lookahead across 4-bits to generate the Carry Output ($C_4$). This minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

- **CARRY LOOKAHEAD BUFFERED OUTPUT**
- **EASILY CASCADED**

**PIN NAMES**

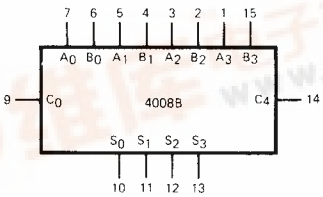
| | |
|---|---|
| $A_0$-$A_3$, $B_0$-$B_3$ | Data Inputs |
| $C_0$ | Carry Input |
| $S_0$-$S_3$ | Sum Outputs |
| $C_4$ | Carry Output |

**LOGIC DIAGRAM**



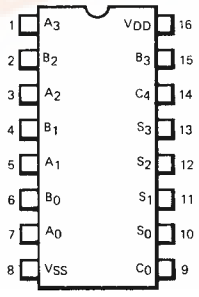

$V_{DD}$ = Pin 16
$V_{SS}$ = Pin 8
○ = Pin Number

**LOGIC SYMBOL**




$V_{DD}$ = Pin 16
$V_{SS}$ = Pin 8

**CONNECTION DIAGRAM**
**DIP** (TOP VIEW)




NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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**DC CHARACTERISTICS:** $V_{DD}$ as shown, $V_{SS}$ = 0 V (See Note 1)

| SYMBOL | PARAMETER | | LIMITS | | | | | | | | | UNITS | TEMP | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ = 5 V | | | $V_{DD}$ = 10 V | | | $V_{DD}$ = 15 V | | | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| $I_{DD}$ | Quiescent Power Supply Current | XC | | | 20 | | | 40 | | | 80 | μA | MIN, 25°C | All inputs at 0 V or $V_{DD}$ |
| | | | | | 100 | | | 300 | | | 600 | | MAX | |
| | | XM | | | 5 | | | 10 | | | 20 | μA | MIN, 25°C | |
| | | | | | 150 | | | 300 | | | 600 | | MAX | |

**AC CHARACTERISTICS AND SET-UP REQUIREMENTS:** $V_{DD}$ as shown, $V_{SS}$ = 0 V, $T_A$ = 25°C (see Note 2)

| SYMBOL | PARAMETER | LIMITS | | | | | | | | | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ = 5 V | | | $V_{DD}$ = 10 V | | | $V_{DD}$ = 15 V | | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| $t_{PLH}$ | Propagation Delay, $A_n$, $B_n$ to $S_n$ | | 150 | 300 | | 60 | 140 | | 50 | 110 | ns | $C_L$ = 50 pF, $R_L$ = 200 kΩ, Input Transition Times ≤ 20 ns |
| $t_{PHL}$ | | | 150 | 300 | | 60 | 140 | | 50 | 110 | ns | |
| $t_{PLH}$ | Propagation Delay, $A_n$, $B_n$ to $C_4$ | | 138 | 275 | | 63 | 130 | | 50 | 100 | ns | |
| $t_{PHL}$ | | | 138 | 275 | | 63 | 130 | | 50 | 100 | ns | |
| $t_{PLH}$ | Propagation Delay, $C_o$ to $S_n$ | | 115 | 250 | | 69 | 115 | | 52 | 90 | ns | |
| $t_{PHL}$ | | | 123 | 250 | | 69 | 115 | | 52 | 90 | ns | |
| $t_{PLH}$ | Propagation Delay, $C_o$ to $C_4$ | | 72 | 200 | | 28 | 95 | | 23 | 75 | ns | |
| $t_{PHL}$ | | | 95 | 200 | | 28 | 95 | | 23 | 75 | ns | |
| $t_{TLH}$ | Output Transition Time | | 60 | 135 | | 30 | 75 | | 20 | 45 | ns | |
| $t_{THL}$ | | | 60 | 135 | | 30 | 75 | | 20 | 45 | ns | |

NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

## APPLICATION

### A 2-DIGIT BCD TO 7-BIT BINARY DECODER USING THE 4008B