TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS257

January 1997

CD74FCT540, CD74FCT541

BiCMOS FCT Interface Logic, Octal Buffers/Line Drivers, Three-State

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 6.4ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- CD74FCT540
  - Inverting
- CD74FCT541
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 64mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT540 and CD74FCT541 octal buffers/line drivers use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 milliamperes.

The CD74FCT540 is a three-state buffer having two active LOW output enables. The CD74FCT541 is a noninverting three state buffer having two active LOW output enables.

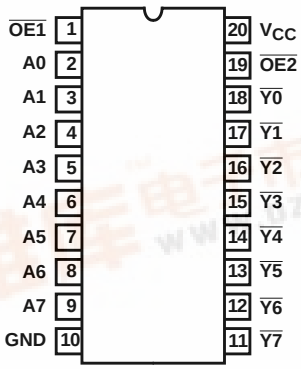
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT540E	0 to 70	20 Ld PDIP	E20.3
CD74FCT541E	0 to 70	20 Ld PDIP	E20.3
CD74FCT540M	0 to 70	20 Ld SOIC	M20.3
CD74FCT541M	0 to 70	20 Ld SOIC	M20.3
CD74FCT541SM	0 to 70	20 Ld SSOP	M20.209

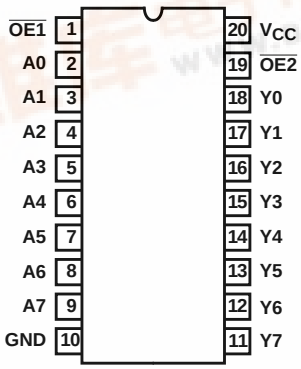
NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

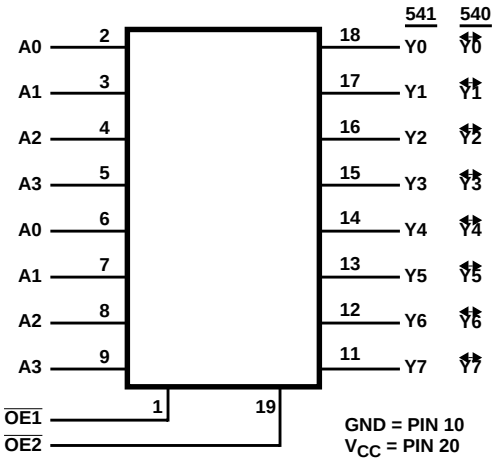
CD74FCT540
(PDIP, SOIC)
TOP VIEW



CD74FCT541
(PDIP, SOIC, SSOP)
TOP VIEW



Functional Diagram



TRUTH TABLE (Note 1)

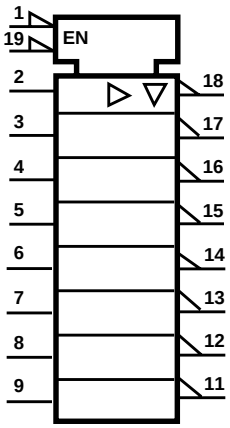
INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	A_n	CD74FCT540	CD74FCT541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

NOTE:

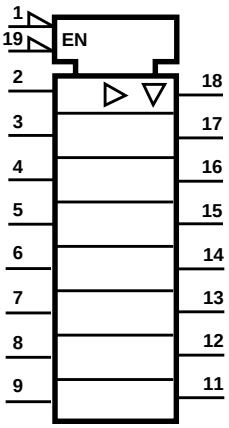
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Immaterial
   Z = HIGH Impedance

IEC Logic Symbol

CD74FCT540



CD74FCT541



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Operating Conditions

Operating Temperature Range (T_A) . . . . . 0^oC to 70^oC
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} ($^oC/W$)
PDIP Package 135
SOIC Package 125
SSOP Package 130
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC and SSOP-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Commercial Temperature Range 0^oC to 70^oC, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V (Note 5)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25^oC		0^oC TO 70^oC		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max. @ 70^oC.

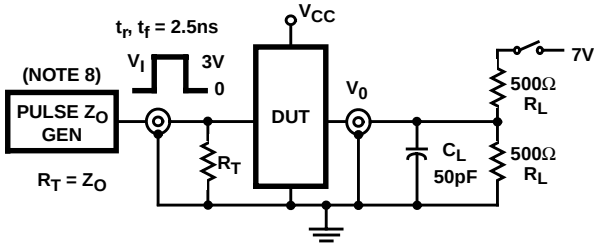
Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 3) (Note 6)

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays		(Note 6)				
Data to Outputs						
CD74FCT540	t_{PLH}, t_{PHL}	5	6.4	2	8.5	ns
CD74FCT541	t_{PLH}, t_{PHL}	5	6	2	8	ns
Output Disable to Output	t_{PLZ}, t_{PHZ}	5	7.1	2	9.5	ns
Output Enable to Output	t_{PZL}, t_{PZH}	5	7.5	2	10	ns
Power Dissipation Capacitance	C_{PD} (Note 7)					
CD74FCT540		-	37	-	-	pF
CD74FCT541		-	40	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	15	pF

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = $V_{CC}\ I_{CC} + \Sigma(V_{CC}^2\ f_I\ C_{PD} + V_O^2\ f_O\ C_L + V_{CC}\ \Delta I_{CC}\ D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

Test Circuits and Waveforms



NOTE:

8. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: t_r = t_f = 2.5ns (10% to 90%), unless otherwise specified

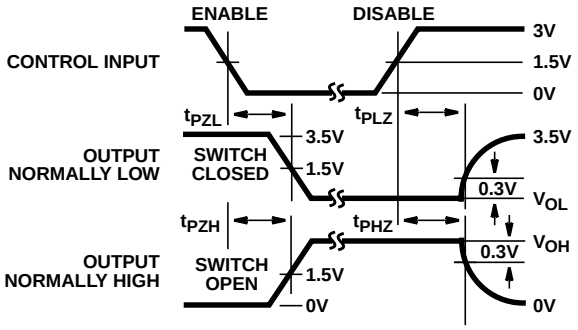


FIGURE 2. ENABLE AND DISABLE TIMING

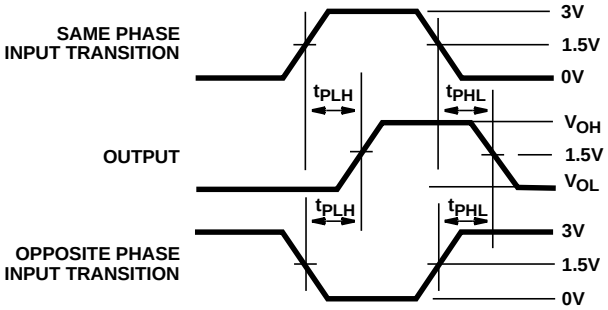
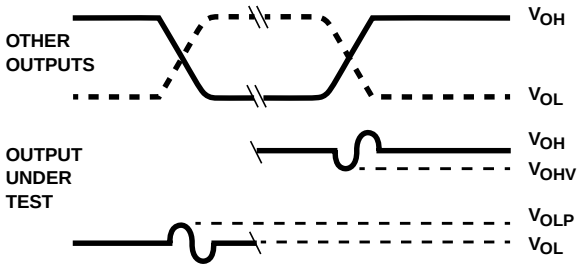


FIGURE 3. PROPAGATION DELAY



NOTES:

9. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
10. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
11. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 4. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

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