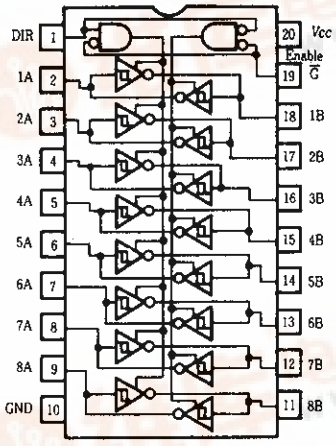
HD74LS642-1 ●Octal Bus Transceivers (inverted open-collector outputs)

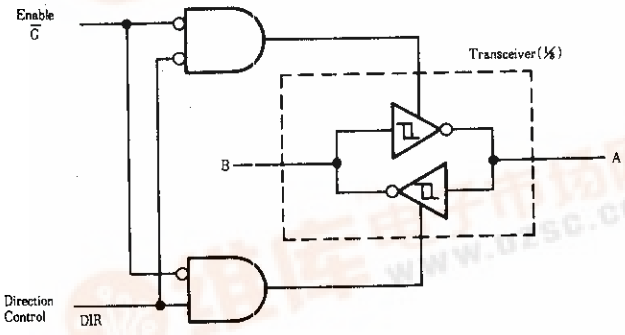
This octal bus transceiver is designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	unit
Output current	V_{CC}	4.75	5.00	5.25	V
Output voltage	V_{OH}	—	—	5.5	V
Output current	I_{OL}	—	—	48	mA
Operating temperature range	T_{opr}	−20	25	75	℃

■FUNCTION TABLE

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

H; high level,
L; low level,
X; irrelevant

HD74LS642-1

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	—	—	V
		V_{IL}			—	—	0.8	
Hysteresis		$V_T^+ - V_T^-$	$V_{CC}=4.75V$		0.2	—	—	V
Output current		I_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$		—	—	100	μA
Output voltage		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=12mA$	—	—	0.4	V
				$I_{OL}=24mA$	—	—	0.5	
				$I_{OL}=48mA$	—	—	0.5	
Input current		I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		—	—	20	μA
		I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		—	—	−400	μA
	A or B	I_I	$V_{CC}=5.25V$	$V_I=5.5V$	—	—	0.1	mA
	DIR or $\overline{G}$			$V_I=7V$	—	—	0.1	
Supply current**		I_{CCH}	$V_{CC}=5.25V$		—	48	70	mA
		I_{CCL}			—	62	90	
		I_{CCZ}			—	64	95	
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		—	—	−1.5	V

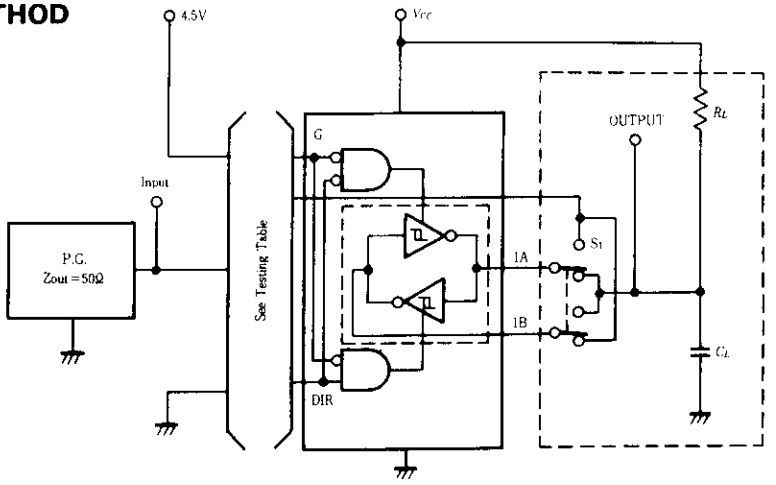
* $V_{CC}=5V$, $Ta=25°C$
** I_{CC} is measured with all outputs open.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	A	B	$C_L=45pF$ $R_L=667\Omega$	—	19	25	ns
		B	A		—	19	25	ns
	t_{PHL}	A	B		—	14	25	ns
		B	A		—	14	25	ns
Output enable time	t_{PLH}	$\overline{G}$	A		—	26	40	ns
		$\overline{G}$	B		—	28	40	ns
	t_{PHL}	$\overline{G}$	A		—	43	60	ns
		$\overline{G}$	B		—	39	60	ns

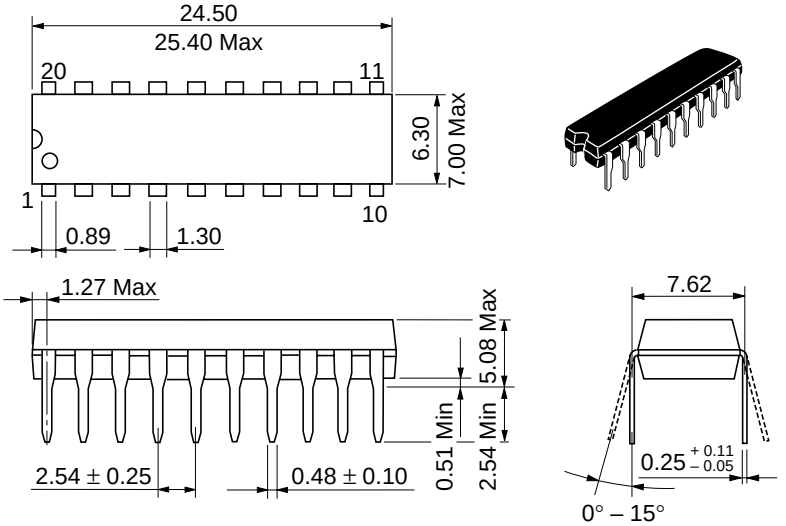
■TESTING METHOD

Test Circuit



Notes) 1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B are identical to above load circuit.
2. C_L includes probe and jig capacitance.
3. S_1 is a input-output switch.

Unit: mm


24.50
25.40 Max
20
11
6.30
7.00 Max
1
10
0.89
1.30
1.27 Max
5.08 Max
0.51 Min
2.54 Min
2.54 ± 0.25
0.48 ± 0.10
7.62
0.25 +0.11 −0.05
0° – 15°

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