OKI Semiconductor

MSM6542-01/02/03

REAL TIME CLOCK WITH PERIODIC AND ALARM OUTPUT

DESCRIPTION

The MSM6542 is a perpetual-calendar-based real time clock with an alarm function which can read and write data in units of seconds. It can be connected to various buses and can function as a peripheral IC of a microcomputer.

The clock ranges are seconds, minutes, hours, days, months, years, and days of the week. The alarm ranges are seconds, minutes, hours, days, months, and days of the week.

An event trigger is generated when the time matches the specified time and an alarm occurs or when the clock counter generates a carry. The interrupt and pulse outputs are provided for each of an alarm and a carry.

An interface with a microcomputer is implemented by four data bus pins, four address bus bus pins, three control bus pins, and two chip select pins. These pins are used to write or read data from the clock, alarm, and control registers, or to modify the data.

The MSM6542 has an address latch enable (ALE) input pin, allowing the data bus and address bus to be shared. When the ALE input pin is kept high, the data bus and address bus can be exclusively used.

Other functions of the MSM6542 are: a 30-second adjustment, stop and restart of clock, data registers as RAM, and data register (RAM) protection.

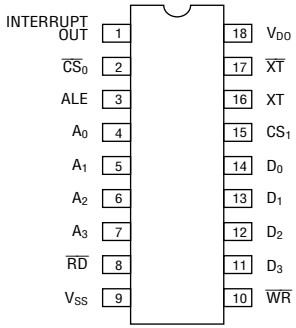
The CMOS circuitry used in the MSM6542 affords low power dissipation. The crystal oscillator operates at 32.768 kHz. Provisions for backup time keeping are included.

FEATURES

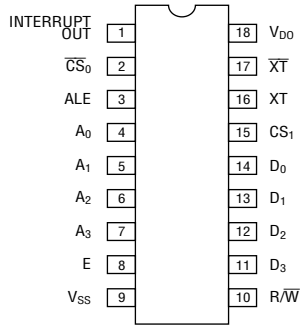
- Real time clock providing seconds, minutes, hours, days, months, years, and days of the week.
- Multiple alarm ranges covering seconds, minutes, hours, days, months, and days of the week. A desired alarm range can be selected.
- A periodic interrupt output interval can be selected over a wide range from 1/1024 seconds up to 10 minutes.
- Interface flexibility allows for connection to many types of microprocessors.
- Single read-out procedure (Read flag).
- Single power sense circuitry. (Data protect function).
- Unused registers can be used as RAM.
- 30-second adjustment by software or hardware (software only for the MSM6542-1/-2).
- Stop and restart of clock by software or hardware (software only for the MSM6542-
- 1 Hz output for adjustment and check of oscillation frequency (MSM6542-3 only).
- User selection of 12 or 24 hour clock mode.
- Address latch enable (ALE) input pin.
- Advanced CMOS circuitry allows low stand-by voltage and current.
- User standard 32.768 kHz oscillator crystal
- Available in multiple packages
  - 18-pin plastic DIP (for the MSM6542-1RS/2RS) (DIP18-P-300).
  - 20-pin plastic SOP (for the MSM6542-1MS-K/2MS-K) (SSOP20-P-250-K).
  - 24-pin plastic DIP (for the MSM6542-3RS) (DIP24-P-600).
  - 24-pin plastic SOP (for the MSM6542-3GS-VK) (SOP24-P-430-VK).
- Pin assignment compatibility with the MSM6242BRS (The MSM6542-3MSK provides near compatibility.).

PIN CONFIGURATION

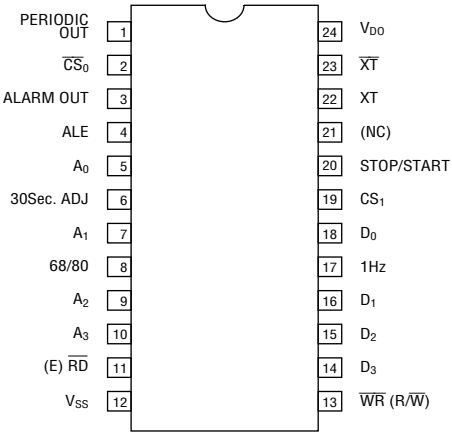
MSM6542-01RS
18-pin plastic DIP (top view)



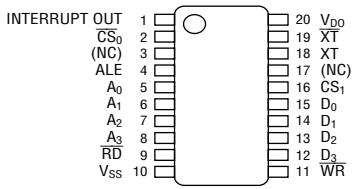
MSM6542-02RS
18-pin plastic DIP (top view)



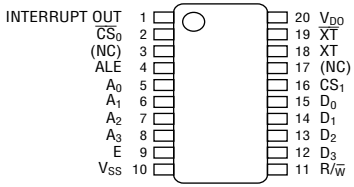
MSM6542-03RS
24-pin plastic DIP (top view)



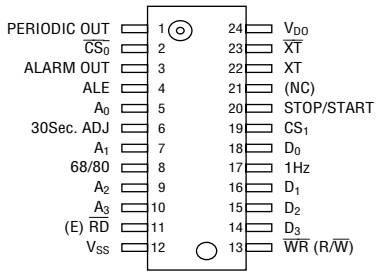
MSM6542-01MS-K
20-pin plastic SOP (top view)



MSM6542-02MS-K
20-pin plastic SOP (top view)

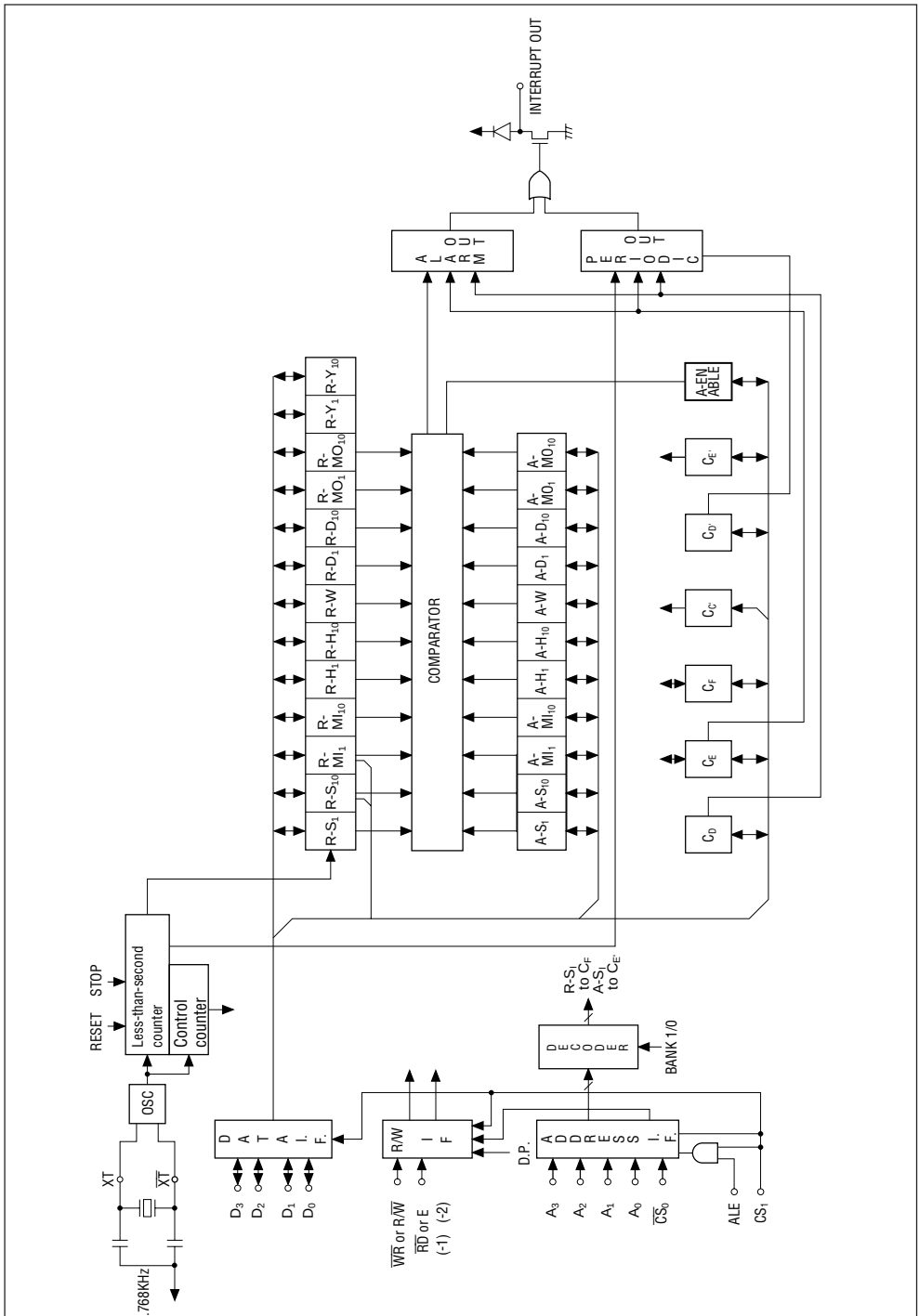


MSM6542-03GS-VK
24-pin plastic SOP (top view)

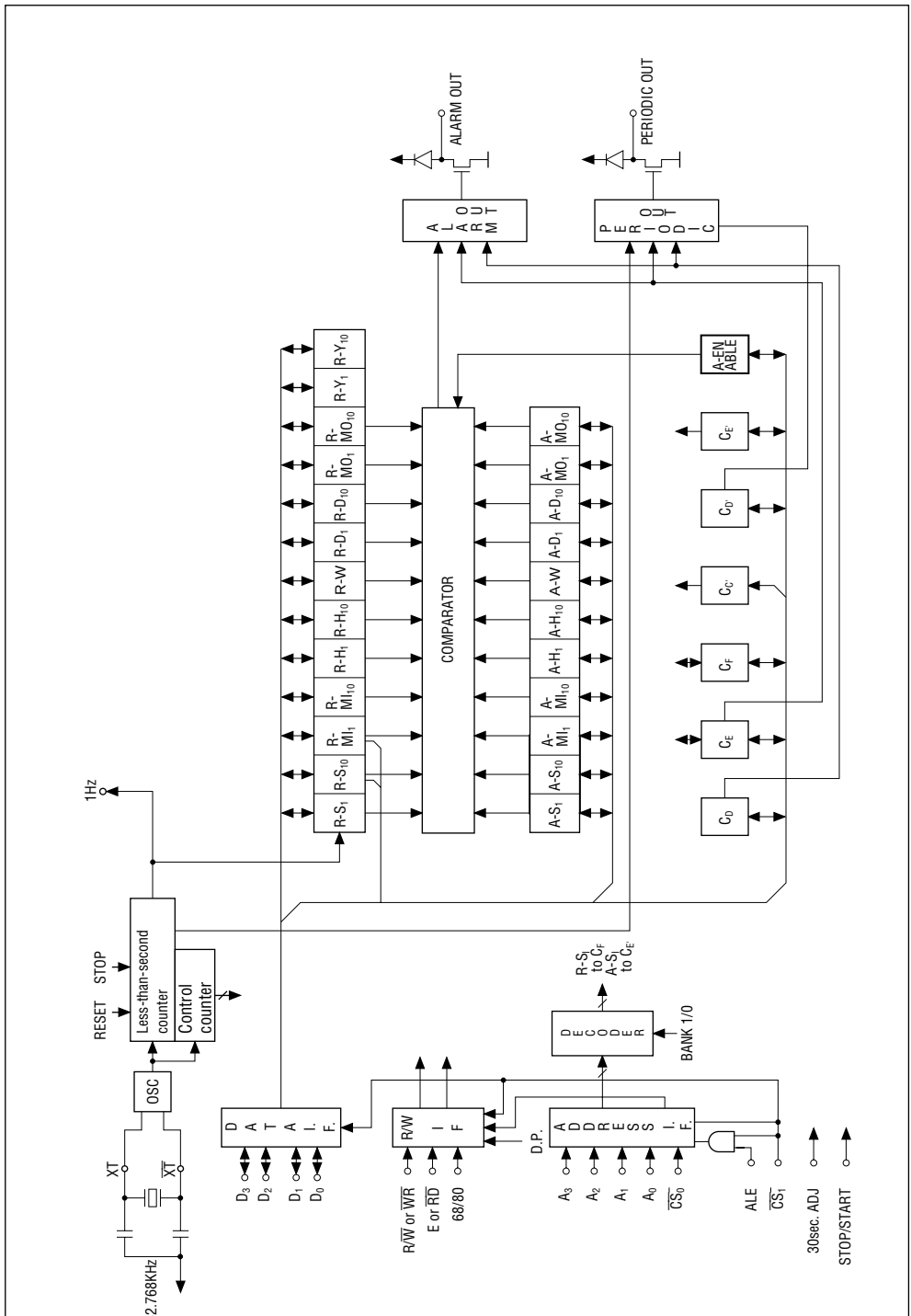


NC : NO Connected (open)

FUNCTIONAL BLOCK DIAGRAM (MSM6542-01, 02)



FUNCTIONAL BLOCK DIAGRAM (MSM6542-03)



REGISTER TABLE

A_3	A_2	A_1	A_0	BANK 0						BANK 1					
				Register symbol	D_3	D_2	D_1	D_0	Register name	Register symbol	D_3	D_2	D_1	D_0	Register name
0	0	0	0	R-S_1	r-s_8	r-s_4	r-s_2	r-s_1	Real time one-second digit register	A-S_1	a-s_8	a-s_4	a-s_2	a-s_1	Alarm one-second digit register
0	0	0	1	R-S_{10}	–	r-s_{40}	r-s_{20}	r-s_{10}	Real time ten-second digit register	A-S_{10}	*	a-s_{40}	a-s_{20}	a-s_{10}	Alarm ten-second digit register
0	0	1	0	R-MI_1	r-mi_8	r-mi_4	r-mi_2	r-mi_1	Real time one-minute digit register	A-MI_1	a-mi_8	a-mi_4	a-mi_2	a-mi_1	Alarm one-minute digit register
0	0	1	1	R-MI_{10}	–	r-mi_{40}	r-mi_{20}	r-mi_{10}	Real time ten-minute digit register	A-MI_{10}	*	a-mi_{40}	a-mi_{20}	a-mi_{10}	Alarm ten-minute digit register
0	1	0	0	R-H_1	r-h_8	r-h_4	r-h_2	r-h_1	Real time one-hour digit register	A-H_1	a-h_8	a-h_4	r-h_2	a-h_1	Alarm one-hour digit register
0	1	0	1	R-H_{10}	–	r-pm/am	r-h_{20}	r-h_{10}	Real time PM/AM ten-hour digit register	A-H_{10}	*	a-PM/AM	a-h_{20}	a-h_{10}	Alarm PM/AM ten-hour digit register
0	1	1	0	R-D_1	r-d_8	r-d_4	r-d_2	r-d_1	Real time one-day digit register	A-D_1	a-d_8	a-d_4	a-d_2	a-d_1	Alarm one-day digit register
0	1	1	1	R-D_{10}	*	*	r-d_{20}	r-d_{10}	Real time ten-day digit register	A-D_{10}	*	*	a-d_{20}	a-d_{10}	Alarm ten-day digit register
1	0	0	0	R-MO_1	r-mo_8	r-mo_4	r-mo_2	r-mo_1	Real time one-month digit register	A-MO_1	a-mo_8	a-mo_4	a-mo_2	a-mo_1	Alarm one-month digit register
1	0	0	1	R-MO_{10}	*	*	*	r-mo_{10}	Real time ten-month digit register	A-MO_{10}	*	*	*	a-mo_{10}	Alarm ten-month digit register
1	0	1	0	R-Y_1	r-y_8	r-y_4	r-y_2	r-y_1	Real time one-year digit register	A-W	*	a-w_4	a-w_2	a-w_1	Alarm day-of-week register
1	0	1	1	R-Y_{10}	r-y_{80}	r-y_{40}	r-y_{20}	r-y_{10}	Real time ten-year digit register	A-ENABLE	a-e_8	a-e_4	a-e_2	a-e_1	Register to specify the alarm range
1	1	0	0	R-W	–	r-w_4	r-w_2	r-w_1	Real time day-of-week register	$C_{C'}$	–	–	$TEST_2$	$TEST_1$	Control C register
1	1	0	1	C_D	IT/PLS_2	IT/PLS_1	$MASK_2$	$MASK_1$	Control D register	$C_{D'}$	–	CY_2	CY_1	CY_0	Control D' register
1	1	1	0	C_E	IRQ $FLAG_0$	REST	IRQ $FLAG_2$	IRQ $FLAG_1$	Control E register	$C_{E'}$	HD/SFT	24/12	CAL	DP	Control E' register
1	1	1	1	C_F	BANKI/O	STOP	30-s adjustment	READ FLAG	Control F register	Same as BANK 0					

es:

Since positive logic is used, the high level on a data bus corresponds to 1 in a register.
When DP = 1, data can be written in the BANK 1/0 and DP bits.
Wnen 0 is written in the DP bit, a delay is required until the bit is set at 0.
READ FLAG and IRQ.$FLAG_0$ are read-only flags. READ FLAG is cleared after data is read from it.
IRQ. $FLAG_1$ is cleared after data is read from it with IT/PLS_1 set at 1. When IT/PLS_1 is 0, only 0 can be written in IRQ. $FLAG_1$ and it cannot be cleared when it is read. Similarly, IRQ. $FLAG_2$ is cleared after data is read from it with IT/PLS_2 set at 1. When IT/PLS_2 is 0, only 0 can be written in IRQ. $FLAG_2$ and it cannot be cleared when it is read.
For the MSM6542-01/02, HD/SFT is set internally at 0.
Data can be written in the $C_{C'}$ register but it is cleared when it is read. Therefore, read data is always 0.
When r-pm/am is 1, the time is P.M. When it is 0, the time is A.M. This is also true for a-pm/am.
The contents of all registers are unpredictable when power is turned on from 0V to 5V.
A hyphen in the table indicates that the bit is not present. When the bit is read, it always provides 0.
When a bit marked an asterisk (*) in the table is used as part of a clock register or alarm register, it always provides 0 at read. When the bit is used as part of RAM, however, it can be used for read and write.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Condition	Value	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to 7	V
Input voltage	V_I	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_O	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Storage temperature range	T_{STG}	–	–55 to +150	°C

Operation Range

Rating	Symbol	Condition	Value	Unit
Power supply voltage	V_{DD}	–	4.5 to 5.5	V
Clock power supply voltage	V_{CLK}	–	2.0 to 6	V
Crystal oscillator frequency	$f_{(xt)}$	–	32.768	kHz
Operating temperature range	T_{OP}	–	–40 to +85	°C

Note: The clock power supply voltage is required to assure operation of the crystal oscillator and clock.

DC Characteristics

(V_{DD} = 5V ±10%, Ta = -40 ~ +85°C)

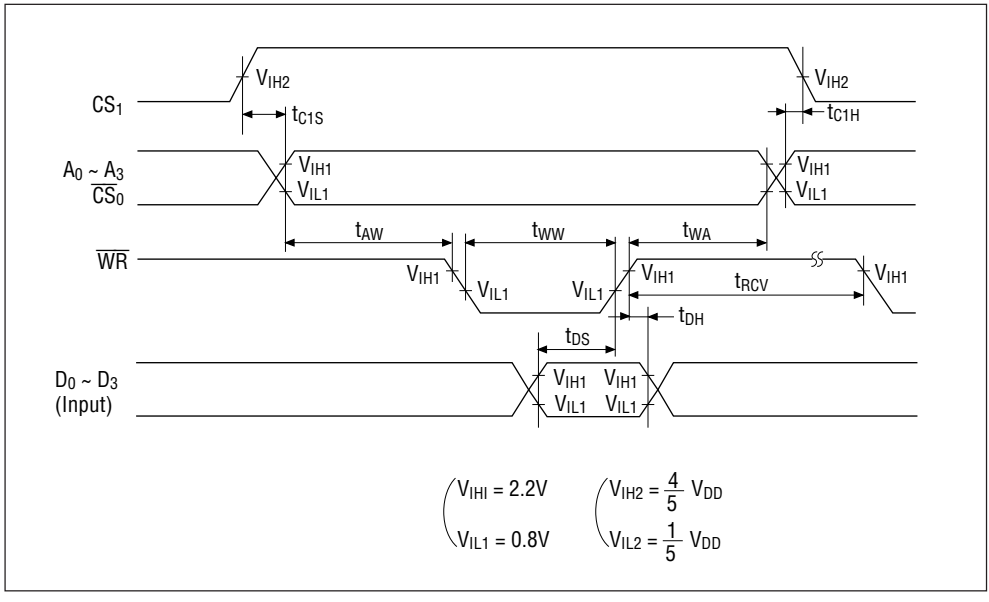
Rating	Symbol	Condition	Min.	Typ.	Max.		Applicable pin
High input voltage (1)	V_{IH1}		2.2	–	–	V	$\overline{CS}_0$, A_0 ~A_3, D_0 ~ D_3 $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), ALE, 30-s ADJ
Low input voltage (1)	V_{IL1}		–	–	0.8		
High input voltage (2)	V_{IH2}		0.8 V_{DD}	–	–		STOP/START
Low input voltage (2)	V_{IL2}		–	–	0.2 V_{DD}		CS_1, 68/80
Input leakage (1)	I_{LK1}	V_1 = V_{DD}/0V	–1	–	1	µA	$\overline{CS}_0$, ALE, A_0 ~ A_3, 68/80, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), CS1, 30-s ADJ
Input leakage (2)	I_{LK2}		–10	–	10		D_0 ~ D_3, STOP/START
High input current	I_{IH}	V_{IH} = 0.8 V_{DD}	–100	–	–20		STOP/START
Low input current	I_{IL}	V_{IL} = 0.2 V_{DD}	20	–	100		
High output voltage	V_{OH}	I_{OH} = –400 µA	2.4	–	–	V	D_0 ~ D_3, 1Hz
Low output voltage (1)	V_{OL1}	I_{OL} = 2.5 mA	–	–	0.4		
Low output voltage (2)	V_{OL2}	I_{OL} = 2.5 mA	–	–	0.4		INTERRUPT PERIODIC OUT ALARM
Leakage current	I_{OFFLK}	V_I = V_{DD}/0V	–	–	10	µA	
Current consumption (1)	I_{DD1}	Oscillation at 32.768 kHz, V_{DD} = 5V	–	–	30	µA	V_{DD}
Current consumption (2)	I_{DD2}	CS_1 ≈ 0V, V_{DD} = 2V	–	–	5		
Input capacitance (1)	C_{I1}	Input oscillator Frequency 1 MHz	–	3	–	pF	Input pins other than D_0 to D_3
Input capacitance (2)	C_{I2}		–	5	–		D_0 to D_3

Switching Characteristics

80-xxx
Write mode (ALE is always at V_{DD}.)

(V_{DD} = 5V ±10%, Ta = –40 to +85°C (in the 80 mode for the MSM6542-01/03))

Rating	Symbol	Condition	Min.	Typ.	Max.	Unit
CS_1 set-up time	t_{C1S}	–	1000	–	–	ns
CS_1 hold time	t_{C1H}	–	1000	–	–	ns
Address stable before WRITE	t_{AW}	–	20	–	–	ns
Address stabel after WRITE	t_{WA}	–	10	–	–	ns
WRITE pulse width	t_{WW}	–	120	–	–	ns
Data set-up time	t_{DS}	–	100	–	–	ns
Data hold time	t_{DH}	–	10	–	–	ns
$\overline{RD}/\overline{WR}$ recovery time	t_{RCV}	–	100	–	–	ns

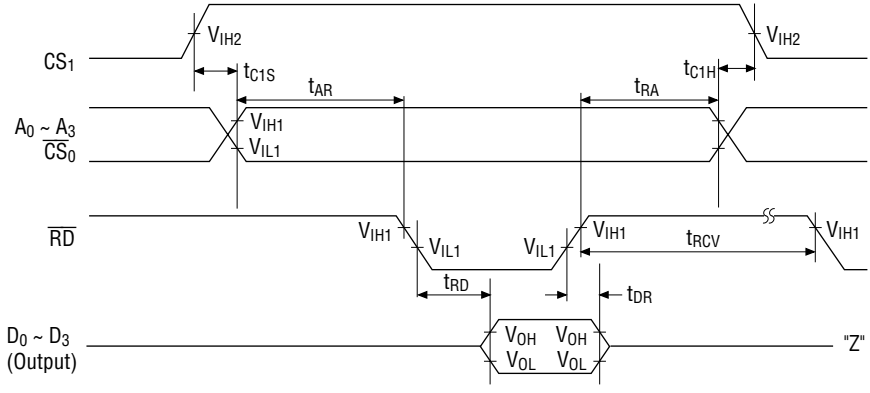


80-xxx

Read mode (ALE is always at V_{DD}.)

(V_{DD} = 5V ±10%, Ta = –40 to +85°C (in the 80 mode for the MSM6542-01/03))

Rating	Symbol	Condition	Min.	Typ.	Max.	Unit
CS_1 set-up time	t_{C1S}	–	1000	–	–	ns
CS_1 hold time	t_{C1H}	–	1000	–	–	ns
Address stable before READ	t_{AR}	–	20	–	–	ns
Address stable after READ	t_{RA}	–	20	–	–	ns
$\overline{RD}$ to data	t_{RD}	CL = 150 pF	–	–	120	ns
Data hold	t_{DR}	–	10	–	45	ns
$\overline{RD}/\overline{WR}$ recovery time	t_{RCV}	–	100	–	–	ns

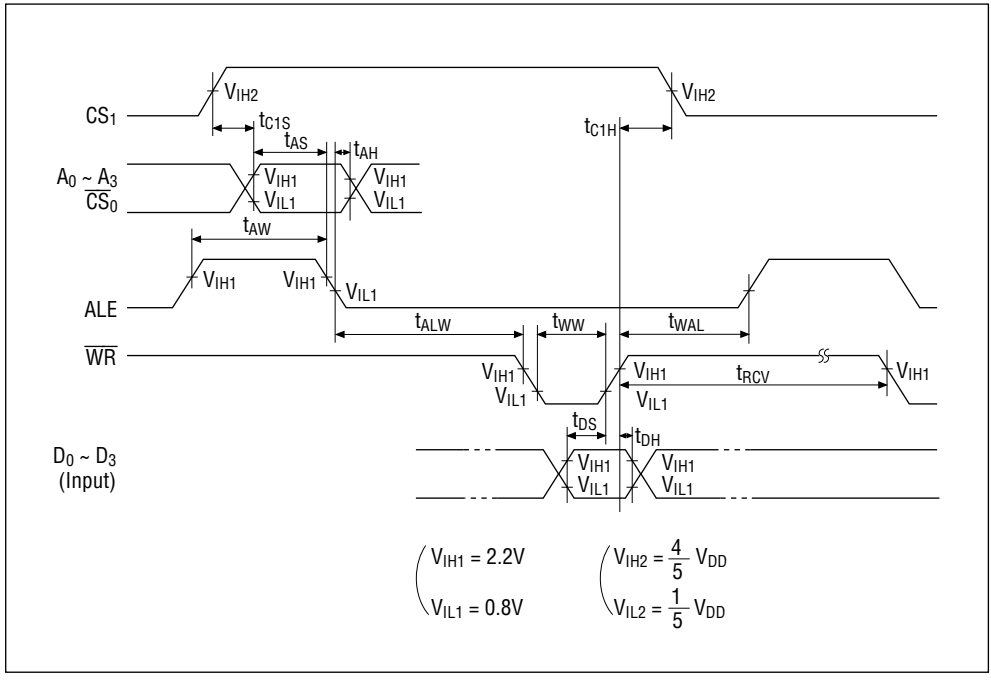


80-xxx

Write mode (ALE is used.)

(V_{DD} = 5V ±10%, Ta = –40 to +85°C (in the 80 mode for the MSM6542-01/03))

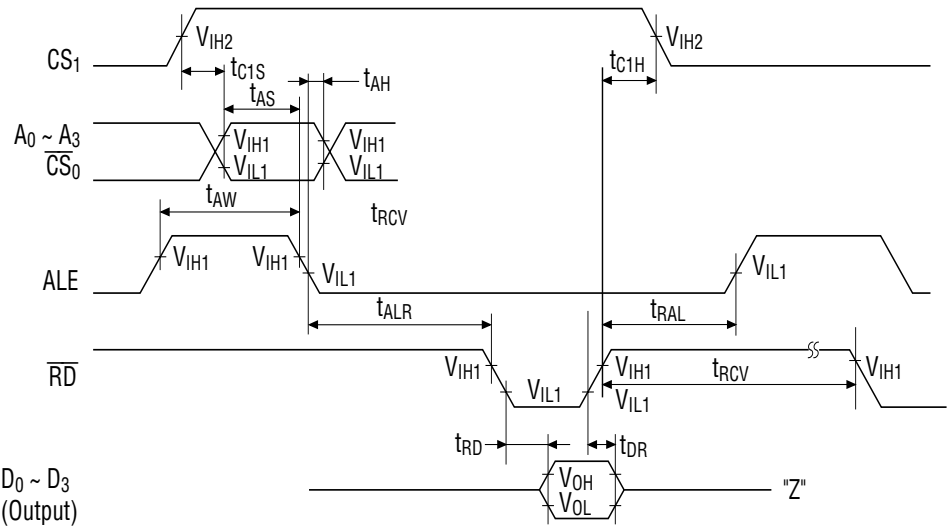
Rating	Symbol	Condition	Min.	Typ.	Max.	Unit
CS_1 set-up time	t_{C1S}	–	1000	–	–	ns
Address set-up time	t_{AS}	–	25	–	–	ns
Address hold time	t_{AH}	–	25	–	–	ns
ALE pulse width	t_{AW}	–	40	–	–	ns
ALE before WRITE	t_{ALW}	–	10	–	–	ns
WRITE pulse width	t_{WW}	–	120	–	–	ns
ALE after WRITE	t_{WAL}	–	20	–	–	ns
Data set-up time	t_{DS}	–	100	–	–	ns
Data hold time	t_{DH}	–	10	–	–	ns
CS_1 hold time	t_{C1H}	–	1000	–	–	ns
$\overline{RD}/\overline{WR}$ recovery time	t_{RCV}	–	100	–	–	ns



80-xxx
Read mode (ALE is used.)

(V_{DD} = 5V ±10%, Ta = –40 to +85°C (in the 80 mode for the MSM6542-01/03))

Rating	Symbol	Condition	Min.	Typ.	Max.	Unit
CS_1 set-up time	t_{C1S}	–	1000	–	–	ns
Address set-up time	t_{AS}	–	25	–	–	ns
Address hold time	t_{AH}	–	25	–	–	ns
ALE pulse width	t_{AW}	–	40	–	–	ns
ALE before READ	t_{ALR}	–	10	–	–	ns
ALE after READ	t_{RAL}	–	20	–	–	ns
$\overline{RD}$ to data	t_{RD}	CL = 150 pF	–	–	120	ns
Data hold	t_{DR}	–	10	–	45	ns
CS_1 hold time	t_{C1H}	–	1000	–	–	ns
$\overline{RD}/\overline{WR}$ recovery time	t_{RCV}	–	100	–	–	ns



$V_{IH1} = 2.2V$, $V_{IL1} = 0.8V$

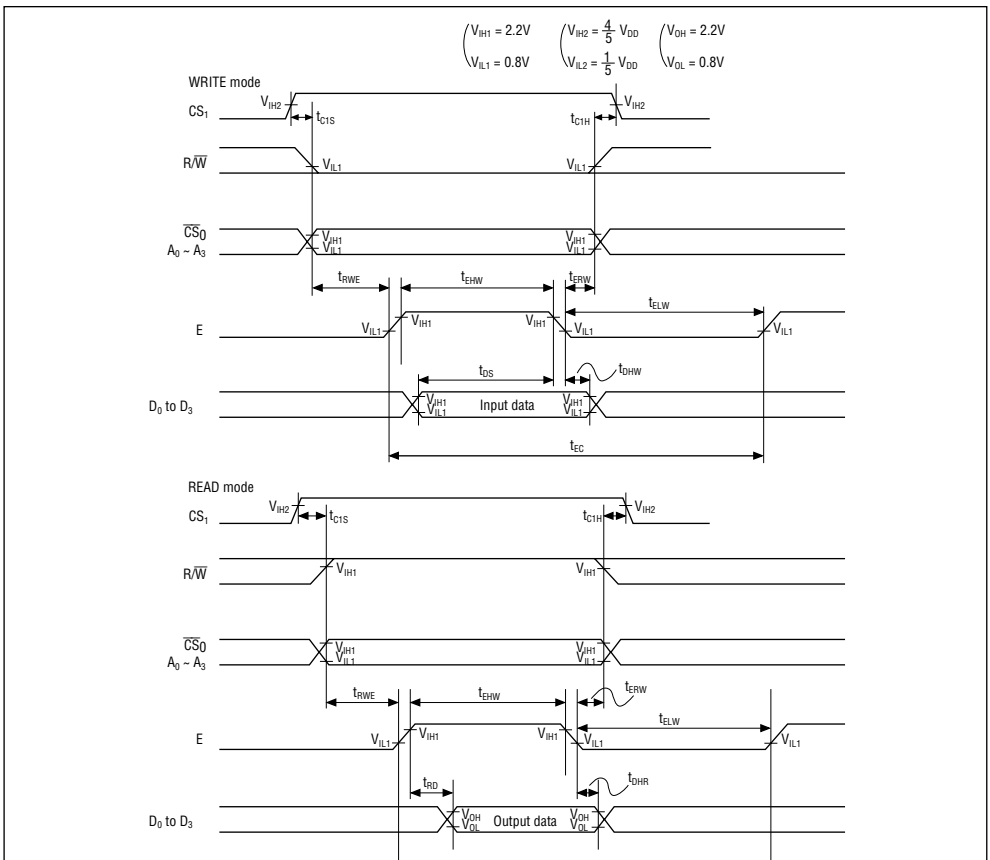
$V_{IH2} = \frac{4}{5} V_{DD}$, $V_{IL2} = \frac{1}{5} V_{DD}$

$V_{OH} = 2.2V$, $V_{OL} = 0.8V$

68-xxx

(V_{DD} = 5V ±10%, Ta = 0°C to +70°C (in the 86 mode for the MSM6542-02/03))

Rating	Symbol	Condition	Min.	Typ.	Max.	Unit
CS_1 set-up time	t_{C1S}	–	1000	–	–	ns
R/$\overline{W}$ address set-up time	t_{RWE}	–	100	–	–	ns
E 'H' pulse width	t_{EHW}	–	220	–	–	ns
R/$\overline{W}$ address hold time	t_{ERW}	–	20	–	–	ns
E 'L' pulse width	t_{ELW}	–	220	–	–	ns
E cycle time	t_{EC}	–	500	–	–	ns
Data set-up time	t_{DS}	–	180	–	–	ns
WRITE data hold time	t_{DHW}	–	20	–	–	ns
E to data	t_{RD}	CL = 150 pF	–	–	120	ns
READ data hold time	t_{DHR}	–	10	–	–	ns
CS_1 hold time	t_{C1H}	–	1000	–	–	ns



DESCRIPTION OF PINS

D_0 to D_3 (Data bus pins 0 to 3)

These input pins connected to the data bus of a microcomputer are used for the microcomputer to read and write registers. The interface uses the positive logic. When $\overline{CS}_0$ is low, CS_1 is high, $\overline{RD}$ is low, and $\overline{WR}$ is high (for the 68-xxx system, $\overline{CS}_0$ is low, CS_1 is high, R/$\overline{W}$ is high, and E is high), these data bus pins are in the output mode. In the other cases, they are in the high impedance status.

A_0 to A_3 (Address bus pins 0 to 3)

These input pins connected to the address bus of a microcomputer specify a register used by the microcomputer for read or write. The address data specified by these pins is used in conjunction with the input to the ALE pin.

ALE (Address Latch Enable)

This input pin is for address and $\overline{CS}_0$.

When the ALE pin is high, the address bus data and $\overline{CS}_0$ are read into the IC. When it is low, the address data and $\overline{CS}_0$ read at ALE = H are retained in the IC. CS_1 functions independently of the ALE pin.

When using an MSC-48-, MSC-51-, or 8085-based microcomputer having an ALE output pin, connect this pin to the ALE output pin of the microcomputer. When a four-bit microcomputer shares the four address bus pins, A_0 to A_3, with another peripheral IC, the ALE pin on this IC can be used to specify it.

When the microcomputer has no ALE output pin, connect the ALE input pin on this IC to the V_{DD}.

$\overline{WR}$ [R/$\overline{W}$] (WRITE [READ/$\overline{WRITE}$])

This input pin is connected to the $\overline{WR}$ pin for the 80-based CPU or the R/$\overline{W}$ pin for the 68-based CPU.

$\overline{RD}$ [E] (READ [E])

This input pin is connected to the $\overline{RD}$ pin for the 80-based CPU or the E pin for the 68-based CPU.

$\overline{CS}_0$, CS_1 (Chip select pins 0 and 1)

These input pins enable or disable input of ALE, $\overline{WR}$ (R/$\overline{W}$), and $\overline{RD}$ (E). When $\overline{CS}_0$ is low and CS_1 is high, these inputs are enabled. In the other combinations, the IC unconditionally assumes that ALE is low and $\overline{WR}$ and $\overline{RD}$ are high (for the 68-based CPU, E is low). However, $\overline{CS}_0$ needs to operate in conjunction with ALE and CS_1 operates independently of ALE. Connect CS_1 to the power supply voltage detection pin. For more information, see the descriptions in "USAGE" and "USE OF CS_1."

PERIODIC OUT (Only for the MSM6542-03)

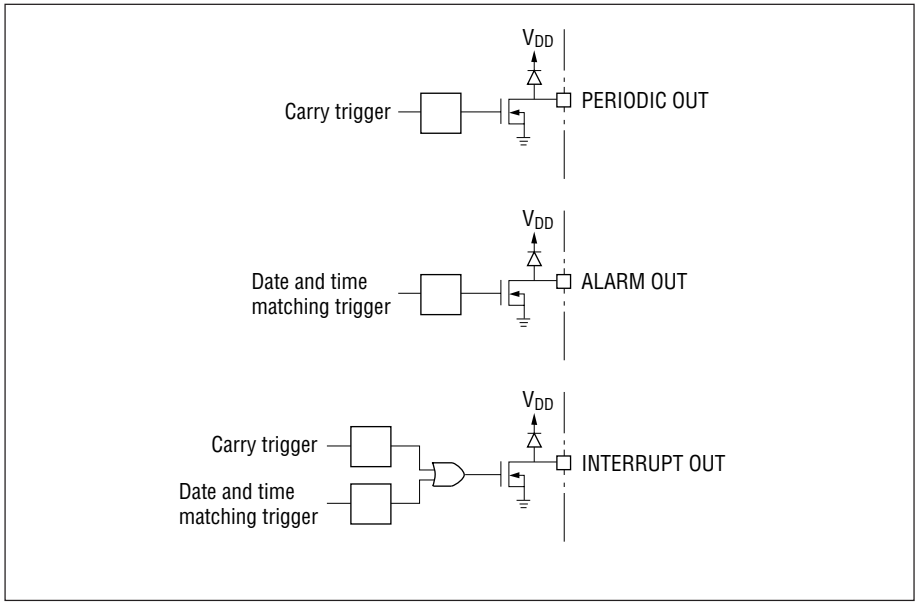
This output pin is used for N-channel open drain. It outputs a single pulse or an interrupt request as a trigger each time a carry is generated from the clock counter. Output from this pin is not disabled by $\overline{CS}_0$ and CS_1.

ALARM OUT (Only for the MSM6542-03)

This output pin is used for N-channel open drain. It outputs a single pulse or an interrupt request each time the contents of the clock counter match the date and time for which an alarm is set. Output from this pin is not disabled by $\overline{CS}_0$ and CS_1.

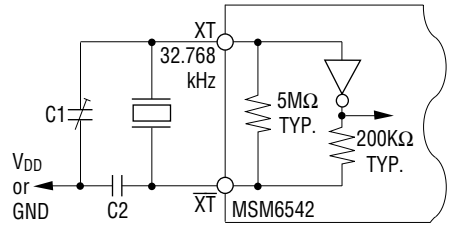
INTERRUPT OUT (Only for the MSM6542-01/02)

This output pin is N-channel open drain. It ORs the signals from the PERIODIC OUT and ALARM OUT pins above.



XT and $\overline{XT}$ (X'tal OSC)

These pins are the connecting terminals to connect the capacitors and crystal oscillator at 32.768kHz as shown below.



Example

(Equivalent series resistance ≤ 30 kΩ
C_1, C_2 = 15 to 30 pF)

Note: Oscillation accuracy and allowable values of the equivalent series resistor for the crystal oscillator depend on the value of the capacitor used for oscillation. For selection of a crystal oscillator and the value of the capacitor needed for it, consult the crystal oscillator manufacturer.

To supply external 32.768 kHz clocks, enter CMOS output or pulled-up TTL output to the XT pin and leave the $\overline{XT}$ pin open.

V_{DD} and V_{SS}

These are power supply pins. Connect the V_{SS} pin to ground and supply positive power to the V_{DD} pin.

The 1 Hz, 30 sec ADJ, STOP/START, and 68/80 pins described below are used only for the MSM6542-03.

1 Hz

This output pin is used to confirm the oscillation frequency. It outputs 1-Hz pluses at a duty cycle of 50%.

This pin provides one-second output from the clock counter. Therefore, it is cleared to a low when the REST bit is high or 30-second adjustment is performed. When STOP function is performed, the output stops at whatever level the output is at that instant.

This pin provides CMOS output level, regardless of the level of the CS_1 pin. If a load is connected to this pin during standby operation, the battery will be quickly dissipated.

30-sec ADJ (30-seconds Adjustment)

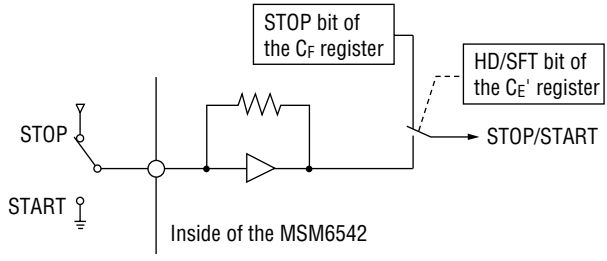
When this input pin goes high, 30-second adjustment is performed on the rising edge. When not used, connect to ground.

STOP/START

This input pin can be used as an integrating clock. When the pin is high, clocking at frequencies lower than 4096 Hz stops. When the pin goes low, clocking is resumed.

The HD/SFT bit of the C_E' register specifies whether the stop/start function is implemented by hardware or software.

When not used, connect to ground. For more information, see the description of "C_F register" and "C_E' register" in "EXPLANATION OF REGISTERS."



Equivalent circuit of the STOP/START pin

68/80

This input pin selects which CPU this IC is to be connected. To connect the IC to the 68-based CPU, leave the pin at V_{DD}. To connect the IC to the 80-based CPU, leave the pin at the ground level.

EXPLANATION OF REGISTERS

Registers R-S_1, R-S_{10}, R-MI_1, R-MI_{10}, R-H_1, R-H_{10}, R-D_1, R-D_{10}, R-MO_1, R-MO_{10}, R-Y_1, R-Y_{10}, R-W

a) The letter R followed by a hyphen (-) in these register names indicate a realtime register. S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, MO_1, MO_{10}, Y_1, Y_{10}, and W are abbreviations for Second 1, Second 10, MInute 1, MInute 10, Hour 1, Hour 10, Day 1, Day 10, MOnth 1, MOnth 10, Year 1, Year 10, and Week. The value of each register is weighted in BCD.

b) Positive logic is used. For example, when (r-s_8, r-s_4, r-s_2, r-s_1) is (1, 0, 0, 1), it indicates 9 seconds.

c) An asterisk (*) in bank 0 in the realtime register table indicates the bit is automatically set at 0 even though the write data is 1, when the CAL bit of the C_E' register is high.

When the CAL bit is low, registers R-D_1, R-D_{10}, R-MO_1, R-MO_{10}, R-Y_1, and R-Y_{10} are used as RAM areas. The bits marked * in these RAM areas can be used for write and read operations.

For more information, see the description of "C_E' register" in "EXPLANATION OF REGISTERS."

d) Be sure not to set non-existent data in an non-RAM area, that is, realtime registers. Otherwise, a clock error may occur.

e) r-pm/am, r-h_{20}, and r-h_{10}

In the 12-hour clock mode, the possible hours are from 1 A.M. to 12 A.M. and from 1 P.M. to 12 P.M. When the bit is 1, it indicates P.M. When the bit is 0, it indicates A.M. In the 24-hour clock mode, the possible hours are from 0 o'clock to 23 o'clock.

During write operation, the r-pm/am bit is ignored in the 24-hour clock mode and the r-h_{20} bit in the 12-hour clock mode.

During read operation, the r-pm/am bit is unconditionally set at 0 in the 24-hour clock mode and the r-h_{20} bit in the 12-hour clock mode.

f) R-Y_1 and R-Y_{10}

The IC described in this manual operates in Gregorian years. When it operates in Japanese calendar years (Heisei), a leap year is also automatically determined. Leap years are 1992, 1996, 2000, 2004, 2008, and so on.

g) R-W

The R -W bits counts from 0 to 6. An example of weighting is shown in the following table.

r-w$_4$	r-w$_2$	r-w$_1$	Day of the week
0	0	0	Sun
0	0	1	Mon
0	1	0	Tue
0	1	1	Wed
1	0	0	Thu
1	0	1	Fri
1	1	0	Sat

Days are not determined from dates.

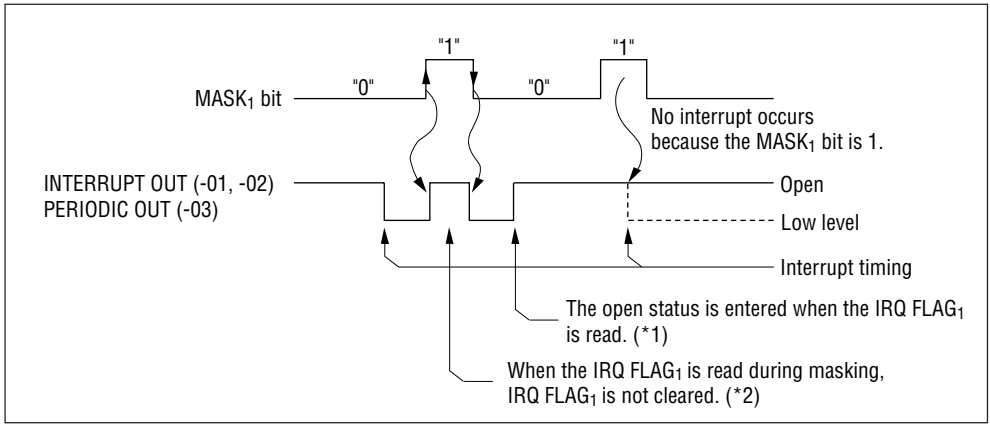
C_D register (Control D Register)

a) $MASK_1$ (D_0)

This bit controls periodic output for which a carry from the clock counter is used as a trigger. When the bit is 0, output is provided from the INTERRUPT OUT pin for the MSM6542-01/02 or the PERIODIC OUT pin for the MSM6542-03. When the bit 1, output is disabled.

The relationships between causes of periodic output and the status of the $MASK_1$ bit are shown below. (For the MSM6542-01/02, data resulting from the ORing of periodic output and alarm output is output to the INTERRUPT OUT pin. For convenience, however, alarm output is ignored in the following description.)

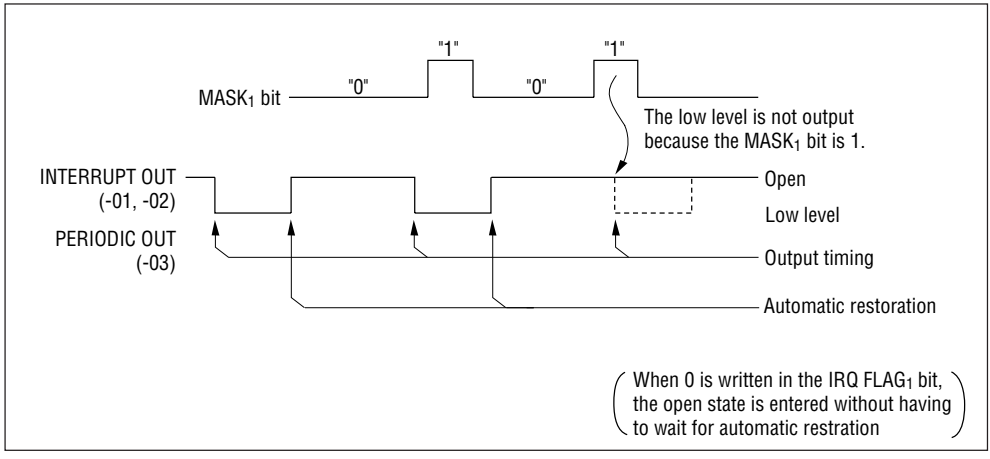
i) In the periodic interrupt mode (when the IT/PLS_1, bit is 1)



*1 When DP = 1, the open state is not entered until a certain period passes after an interrupt is generated. (See the description of the C_E register.)

*2 However, when DP = 1, if the IRQ $FLAG_1$ bit is read out within 122µs after an interrupt is generated, it is cleared after 122µs from the generation of the interrupt.

ii) In the periodic pulse output mode (when the IT/PLS_1 bit is 0.)

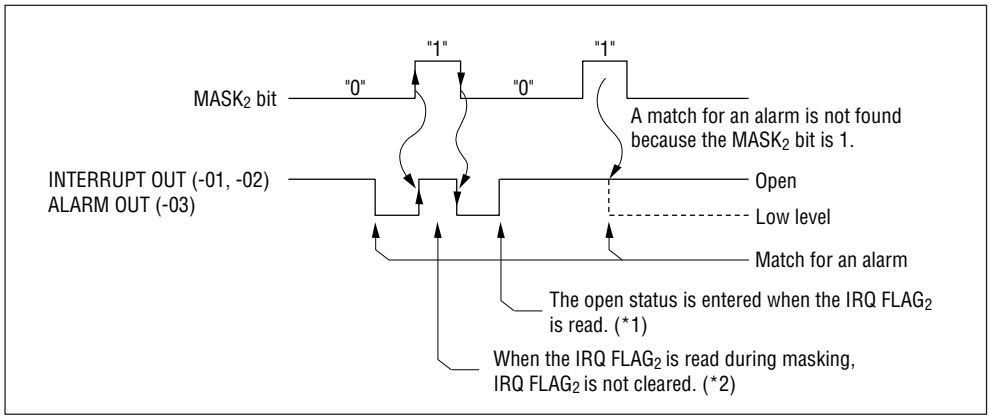


b) $MASK_2$ (D_1)

This bit controls the alarm output each time the contents of the clock counter match the date and time for which an alarm is set. When the bit is 0, an alarm is output from the INTERRUPT OUT pin for the MSM6542-01/02 or the ALARM OUT pin for the MSM6542-3. When the bit is 1, alarm output is disabled.

The relationships between causes of alarm output and the status of the $MASK_2$ bit are shown below. (For the MSM6542-01/02, data resulting from the OR-ing of periodic output and alarm output is output to the INTERRUPT OUT pin. For convenience, however, periodic output is ignored in the following description.)

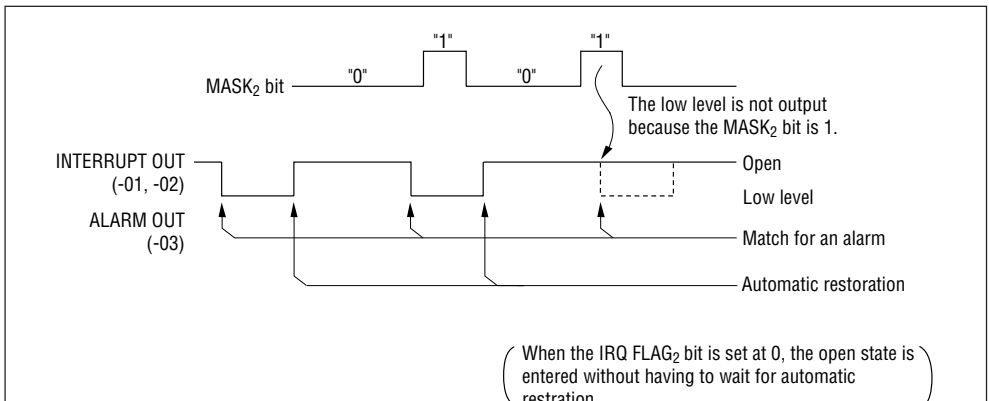
i) In the alarm interrupt mode (when the IT/PLS_2 bit is 1)



*1 When DP = 1, the open state is not entered until a certain period passes after an interrupt is generated. (See the description of the C_E register.)

*2 However, when DP = 1, if the IRQ $FLAG_2$ bit is read out within 122µs after an interrupt is generated, it is cleared after 122µs from the generation of the interrupt.

ii) In the alarm pulse output mode (when the IT/PLS_2 bit is 0)



c) IT/PLS$_1$ (D_2) (InTerrupt/PuLSe $_1$)

This bit determines a mode for periodic output. When the bit is 1, a low-level interrupt request is output from the INTERRUPT OUT pin for the MSM6542-01/02 or from the PERIODIC OUT pin for the MSM6542-3. When the bit is 0, a low-level pulse is output. In this case, the MASK$_1$ bit is 0. The output periods of interrupt output and pulse output are determined by the setting of the C_D' register.

d) IT/PLS$_2$ (D_3) (InTerrupt/PuLSe $_2$)

This bit determines a mode for alarm output. When the bit is 1, a low-level alarm interrupt request is output from the INTERRUPT OUT pin for the MSM6542-01/02 or from the ALARM OUT pin for the MSM6542-03. When the bit is 0, a low-level pulse is output. In this case, the MASK$_2$ bit is 0. When the contents of the alarm register match those of the realtime counter within the range specified by the A-ENABLE register, an output waveform is provided.

In the alarm pulse output mode, the low level of a pulse lasts for about 61 µs.

C_E register (Control E register)

a) IRQ FLAG$_1$ (D_0) (Interrupt ReQuest FLAG$_1$)

The status of this bit depends on the hardware output, low or open, from the PERIODIC OUT pin for the MSM6542-3 or INTERRUPT OUT pin which uses carry as a trigger for the MSM6542-1/2. When hardware output is low, the bit is set at 1. When it is open, the bit is set at 0.

The IRQ FLAG$_1$ bit is mainly used to indicate that there is an interrupt request for the microcomputer. When the period set by the D_2 (CY_2), D_1 (CY_1), and D_0 (CY_0) bits of the C_D' register expires with the D_0 (MASK$_1$) bit of the C_D register set at 0, output from the INTERRUPT OUT pin changes from open to low. At the same time, the IRQ FLAG$_1$ bit changes from 0 to 1.

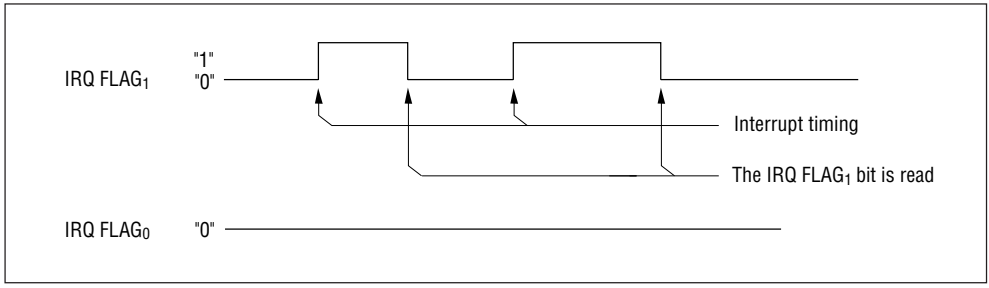
When the D_2 (IT/PLS$_1$) bit of the C_D register is 1 (interrupt mode), the IRQ FLAG$_1$ bit remains at 1 (hardware output is low) until the bit is read. When the bit is read, it is cleared. However, when the IRQ FLAG$_1$ bit is read whithin about 122 µs of occurrence of an interrupt with the D_0 (DP) bit of the C_E' register set at 1, the IRQ FLAG$_1$ bit is not cleared immediately. It is cleared about 122 µs after the interrupt occurs. When the bit is read at least about 122 µs after an interrupt occurs, it is cleared immediately.

In the interrupt mode, writing 0 in the IRQ FLAG$_1$ bit does not clear the bit. When another interrupt occurs with the bit set at 1, it is ignored.

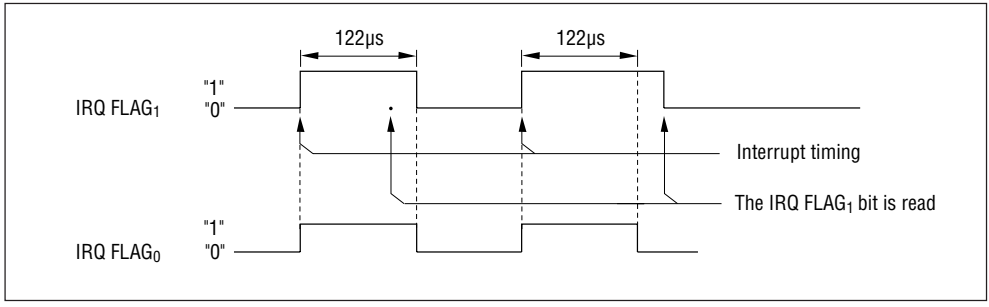
When the D_2 (IT/PLS$_1$) bit of the C_D register is 0 (periodic pulse output mode), the IRQ FLAG$_1$ bit remains at 1 (hardware output is low) until 0 is written in the bit or the automatic restoration time determined by the period set by the D_2 (CY_2), D_1 (CY_1), and D_0 (CY_0) bits of the C_D' register expires. When the IRQ FLAG$_1$ bit is read in the periodic pulse output mode, it is not cleared.

i) In the interrupt mode (when the IT/PLS_1 bit is 1)

(i-1) When DP is 0:

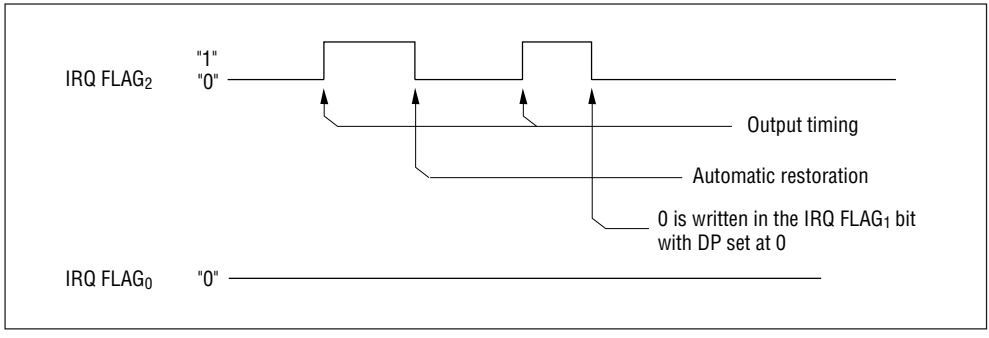


(i-2) When DP is 1:



Note: When the IRQ $FLAG_1$ bit is read within the 122 µs interval with the $MASK_1$ bit set at 1, it is not cleared. The IRQ $FLAG_1$ bit is cleared after the 122 µs interval ends.

ii) In the periodic pulse output mode (when the IT/PLS_1 bit is 0)



b) IRQ $FLAG_2$ (D_1) (Interrupt ReQuest $FLAG_2$)

The status of this bit depends on the hardware output, low or open, from the ALARM OUT pin for the MSM6542-03 or INTERRUPT OUT pin which uses a match with a set alarm time as a trigger for the MSM6542-01/02. When hardware output is low, the bit is set at 1. When it is open, the bit is set at 1.

The IRQ $FLAG_2$ bit is mainly used to indicate that there is an alarm timer interrupt for the microcomputer. When the time set by alarm registers, A-S_1 to A-W, and the A-ENABLE register expires with the D_1 ($MASK_2$) bit of the C_D register set at 0, hardware output changes from open to low. At the same time, the IRQ $FLAG_2$ bit changes from 0 to 1.

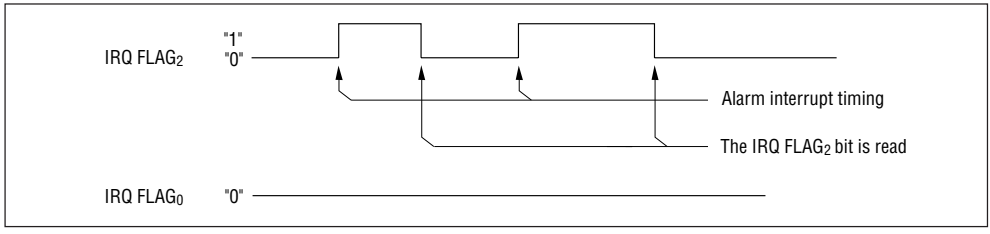
When the D_3 (IT/PLS_2) bit of the C_D register is 1 (alarm interrupt mode), the IRQ $FLAG_2$ bit remains at 1 (hardware output is low) until the bit is read. When the bit is read, it is cleared. However, when the IRQ $FLAG_2$ bit is read within about 122 µs of occurrence of an alarm interrupt with the D_0 (DP) bit of the C_E' register set at 1, the IRQ $FLAG_2$ bit is not cleared immediately. It is cleared about 122 µs after the interrupt occurs. When the bit is read at least about 122 µs after an interrupt occurs, it is cleared immediately.

In the alarm interrupt mode, writing 0 in the IRQ $FLAG_2$ bit does not clear the bit. When another interrupt occurs with the bit set at 1, it is ignored.

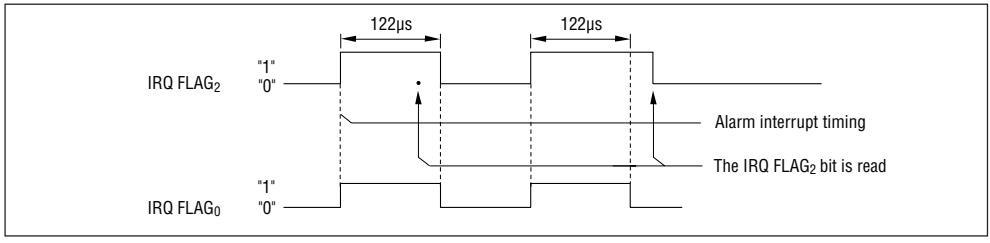
When the D_3 (IT/PLS_2) bit of the C_D register is 0 (alarm pulse output mode), the IRQ $FLAG_2$ bit remains at 1 (hardware output is low) until 0 is written in the bit or automatic restoration is performed about 61 µs later. When the IRQ $FLAG_2$ bit is read in the alarm pulse output mode, it is not cleared.

i) In the alarm interrupt mode (when the IT/PLS_2 bit is 1)

(i-1) When DP is 0:

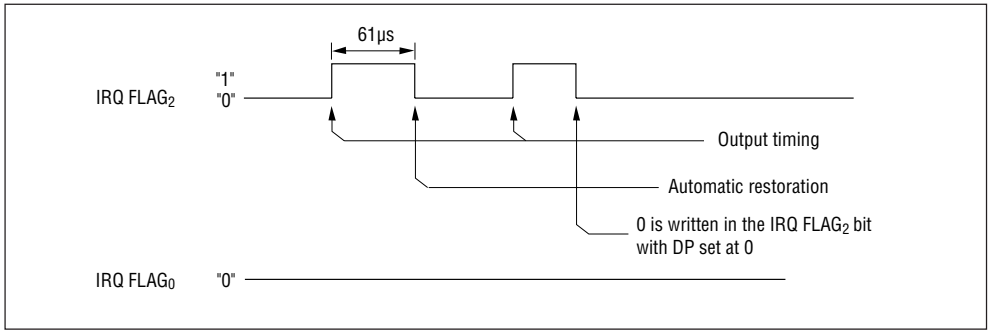


(i-2) When DP is 1:



Note: When the IRQ $FLAG_2$ bit is read within the 122 µs interval with the $MASK_1$ bit set at 1, it is not cleared. The IRQ $FLAG_2$ bit is cleared after the 122 µs interval ends.

ii) In the alarm pulse output mode (when the IT/PLS_2 bit is 0)



c) REST (D_2) (RESeT)

This bit resets the less-than-second counter. While the bit is 1, the counter is being reset. When 0 is written in the bit, reset is canceled.

When CS_1 goes low, the REST bit is automatically set at 0. When 1 is written in the bit, the $TEST_1$ and $TEST_2$ bits of the C_C' register are also set at 0.

d) IRQ $FLAG_0$ (D_3) (Interrupt ReQuest $FLAG_0$)

This bit indicates whether the extended time zone for interrupt output is in progress when the DP is 1. The bit is set at 1 when: (1) the D_2 (IT/PLS_1) bit of the C_D register is 1 (periodic interrupt mode) or the D_3 (IT/PLS_2) bit of the C_D registe is 1 (alarm interrupt mode), (2) the D_0 (DP) bit of the C_E' register is 1 (data protect mode), and (3) 122 µs (extended time zone) do not elapse after a periodic interrupt or an alarm interrupt occurs. When 122 µs elapse after occurrence of such an interrupt, the bit is automatically set at 0.

The bit is not cleared when it is read. Also, data cannot be written in the bit.

C_F Register (Control F Register)

a) READ FLAG (D_0)

This bit indicates a one-second carry. It is used to read time data.

When the READ FLAG bit is read, it is reset at 0. The status lasts until the less-than-second realtime counter generates a carry to the one-second counter.

When a carry to the one-second realtime counter is generated, the READ FLAG bit is set at 1. The status lasts until the bit is read.

When a carry to the one-second realtime counter is generated with the READ FLAG bit set at 1, the bit remains unchanged, i.e., at 1.

The READ FLAG bit is also set at 1 when 30-s adjustment is performed by software or hardware. The status last until the bit is read.

For the usage of the READ FLAG bit, see "Reading registers" in reference flowcharts.

b) 30-s ADJ (D_1) (30-s ADJustment)

When 1 is written in this bit, software makes a 30-s adjustment. For 125 µs after this writing, registers R-S_1 to R-W (at addresses 0 to C in bank 0 in the register table) cannot be read or written due to limitations to the inside of the IC. When the CAL bit of the C_E' register is 0, however, registers R-D_1 to R-Y_{10} (at addresses 6 to B in bank 0) which can be used as RAM are as can be read or written during 30-s adjustment. The bit remains at 1 for up to 250 µs after 1 is written in the bit. Then, the bit is automatically reset at 0. Confirm that the bit is automatically reset at 0 before manipulating registers R-S_1 to R-Y_{10} and R-W (when CAL is 0, R-S_1 to R-H_{10} and R-W).

The 30-s ADJ bit is also set at 1 when hardware makes a 30-s adjustment. In this case too, confirm that the bit is automatically reset at 0 before manipulating registers R-S_1 to R-Y_{10} and R-W (when CAL is 0, R-S_1 to R-H_{10} and R-W).

When the 30-s ADJ bit is set at 1, the D_0 (READ FLAG) of the bit C_F register is also set at 1.

c) STOP (D_2)

This bit is used for the integrating clock operated by software. When the bit is set at 1, clocking at 4096 Hz and lower stops. When the bit is set at 0, clocking is resumed.

For the MSM6542-3, the HD/SFT bit of the C_E' register can be used to select hardware or software to implement the stop/restart function.

d) BANK 1/0 (D_3)

When this bit is set at 1, bank 1 is selected. When it is set at 0, bank 0 is selected. The bit can be set even in the data protect mode.

Registers A-S_1, A-S_{10}, A-MI_1, A-MI_{10}, A-H_1, A-H_{10}, A-D_1, A-D_{10}, A-MO_1, A-MO_{10}, A-W

a) The letter A followed by a hyphen (-) in these register names indicate an alarm register. S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, MO_1, MO_{10}, and W are abbreviations or $Second_1$, $Second_{10}$, $MInute_1$, $MInute_{10}$, $Hour_1$, $Hour_{10}$, Day_1, Day_{10}, $MOnth_1$, $MOnth_{10}$, and Week. The value of each register is weighted in BCD.

b) The positive logic is used. For example, when (a-s_8, a-s_4, a-s_2, a-s_1) is (1, 0, 0, 1), it indicates 9 seconds.

c) An asterisk (*) in the alarm register table indicates the bit automatically set at 0 even though the write data is 1. This is true when the alarm register is in the alarm setting range set by the A-ENABLE register.

The registers outside the alarm setting range set by the A-ENABLE register are used as RAM areas. The bits marked * in these RAM areas can be used for write and read operations.

For more information, see the descriptions of "A-ENABLE."

d) Be sure not to set non-existing data in alarm registers in the alarm setting range. Otherwise, an alarm may not be generated.

e) a-pm/am, a-h_{20}, and a-h_{10}

In the 12-hour clock mode, the possible hours are from 1 A.M. to 12 A.M. and from 1 P.M. to 12 P.M. When the bit is 1, it indicates P.M. When the bit is 0, it indicates A.M. In the 24-hour clock mode, the possible hours are from 0 o'clock to 23 o'clock.

In the 12-hour clock mode, the a-h_{20} bit is write-enabled. When 1 is written in it, an alarm indicating an impossible time is generated. This is also true for the other registers: when an impossible alarm time is set, no alarm is generated.

In the 24-hour clock mode, the a-pm/am bit is read- and write-enabled but its status is assumed to be always the same as that of the r-pm/am bit.

f) A-W

The A-W bits use the numbers from 0 to 6. Weight these bits in the same way as for R-W.

g) The alarm registers are not incremented or decremented

A-ENABLE Register (Alarm ENABLE)

This register sets a comparison range for the real time counter and alarm registers.

The alarm registers outside the comparison range can be used as four-bit RAM areas. (The bits marked an asterisk (*) in the register table can be used for write and read operations. When DP is 1, however, write operation is not possible.)

The following table shows the relationships between the status of the A-ENABLE register bits and alarm comparison ranges.

	ae8	ae4	ae2	ae1	Alarm comparlson range
0	0	0	0	0	None
1	0	0	0	1	A ~ S_1
2	0	0	1	0	A-S_1 ~ A-S_{10}
3	0	0	1	1	A-S_1 ~ A-MI_1
4	0	1	0	0	A-S_1 ~ A-MI_{10}
5	0	1	0	1	A-S_1 ~ A-H_1
6	0	1	1	0	A-S_1 ~ A-H_{10}
7	0	1	1	1	A-S_1 ~ A-D_1
8	1	0	0	0	A-S_1 ~ A-D_{10}
9	1	0	0	1	A-S_1 ~ A-MO_1
A	1	0	1	0	A-S_1 ~ A-MO_{10}
B	1	0	1	1	A-S_1 ~ A-H_{10}, A-W
C	1	1	0	0	A-S_1 ~ A-D_1, A-W
D	1	1	0	1	A-S_1 ~ A-D_{10}, A-W
E	1	1	1	0	A-S_1 ~ A-MO_1, A-W
F	1	1	1	1	A-S_1 ~ A-MO_{10}, A-W

C_C' Register (Control C' Register)

This register is a test register. The user can use it when both the $TEST_1$ (D_0) and $TEST_2$ (D_1) bits of the register are 0. When either or both TEST bits are 1, Oki's test functions are enabled, making the execution results of user's functions unpredictable.

When the register is read, it is automatically cleared. The read value is always 0. When 1 is written in the REST (D_2) bit of the C_E register, the C_C' register is automatically set at 0.

C_D' Register (Control D' Register)

This register sets an interrupt period when the IT/PLS_1 (D_2) bit of the C_D register is 1 and a pulse output period when the bit is 0. The following table shows the relationships between the status of the C_D' register bits and the length of periods.

CY_2	CY_1	CY_0	Period	Duty cycle of the low level when $IT/PLS_1 = 0$
0	0	0	1/1024 s	1/2
0	0	1	1/128 s	1/2
0	1	0	1/64 s	1/2
0	1	1	1/16 s	1/2
1	0	0	1/2 s	1/2
1	0	1	1 s	1/8192
1	1	0	1 min	1/491520
1	1	1	10 min	1/4915200

C_E' Register (Control E' Register)

a) DP (D_0) (Data Protect bit)

This bit has the following two functions:

i) Restricts write operation to the IC.

ii) Prolongs the resetting of the IRQ $FLAG_1$ bit when the bit is read within 122 µs of occurrence of a periodic alarm in the periodic interrupt mode. Also prolongs the resetting the IRQ $FLAG_2$ bit in the same way in the alarm interrupt mode.

i) Restriction of write operation

When the DP bit is 0, normal write operation is enabled. When the bit is 1, however, the IC is write-protected except the BANK 1/0 (D_3) bit of the C_F register for which write operation is always allowed.

The DP bit is designed to protect the registers from extenal noise, particularly erroneous write signal noise which is generated when the standby power supply voltage is switched to the system power supply voltage or vice versa. After the necessary data is written, it is recommended that the DP bit be set at 1 if only read operation is performed.

ii) Prolongation of reset of the IRQ FLAG bits

When the IT/PLS_1 (D_2) bit of the C_D register is 1 (periodic interrupt mode) with the DP bit set at 0, reading the C_E register clears the IRQ $FLAG_1$ bit. This is also true for the IT/PLS_2 (D_3) bit when it is 1 (alarm interrupt mode): reading C_E register clears the IRQ $FLAG_2$ bit.

When the IRQ $FLAG_1$ bit is read within about 122 µs of occurrence of an interrupt with the IT/PLS_1 (D_2) bit of the C_D register set at 1 (periodic interrupt mode), the IRQ $FLAG_1$ bit is not cleared immediately. Similarly, the IRQ $FLAG_2$ bit is not cleared immediately when the IT/PLS_2 (D_3) bit is 1 (alarm interrupt mode). These IRQ FLAG bits are cleared about 122 µs after an interrupt occurs. When these bits are read at least about 122 µs after an interrupt occurs, they are cleared immediately. For more information,

When an IRQ FLAG bits are read mistakenly due to external noise, particularly erroneous read signal noise which is generated when the standby power supply voltage is switched to the system power supply voltage or vice versa, therefore, the IRQ FLAG bits are not cleared immediately but read at the correct times.

When 1 is written in the DP bit, the bit is immediately set at 1 except the following two cases.

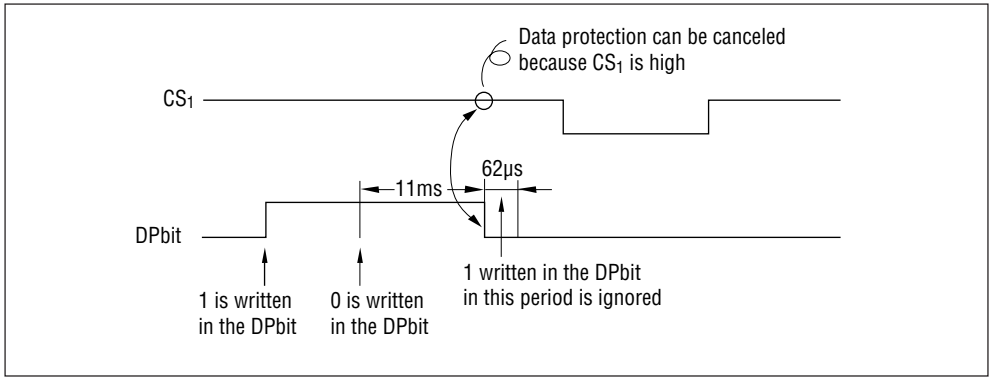
(i) The CS_1 bit is low.

(ii) For 62 µs immediately after the DP bit changes from 1 to 0.

Writing 0 in the DP bit, that is, canceling data protection is allowed only when:

(i) Zero is written in the DP bit more than 2 ms after CS_1 changes from low to high.

(ii) The CS_1 bit is high 11 ms after 0 is written in the DP bit.



b) CAL (D_1) (CALendar)

This bit specifies a range in which the realtime counter is incremented. When the bit is 1, the R-S_1 to R-Y_{10} and R-W register can be incremented. When the bit is 0, the R-S_1 to R-H_{10} and R-W registers can be incremented.

With the CAL bit set at 1, R-D_1 to R-Y_{10} are used as realtime registers. Therefore, setting an impossible time in these registers causes an error. For the bits marked an asterisk (*) of the R-D_{10} and R-MO_{10} registers in the register table, when 1 is written, 0 is automatically set. The alarm comparison range is specified by the A-ENABLE register.

When the CAL bit is 0, the R-D_1 to R-Y_{10} registers are not incremented. They can be used as static RAM, enabling arbitrary values to be set. The bits marked an asterisk (*) of the R-D_{10} and R-MO_{10} registers in the register table can be subject to both write and read operations. The alarm comparison range is specified by the A-ENABLE register. However, the R-D_1 to R-Y_{10} registers are assumed to always provide a match. When these registers are used as static RAM, they cannot be rewritten when the DP bit is 1.

c) 24/12 (D_2) (24-hour clock/12-hour clock)

This bit selects a 24-hour clock or 12-hour clock mode. When the bit is 1, the 24-hour clock mode without PM/AM specification is enabled. When the bit is 0, the 12-hour clock mode with PM or AM specified is enabled.

When the 24/12 bit is rewritten, data in the R-H_1 register and higher will be destroyed. The data needs to be written again.

d) HD/SFT (D_3) (HarDware/SoFTware)(This bit applicable only to the MSM6542-03)

This bit determines which mode, hardware or software, is enabled to validate the stop/start function. When the bit is 1, hardware enables the stop/start function (pin 20). When the bit is 0, software enables the stop/start function (D_2 of the C_F register)

The stop/start function by hardware and that by software cannot be used at the same time.

For the MSM6542-01/02, the stop/start function by software is always enabled due to an internal setting on the IC. However, the HD/SFT bit can be read or written to freely regardless of this setting, enabling the bit to be used as a memo bit.

USAGE

Pattern layout

The oscillation stage of the 32.768 kHz oscillator circuit is at a high impedance to achieve very low power dissipation. In addition, since sine waves are produced at as low as 32.768 kHz, oscillation waves stay near the threshold for a longer time. For this reason, countermeasures must be taken against power supply noise and external noise from the viewpoint of an analog IC.

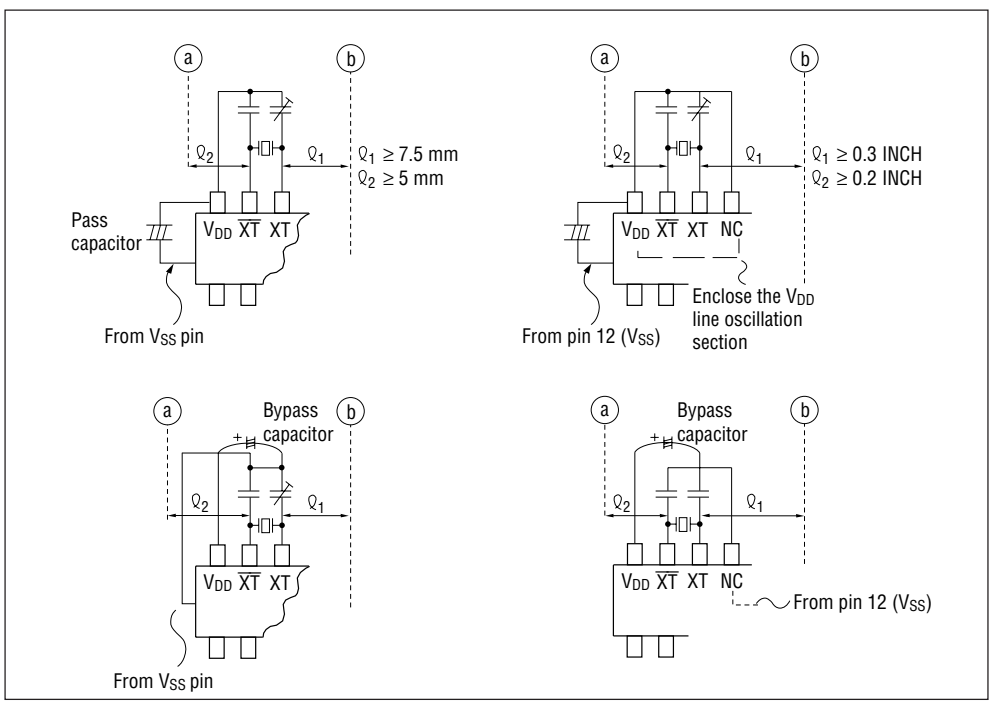
Countermeasures against power supply noise

Insert a 4.7 µF tantalum capacitor and 0.01 µF ceramic capacitor as close to the IC as possible. When another IC (for example, backup RAM) is used in the battery-backed circuit, also insert a by pass capacitor in that IC.

Countermeasures against external noise

Place the crystal for the oscillator circuit and the capacitors as close to the IC as possible. Do not route other signal lines in the oscillator circuit regardless of whether the oscillator circuit is placed on the front or back of the PC board.

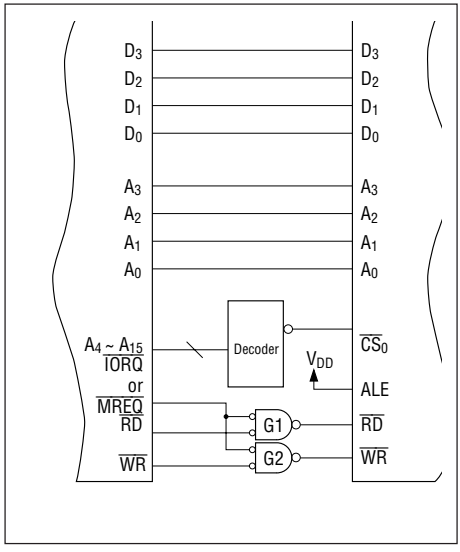
Sufficiently separate the XT and $\overline{XT}$ signal lines from the other signal lines regardless of whether these signal lines are running on the fron or back of the PC board (see a.. and b.. of the figure below).



Sample connection to a microcomputer

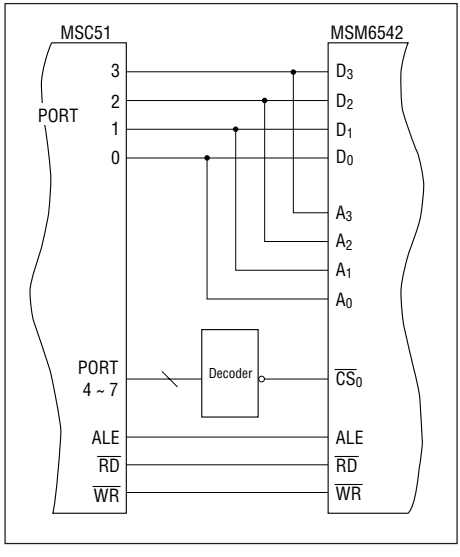
Various microcomputers are upgraded day by day. Updated versions of this data sheet may not be capable of keeping pace with this progress. Check the matching of switching characteristics in advance.

[For the Z80]

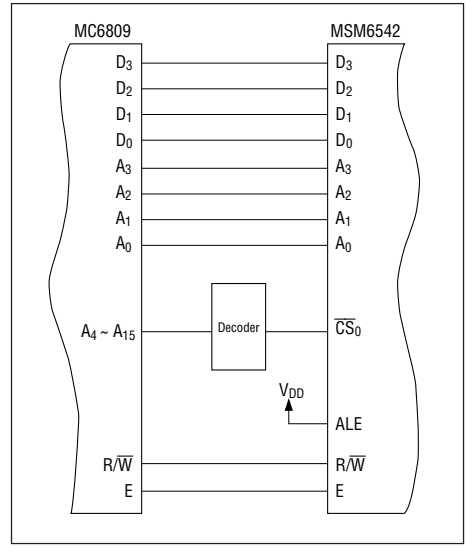


Note: Select either IORQ or MREQ so that the Z80 switching characteristics determined by the crystal oscillator for the Z80 match those of the IC described in this data sheet.

[MCS51]



[MC6809]

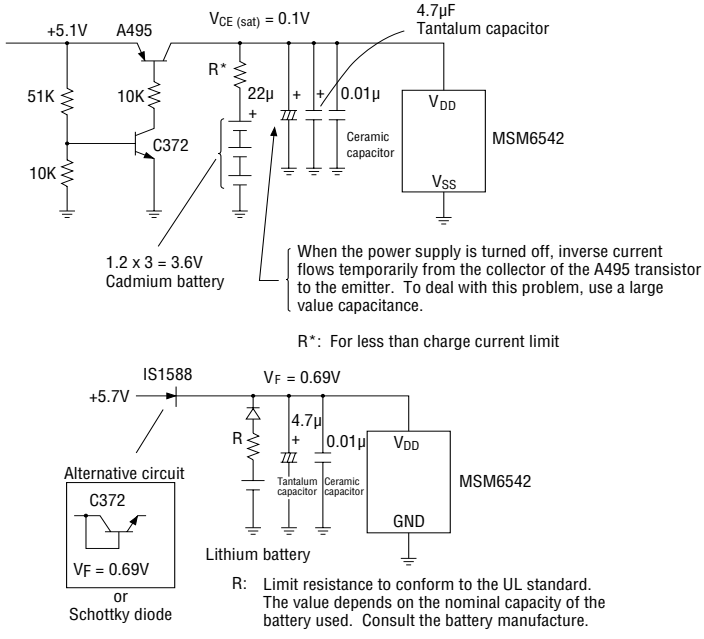


Sample peripheral circuits

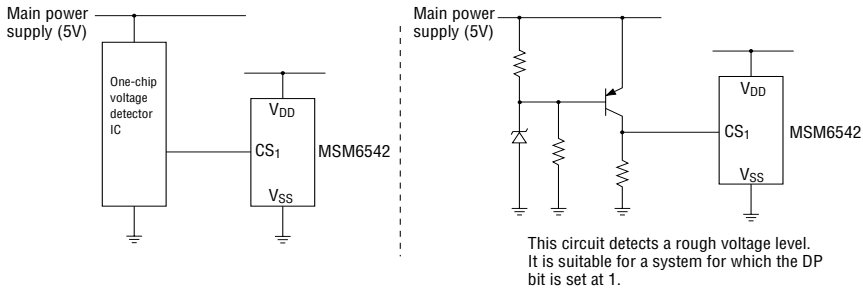
Before using sample peripheral circuits shown below, check them against the user's system.

Power supply circuit (Place a bypass capacitor as close to the IC as possible.)

[When power is supplied from the +5V power supply]

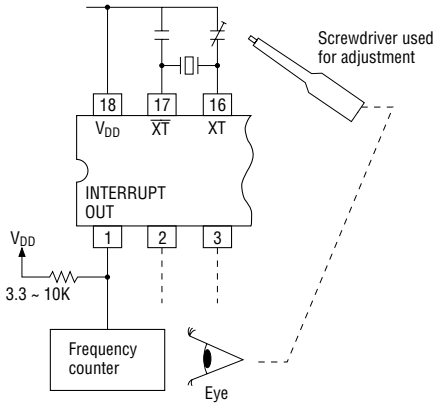


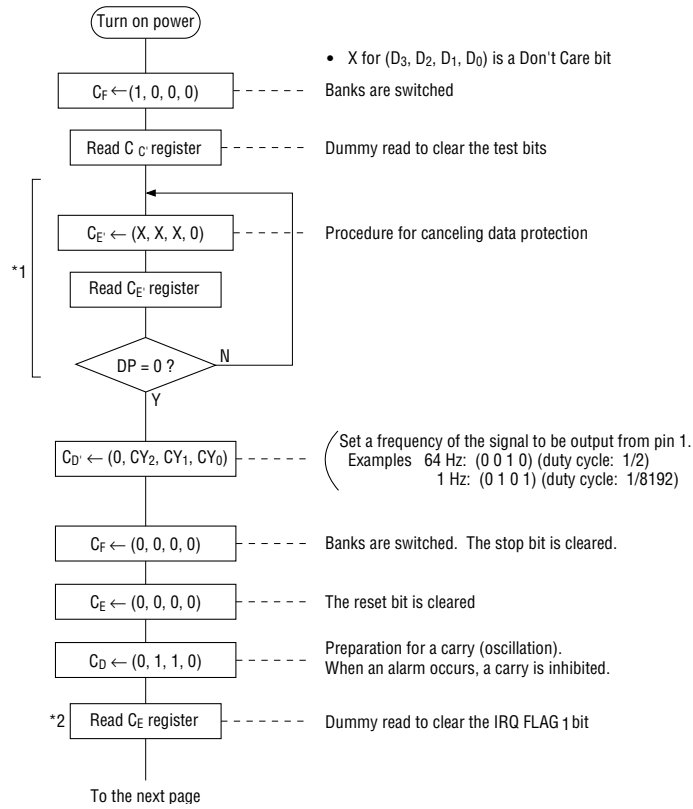
Sample main power supply monitor circuit

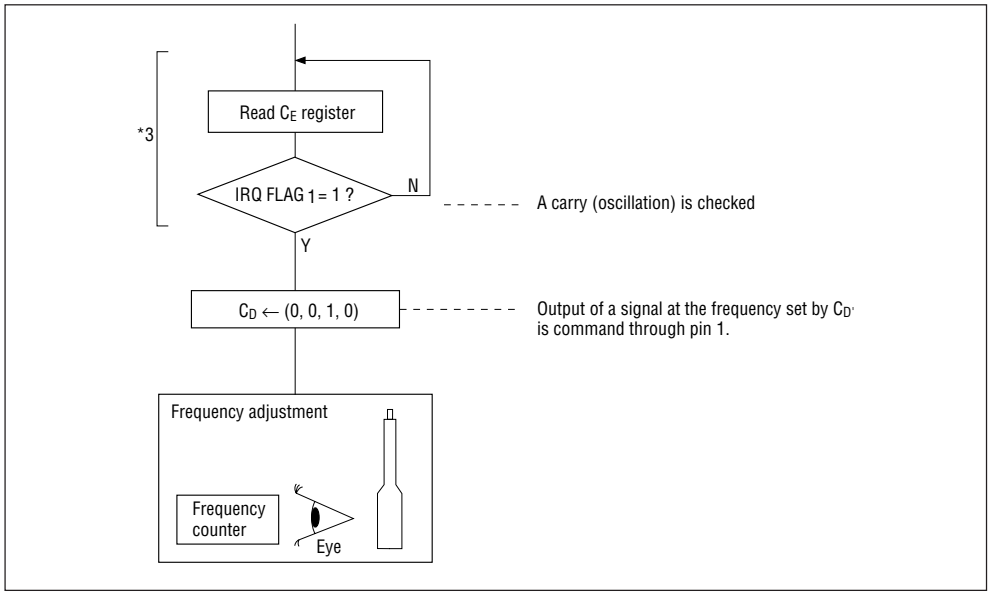


Oscillation frequency adjustment

[For the MSM6542-01/02]







*1 To cancel data protection, oscillation must be in progress. It takes about 13 ms (2 ms during which the writing of DP⇐0 is inhibit in the rising of CS_1 plus 11 ms required until DP = 0 is executed.) This loop includes a wait time before oscillation starts. Usually, the loop takes 0.5 to 2 seconds. When the power is turned on, the value of the DP bit is unpredictable. When the value is 0 incidentally, the loop does not return.

*2, 3 The IRQ $FLAG_1$ is cleared at the step marked *2. If IRQ $FLAG_1$ = 1 is detected in the loop marked *3, therefore, it means that original oscillation is divided.

Other notes

Possible causes why the loop marked *1 or *3 becomes endless

Oscillation waveform at $\overline{XT}$

Yes →
- Incorrect programming
- The frequency counter is not adjusted. Observe the waveform at pin 1 on an oscilloscope.

No →
- Oscillation is impeded by a leak due to a dirty PC board. Clean the PC board.
- The capacitance of the capacitor for oscillation is inadequate. Consult the crystal manufacturer.
- Defective crystal oscillator or IC. Replace it.

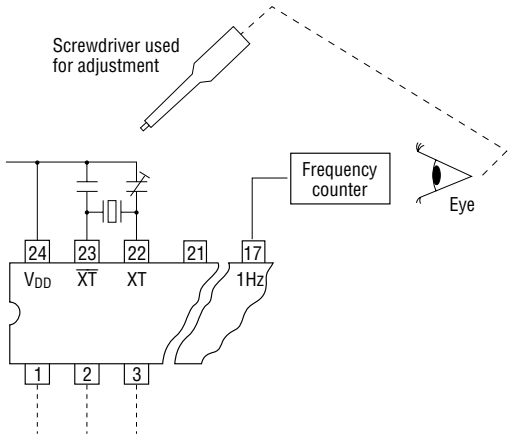
Possible causes when the loop marked *1 or *3 takes a long time (2 or 3 seconds or more)

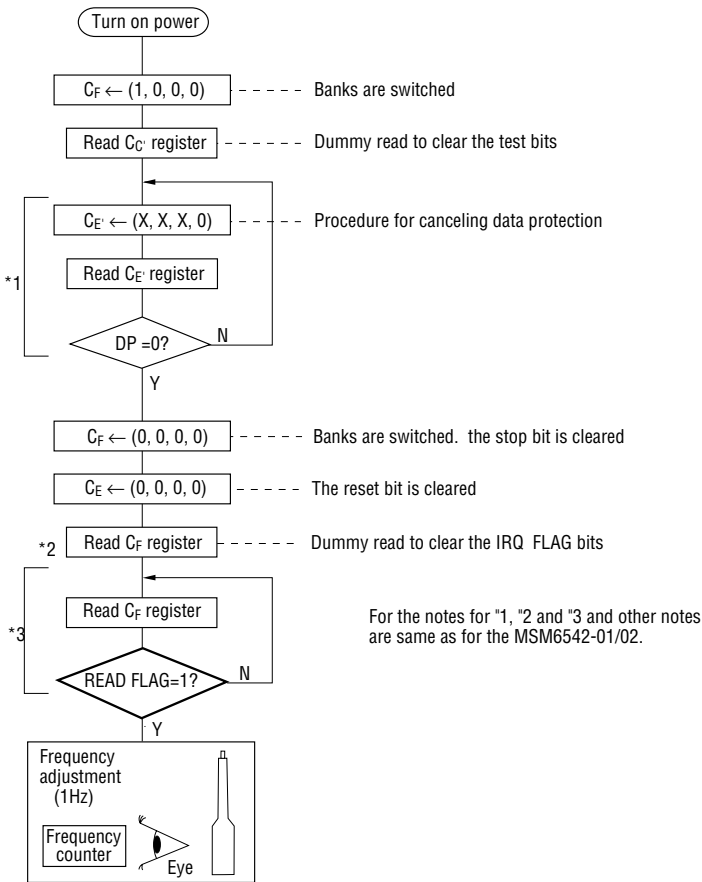
- Oscillation is impeded by a leak due to a dirty PC board. Clean the PC board.
- The capacitance of the capacitor for oscillation is inadequate. Consult the crystal manufactuer.

Possible causes why the frequency counter is not stable.

- The frequency counter is not adjusted. Observe the waveform at pin 1 on an oscilloscope.
- The pattern layout is incorrect. See the description of "Pattern layout." Insert a bypass capacitor having a capacitance of at least 1 µF between the V_{DD} and V_{SS} pins.

For the MSM6542-03





For the notes for "1, "2 and "3 and other notes are same as for the MSM6542-01/02.

Use of CS_1

V_{IH} and V_{IL} of CS_1 has the following three functions:

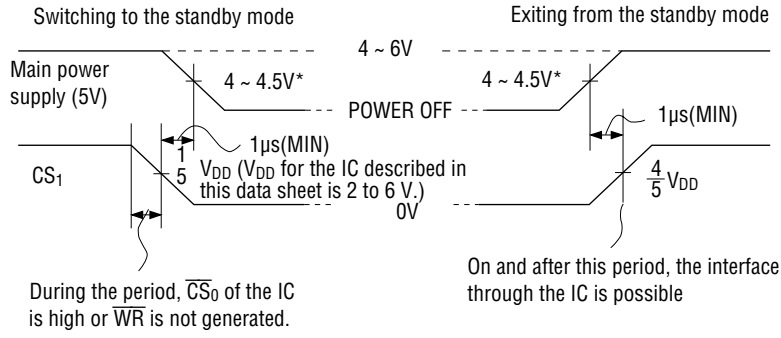
1. Validate the interface with the microcomputer when 5V power is used.
2. Inhibit use of the control bus, data bus, and address bus and prevent through-current specific to CMOS input in the standby mode.
3. Protect register data of the IC when the standby mode is entered or exited.

To implement these functions:

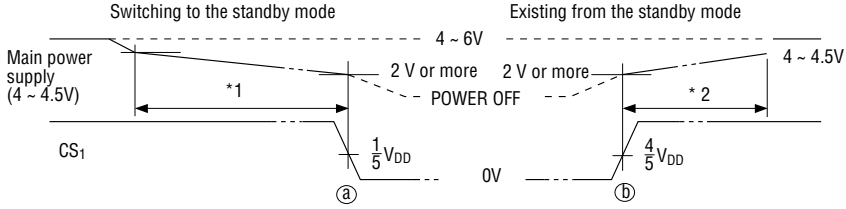
1. To validate the interface with the microcomputer when 5V power is used, input must be at least 4/5 V_{DD}.
2. When the mode is switched to the standby mode, input must be 1/5 V_{DD} or less to inhibit use of the buses. In the standby mode, input must be nearly 0V to prevent through-current.
3. When the standby mode is entered or exited, the main power and CS_1 must conform the following timing charts:

Note: In the standby mode, the operating power supply voltage is from 4V to 2V (minimum value). Clocking is performed but the interface to the outside of the IC is not assured.

When a system is implemented with DP = 0:



When a system is implemented with DP = 1:

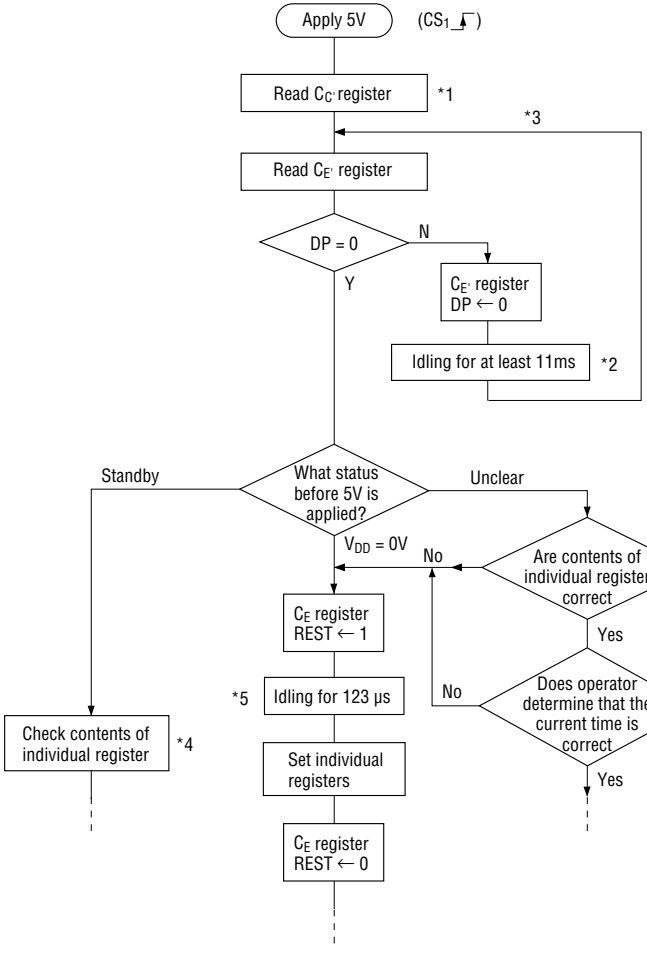


*1, *2:
- The duration in this interval must be 8.7 ms or less.
- Through current at the input stage ($A_0 \sim A_3$, $D_0 \sim D_3$, control inputs) caused by intermediate voltage input level and bus charge current cuaused by not programmed read out operation of CPU will dissipate power source.
  Therefore, it is recommended that the voltage for monitoring the power supply of the CS1 control system be higher than the main power supply/battery switching voltage so that battery backup is enabled only in the interval from ⓐ.. to ⓑ.. .

Reference flowcharts

In the following flowcharts, description of bank switching is omitted.

[Power on sequence when DP is 0]



*1 The test bit is cleared.

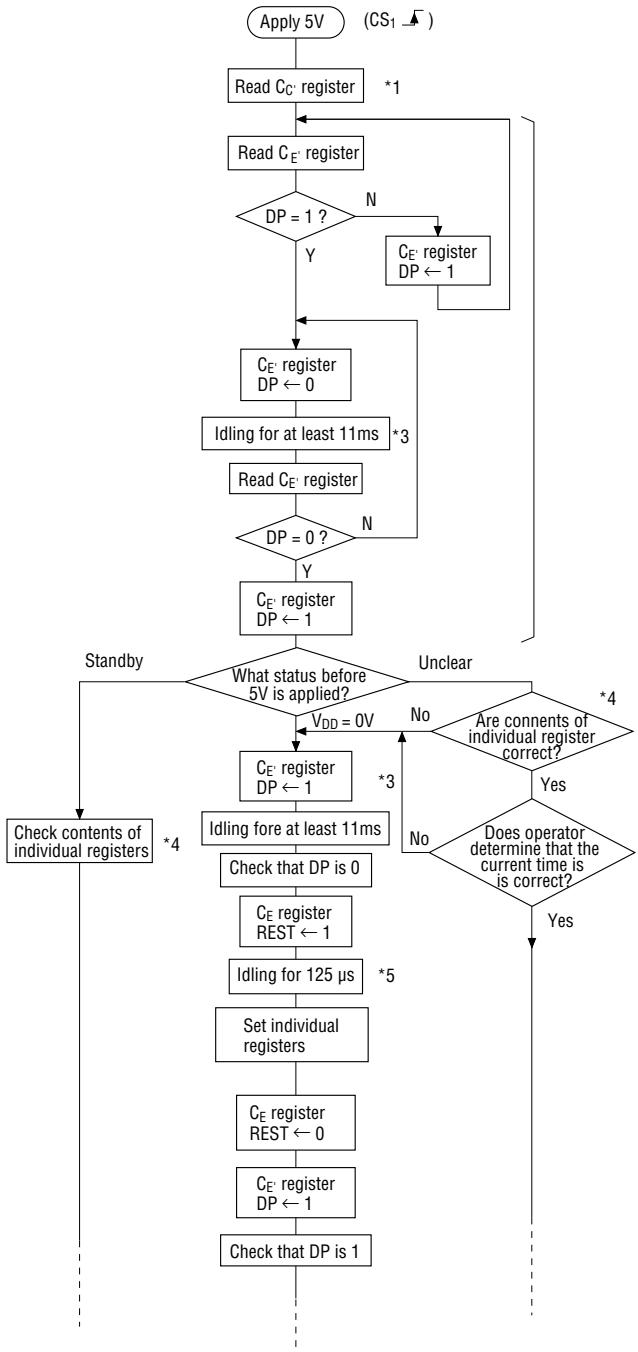
*2 Time until the DP bit becomes 0 under assumption that oscillation is in progress.

*3 When the voltage before 5V is applied is 0V, this loop takes the time equal to the one required to start oscillation. Usually, it takes 0.5 to 2 s.

*4 The contents of R-S, to R-Y_{10} and R-W must be possible values and the values of the other registers must be as expected.

*5 Wait time until a carry which may be generated is completed.

[Power on sequence when DP is 1]



*1 The test bit is cleared.

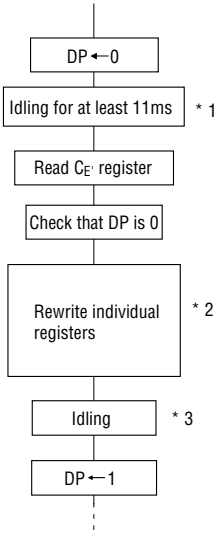
*2 It takes 9 to 11 ms from when 0 is written in the DP bit to when it is set at 0 in the IC. If 0 is written unintentionally in the DP bit during application of 5V power, it may be set at 0. To prevent this, first set the DP bit at 0 then at 1. When the voltage before 5V is applied is 0V, this loop takes the time equal to the one required to start oscillation. Usually, it takes 0.5 to 2 s.

*3 Time until the DP bit becomes 0 under assumption that oscillation is in progress.

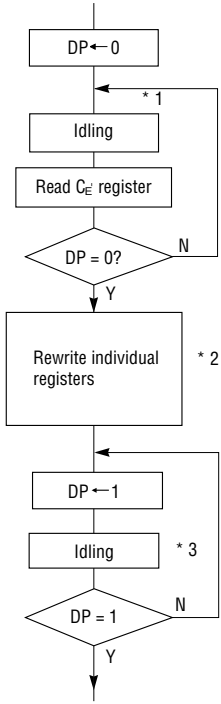
*4 The contents of R-S1, to R-Y10 and R-W must be possible values and the values of the other registers must be as expected.

*5 Wait time until a carry, which may be generated, is completed.

[Temporarily canceling DP = 1 in a system for which DP is set at 1]



OR



*1 Time until the DP bit becomes 0 under assumption that oscillation is in progress.

*2 See "Rewriting individual register."

*3 Writing 1 in it is inhibited for 62 μs after the DP bit is set at 0. This idling is provided to make the DP bit wait to be set at 1.

*1 Processing by other IC or wait time to prevent unnecessary readouts which occur frequently. A measure is 1 ms.

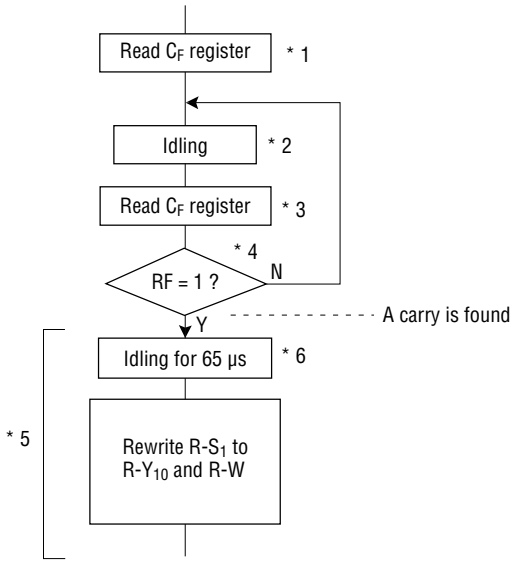
*2 See "Rewriting individual register."

*3 Wait time to prevent unnecessary readouts which occur frequently. A measrue is 10 μs.

[Rewriting individual registers]

When bits other than the BANK 1/0 and DP bits are rewritten, the DP bit must be 0.

(a) R-S_1 to R-Y_{10} and R-W (For the MSM6542-3, 30s adjustment must not be performed through pin 6 during rewriting.)



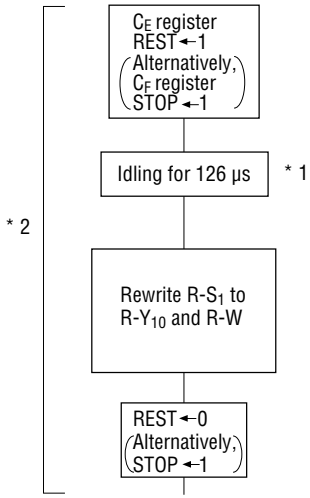
*1 Dummy read to clear the READ FLAG (RF) bit.

*2 Processing by other IC or wait time to prevent unnecessary readouts which occur frequently. A measure is 50 ms.

*3, *4, *5 To assure that rewriting is completed before the next carry is generated, the time required for the step marked *5 must not be longer than 1 s minus time required for steps marked *2 to *4.

*6 Time required for a carry pulse to complete operation

OR



*1 Wait time until a carry which may be generated before 1 is written in the REST (or STOP) bit is completed

*2 When 1 is written in the REST bit, clocking is delayed for the duration during which the less-than-second counter is cleared and clocking is stopped until 0 is written in the REST bit. When 1 is written in the STOP bit, clocking is delayed for the duration during which clocking is stopped initial 0 is written in the STOP bit.

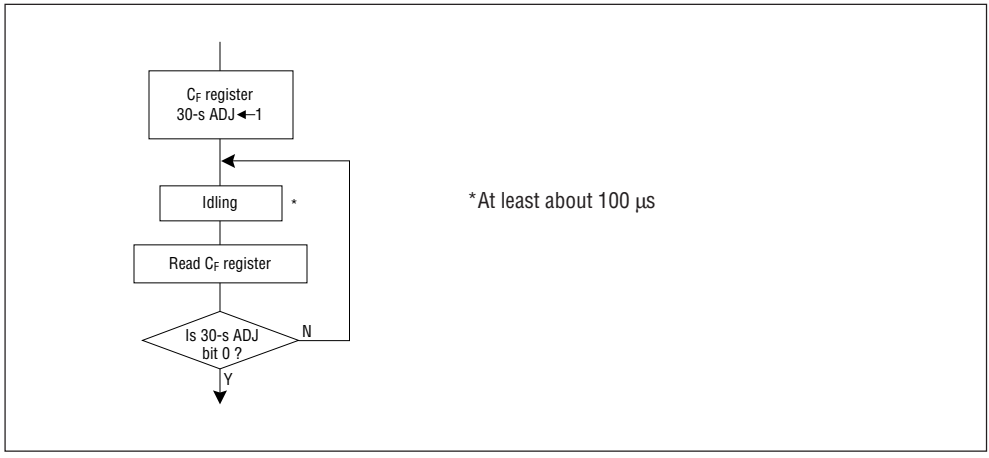
(b)
- R-D_1 to R-Y_{10} when the CAL bit is 0
- $C_{D'}$ REST bit of $C_{E'}$ and C_F (excluding the BANK 1/0 bit)
- A-S_1 to A-M_{10} and A-W
- A-ENABLE and C_D'
- C_E' (excluding the DP bit)
  There is no restriction other than by the DP bit.

(c) BANK 1/0

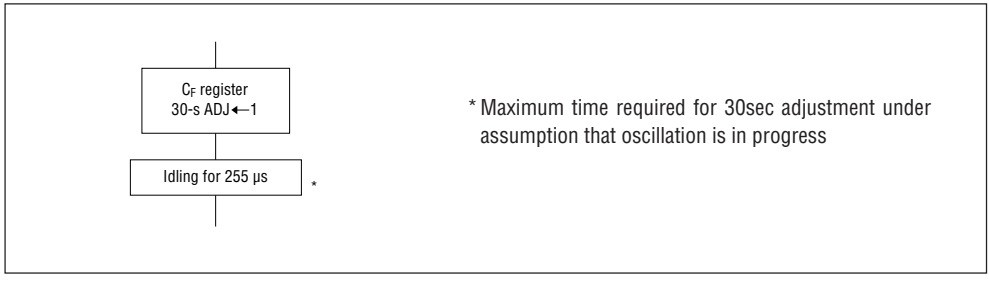
This bit can be rewritten freely even when the DP bit is 1.

(d) 30-s ADJ

Method 1



Method 2



(e) DP

DP ← 1: Rewriting is possible 62 µs after the DP bit changes to 0.

DP ← 0: See "Temporarily canceling DP = 1 is a system for which DP is set at 1."

[Reading individual registers]

(a) Ordingary registers

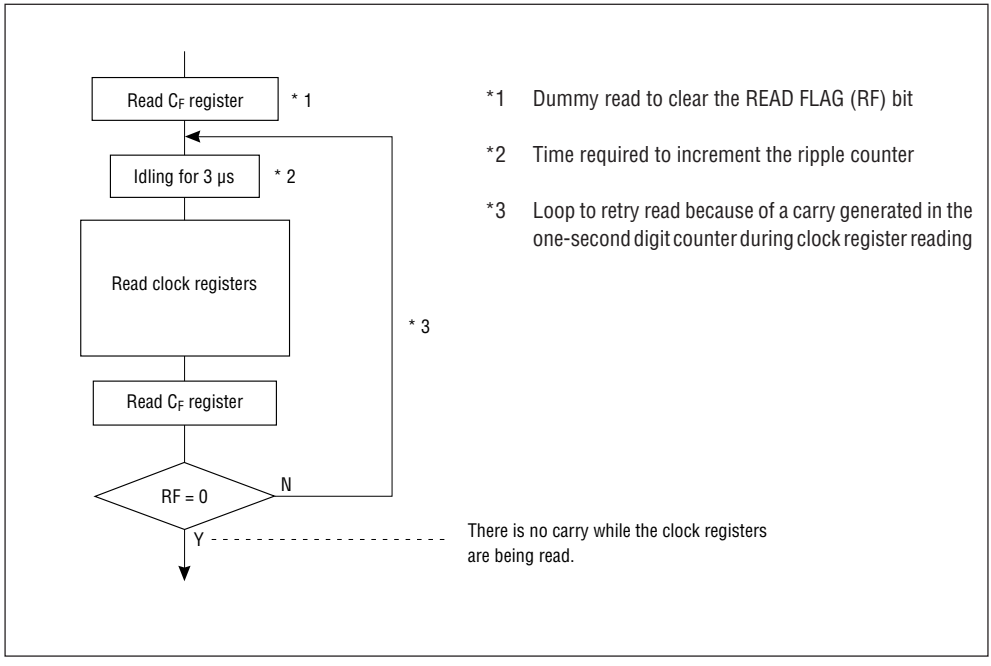
Any registers can be read freely. However, the contents of the following bits change after they are read.

- C_E register

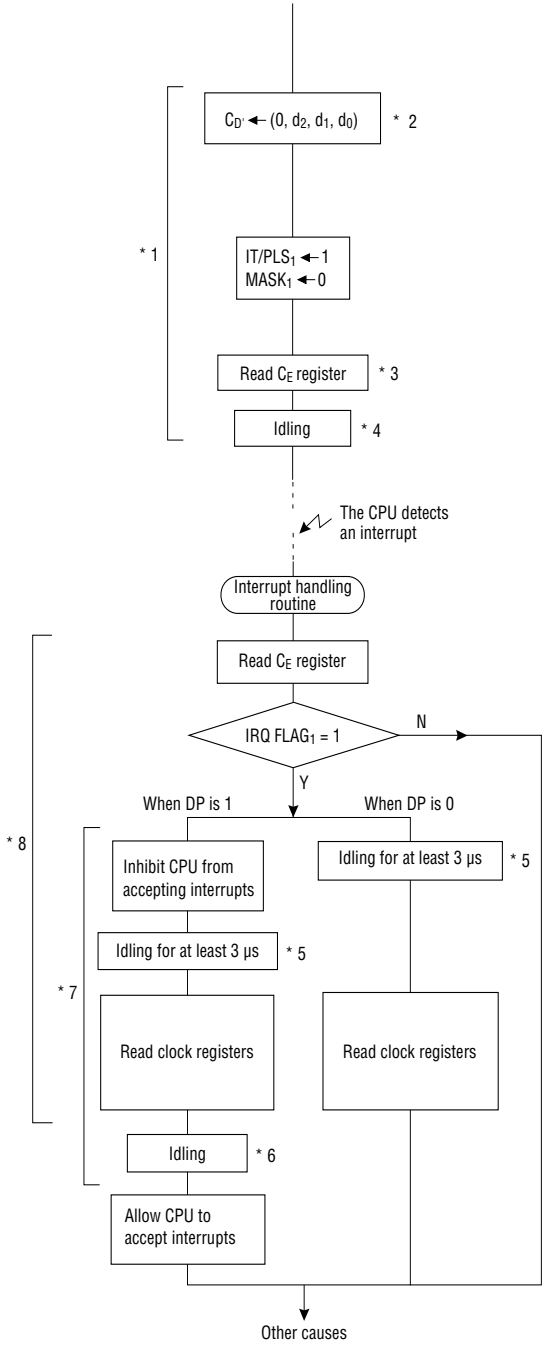
IRQ FLAG$_1$	:	When 1 is read from this bit with IT/PLS$_1$ set at 1, the bit is cleared after read. For the timing when the bit is cleared, see the description of the IRQ FLAG$_1$ bit of the C_E register.
IRQ FLAG$_2$	:	When 1 is read from this bit with IT/PLS$_2$ set at 1, the bit is cleared after read. For the timing when the bit is cleared, see the description of the IRQ FLAG$_2$ bit of the C_E register.
READ FLAG	:	When 1 is read from this bit, the bit is cleared after read.
TEST$_1$, TEST$_2$	:	These bits are reset immediately when they are read. Therefore, 0 is always read from these bits.

(b) Reding time

Method 1 (unscheduled reading)



Method 2 (periodic readout)



*1 Only for initial setting at power on

*2 The values of d2, d1, and d0 depend on the required minimum time unit as follows:

	d2	d1	d0
When up to 1 s is required	1	0	1
When up to 1 min is required	1	1	0
When up to 10 min are required	1	1	1

*3 Dummy read to clear the $IRQ\ FLAG_1$ bit

*4 122 µs when the DP bit is 1,0 µs when the DP bit is 0

*5 Time required to increment the ripple counter

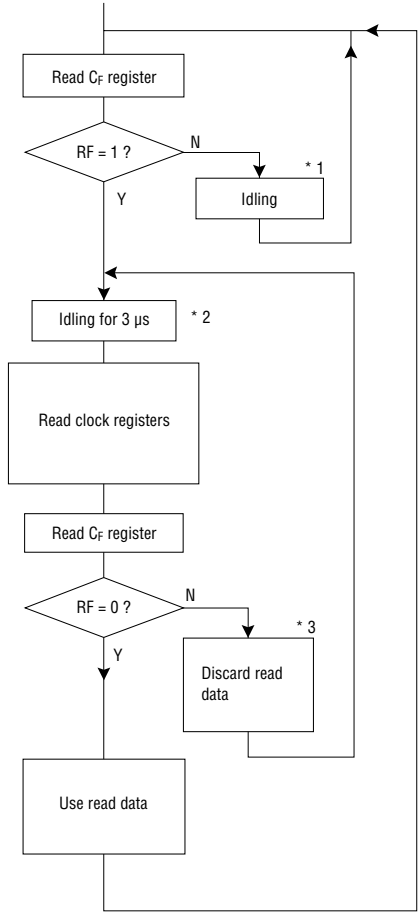
*6, *7 The length of the time must be 122 µs or more because interrupt output is delayed 122 µs due to DP = 1. The idling market *6 is provided for this adjustment.

*8 To assure that readout is completed before the next carry is generated, the time required for these steps must not be longer than the minimum set time unit.

Method 3 (for each second carry)

(a) Setting (d2, d1, d0) at (1, 0, 1) in method 2 (periodical readout) described above

(b) Polling



*1 Processing by other IC or wait time to prevent unnecessary readouts which occur frequently. A measure is 50 ms.

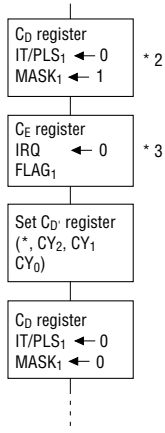
*2 Time required to increment the ripple counter

*3 Loop to retry read because of a carry generated during clock register reading

[Setting for periodic pulse output]

Perform the following setting with the DP bit set at 0. The set values are independent of the setting of the DP bit.

(a) Periodic pulse output (*1)

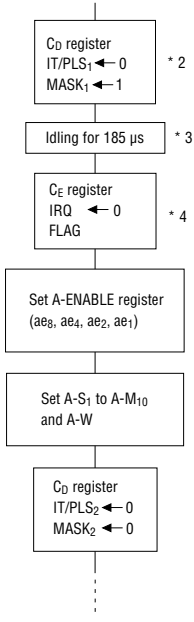


*1 From the viewpoint of software, the IRQ FLAG$_1$ bit is used. From the viewpoint of hardware, pin 1 (PERIODIC OUT) is used for the MSM6542-3 or pin 1 (INTERRUP OUT) for the MSM6542-1/2.

*2 For the MSM6542-1/2, a signal resulting from the ORing with output triggered by an alarm is output to pin 1. When alarm factors are not required, the MASK$_2$ bit must be set at 1.

*3 The IRQ FLAG$_1$ bit is cleared.

(b) Alarm pulse output (*1)



*1 From the viewpoint of software, the IRQ FLAG$_2$ bit is used. From the viewpoint of hardware, pin 2 (ALARM OUT) is used for the MSM6542-3 or pin 1 (INTERRUPT OUT) for the MSM6542-1/2.

*2 For the MSM6542-1/2, a signal resulting from the ORing with output triggered by a periodic carry is output to pin 1. When periodic factors are not required, 1 must be set in the MASK$_1$ bit.

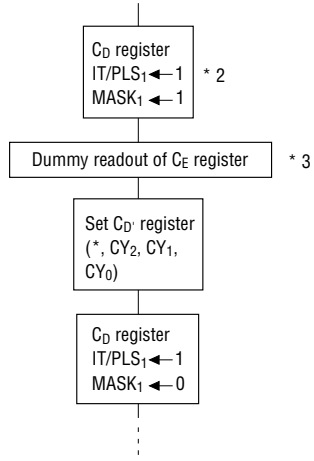
*3 Time required to delete the previous output factors in the IC.

*4 The IRQ FLAG$_2$ bit is cleared.

[Setting interrupt conditions]

Perfomr the following setting with the DP bit set at 0. The set values are independent of the setting of the DP bit.

(a) Periodic interrupt output (*1)

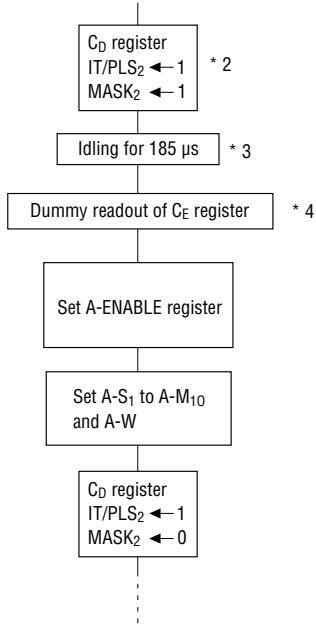


*1 From the viewpoint of software, the IRQ FLAG$_1$ bit is used. From the viewpoint of hardware, pin 1 (PERIODIC OUT) is used for the MSM6542-03 or pin 1 (INTERRUPT OUT) for the MSM6542-01/02.

*2 For the MSM6542-1/2, a signal resulting from the ORing with output triggered by an alarm is output to pin 1. When alarm factors are not required, the MASK$_2$ bit must be set at 1.

*3 The IRQ FLAG$_1$ bit is cleared.

(b) Alarm interrup output (*1)



*1 From the viewpoint of software, the IRQ FLAG$_2$ bit is used. From the viewpoint of hardware, pin 3 (ALARM OUT) is used for the MSM6542-03 or pin 1 (INTERRUPT OUT) for the MSM6542-01/02.

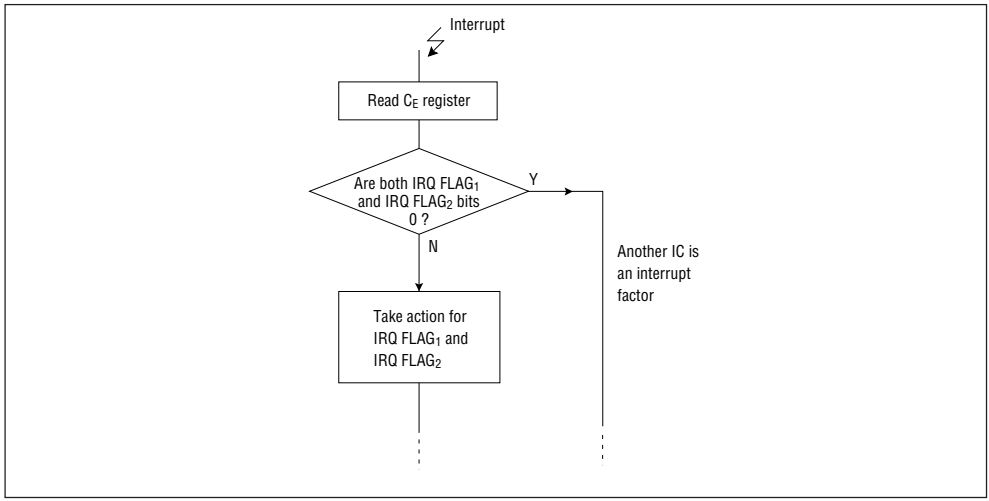
*2 For the MSM6542-01/02, a signal resulting from the ORing with output triggered by a periodic carry is output to pin 1. When periodic factors are not required, 1 must be set in the MASK$_1$ bit.

*3 Time required to output the previous interrupt factors

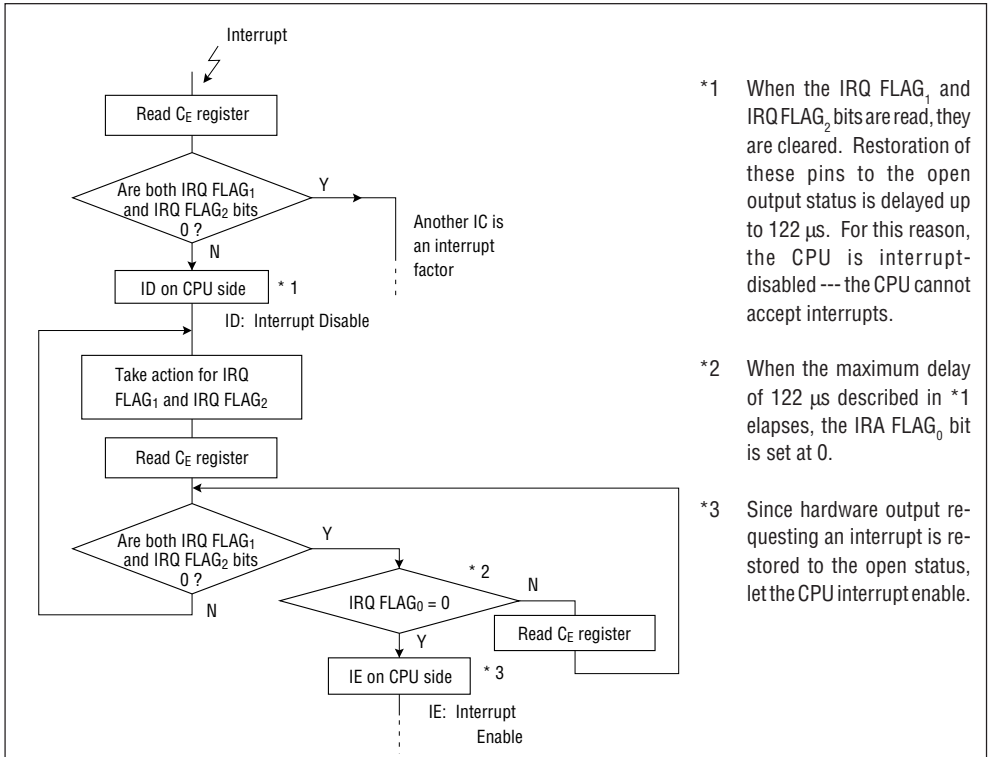
*4 The IRQ FLAG$_2$ bit is cleared.

[Sensing interrupts]

(a) When the DP bit is 0



(b) When the DP bit is 1



*1 When the IRQ $FLAG_1$ and IRQ $FLAG_2$ bits are read, they are cleared. Restoration of these pins to the open output status is delayed up to 122 µs. For this reason, the CPU is interrupt-disabled --- the CPU cannot accept interrupts.

*2 When the maximum delay of 122 µs described in *1 elapses, the IRA $FLAG_0$ bit is set at 0.

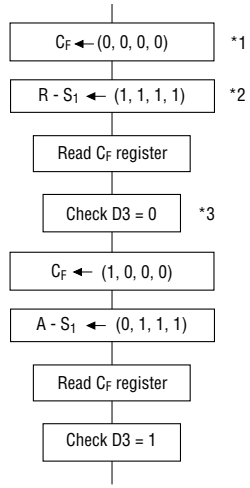
*3 Since hardware output requesting an interrupt is restored to the open status, let the CPU interrupt enable.

[Basic check at the early stage of development]

(a) Read/write check

Only the BANK 1/0 bit can be subject to read and write operations without a paritcular procedure.

The interface can be checked by reading and writing the BANK 1/0 bit.



*1 (D3, D2, D1, D0)

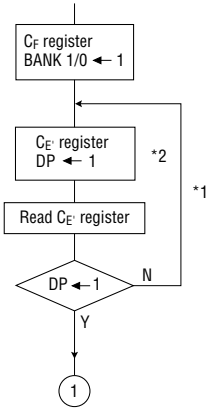
*2 Use addresses and data having values opposite to those in *1 above to charge or discharge the bus in the reverse phase.

*3 D3 is the BANK 1/0 bit.

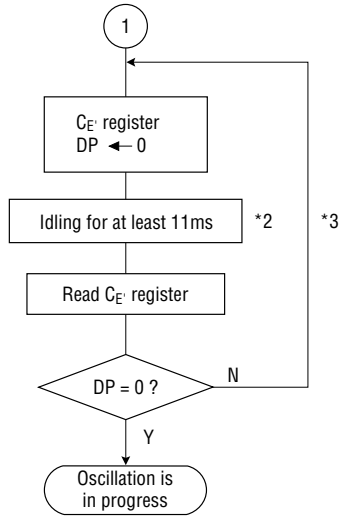
*4 Same idea as *2

(b) Checking oscillation using software

Oscillator operation can be checked using software through increment of clock registers, change of the IRQ $FLAG_1$ and IRQ $FLAG_2$ bits, 30-s adjustment, change of the read flag, and setting the DP bit at 0. These methods, except setting the DP bit at 0, affect the REST and STOP bits. Therefore, the method involved in the DP is used in the following flowcharts:



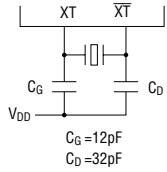
*1, *2 The DP bit is not set at 1 for 62 µs after it changes from 1 to 0. When the step marked *2 is executed within the 62µs interval but oscillation is in progress, the loop marked *1 is completed within 62 µs.



*2 Time until the DP bit becomes 0 under assumption that oscillation is in progress.

*3 The time required for this loop is prolonged by the time equal to the one required to start oscillation. Usually, this time is 0.5 to 2 s.

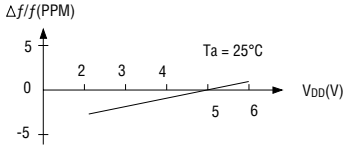
Reference experimental data



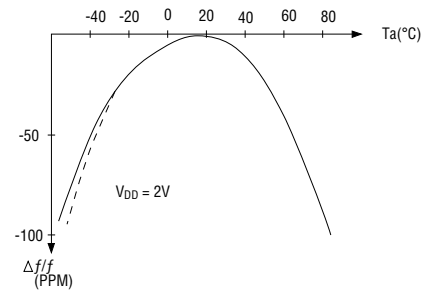
Crystral oscillator: P3 manufactured by Kinseki Co., Ltd.
(32.768 kHz)
Load capacity: CL=12pF
Equivalent series resistance: 30kΩ (MAX)
Secondary temperature coefficient of frequency
characteristics: -4.2 x 10^{-8} /°C (MAX)

Note: The temperature characteristics of the capacitors used are class 0.

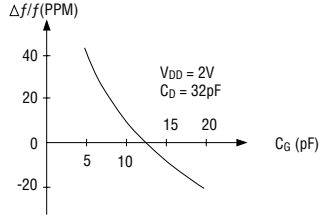
o Dependency of oscillation frequency on power supply voltages



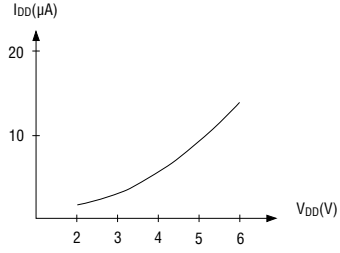
o Dependency of oscillation frequency on temperatures



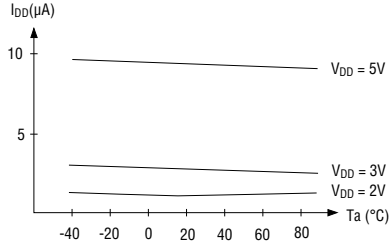
o Dependency of oscillation frequencies on capacitance



o Dependency of I_{DD} on power supply voltages (Ta = 25°C)

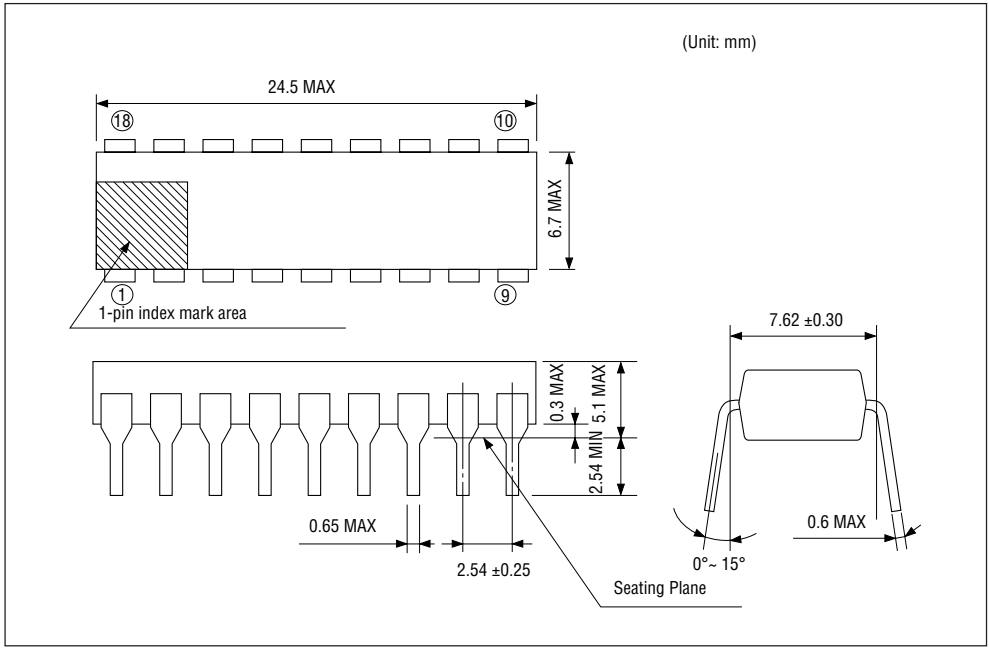


o Dependency of I_{DD} on ambient temperatures

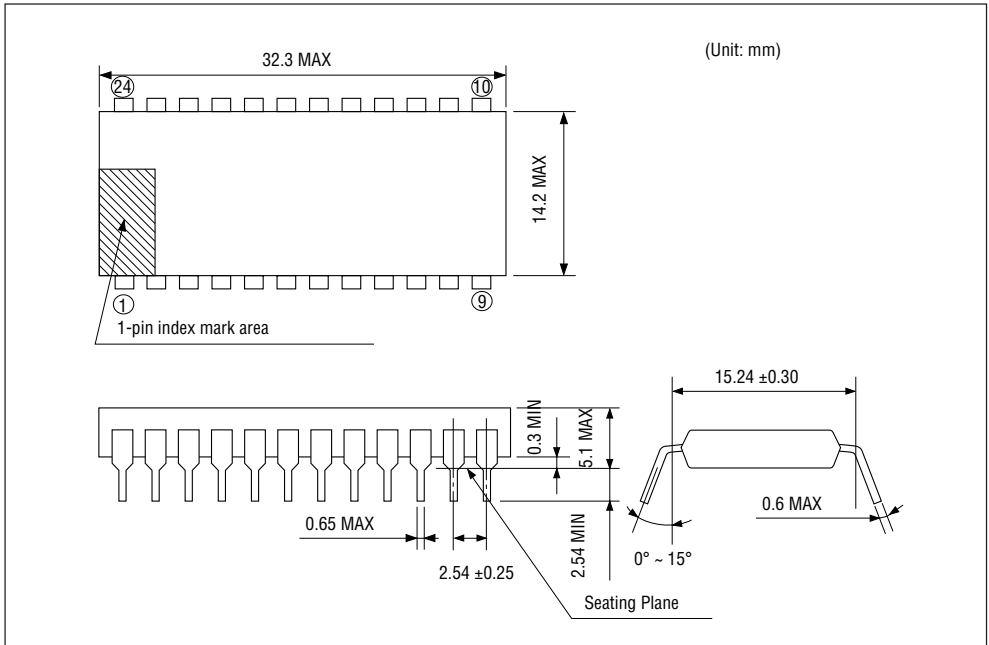


PACKAGE DIMENSIONS

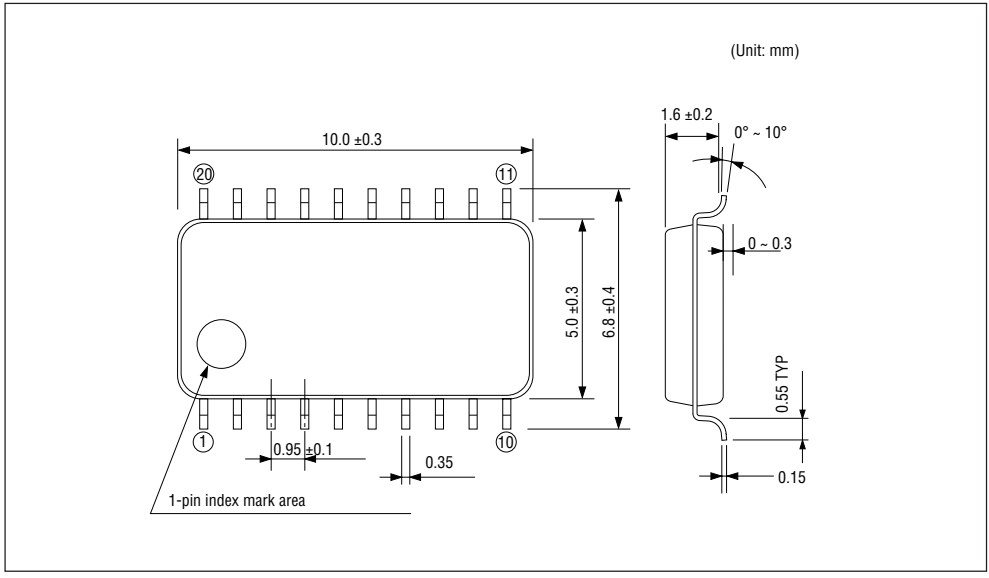
18-pin plastic DIP



24-pin plastic DIP



20-pin plastic flat



24-pin plastic flat