19-1552; Rev 0; 10/99

MAXIM

Ultra-Low-Distortion, Single-Supply, 300MHz Op Amps with Enable

MAX4265–MAX4270

General Description

The MAX4265–MAX4270 single-supply, voltage-feedback op amps are capable of driving a 100Ω load while maintaining ultra-low distortion over a wide bandwidth. They offer superior spurious-free dynamic range (SFDR) performance: -90dBc or better at frequencies below 5MHz and -60dBc at a 100MHz frequency. Additionally, input voltage noise density is 8nV/√Hz while operating from a single +4.5V to +8.0V supply or from dual ±2.25V to ±4.0V supplies. These features make the MAX4265–MAX4270 ideal for use in high-performance communications and signal-processing applications that require low distortion and wide bandwidth.

The MAX4265 single and MAX4268 dual unity-gain-stable amplifiers have up to a 300MHz gain-bandwidth product. The MAX4266 single and MAX4269 dual amplifiers have up to a 350MHz bandwidth at a minimum stable gain of +2V/V. The MAX4267 single and MAX4270 dual amplifiers have a 200MHz bandwidth at a minimum stable gain of +5V/V.

For additional power savings, these amplifiers feature a low-power disable mode that reduces supply current to 1.6mA and places the outputs in a high-impedance state. The MAX4265/MAX4266/MAX4267 are available in a space-saving 8-pin µMAX package, and the MAX4268/MAX4269/MAX4270 are available in a 16-pin QSOP package.

Applications

Base-Station Amplifiers
IF Amplifiers
High-Frequency ADC Drivers
High-Speed DAC Buffers
RF Telecom Applications
High-Frequency Signal Processing

Pin Configurations appear at end of data sheet.

Selector Guide

PART	NO. OF OP AMPS	MIN GAIN (V/V)	BANDWIDTH (MHz)
MAX4265	1	1	300
MAX4266	1	2	350
MAX4267	1	5	200
MAX4268	2	1	300
MAX4269	2	2	350
MAX4270	2	5	200

Features

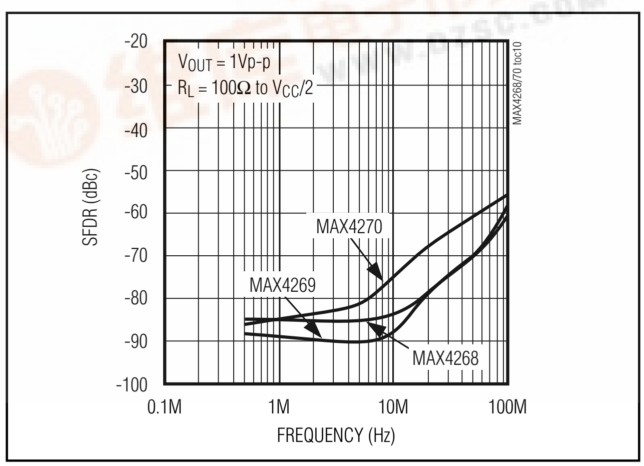
- ♦ +4.5V to +8.0V Single-Supply Operation
- ♦ Superior SFDR with 100Ω Load
  - -90dBc (f_C = 5MHz)
  - -60dBc (f_C = 100MHz)
- ♦ 35dBm IP3 (f_C = 20MHz)
- ♦ 8nV/√Hz Voltage Noise Density
- ♦ 100MHz 0.1dB Gain Flatness (MAX4268)
- ♦ 900V/µs Slew Rate
- ♦ ±45mA Output Driving Capability
- ♦ Shutdown Mode Places Outputs in High-Impedance State

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4265EUA*	-40°C to +85°C	8 µMAX
MAX4265ESA*	-40°C to +85°C	8 SO
MAX4266EUA*	-40°C to +85°C	8 µMAX
MAX4266ESA*	-40°C to +85°C	8 SO
MAX4267EUA*	-40°C to +85°C	8 µMAX
MAX4267ESA*	-40°C to +85°C	8 SO
MAX4268EEE	-40°C to +85°C	16 QSOP
MAX4268ESD	-40°C to +85°C	14 SO
MAX4269EEE	-40°C to +85°C	16 QSOP
MAX4269ESD	-40°C to +85°C	14 SO
MAX4270EEE	-40°C to +85°C	16 QSOP
MAX4270ESD	-40°C to +85°C	14 SO

**Future product—contact factory for availability.*

SFDR vs. Input Frequency



Ultra-Low-Distortion, Single-Supply, 300MHz Op Amps with Enable

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})..+8.5V
Voltage on Any Other Pin ....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Short-Circuit Duration (V_{OUT} to V_{CC} or V_{EE}) ....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.33mW/°C above +70°C)........667mW
8-Pin μMAX (derate 4.10mW/°C above +70°C) 330mW
8-Pin SO (derate 5.9mW/°C above +70°C).................471mW
14-Pin SO (derate 8.33mW/°C above +70°C)............667mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0, R_L = 100Ω to V_{CC}/2, V_{CM} = V_{CC}/2, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC}	Inferred from PSRR test	4.5		8.0	V
Common-Mode Input Voltage	V_{CM}	Inferred from CMRR test	V_{EE} + 1.6		V_{CC} - 1.6	V
Input Offset Voltage	V_{OS}			1	9	mV
Input Offset Voltage Drift	TCV_{OS}			1.5		μV/°C
Input Offset Voltage Channel Matching		MAX4268/MAX4269/MAX4270		1		mV
Input Bias Current	I_B			3.5	40	μA
Input Offset Current	I_{OS}			0.1	5.5	μA
Common-Mode Input Resistance	R_{INCM}	Either input, (V_{EE} + 1.6) ≤ V_{CM} ≤ (V_{CC} - 1.6)		1		MΩ
Differential Input Resistance	R_{INDIFF}	-10mV ≤ V_{IN} ≤ 10mV		40		kΩ
Common-Mode Rejection Ratio	CMRR	(V_{EE} + 1.6V) ≤ V_{CM} ≤ (V_{CC} - 1.6V), no load	60	85		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.5V to 8.0V	60	85		dB
Open-Loop Voltage Gain	A_{OL}	1.75V ≤ V_{OUT} ≤ 3.25V	60	95		dB
Output Voltage Swing	V_{OUT}	V_{CC} - V_{OH}, V_{OL} - V_{EE}		1.1	1.5	dB
Output Current Drive	I_{OUT}	R_L = 20Ω	±30	±45		mA
Output Short-Circuit Current	I_{SC}	Sinking or sourcing to V_{CC} or V_{EE}		100		mA
Closed-Loop Output Resistance	R_{OUT}			0.035		Ω
Power-Up Time	t_{PWRUP}	V_O = 1V step, 0.1% settling time		10		μs
Quiescent Supply Current	I_S	Normal mode, EN_ = 5V or floating		28	32	mA
		Disable mode, EN_ = 0		1.6	5	
Disable Output Leakage Current		$V_{EN\_}$ = 0, V_{EE} ≤ V_{OUT} ≤ V_{CC}		0.2	5	μA
EN_ Logic Low Threshold					V_{CC} - 3.5	V
EN_ Logic High Threshold			V_{CC} - 1.5			V
EN_ Logic Input Low Current		$V_{EN\_}$ = 0		5	100	μA
EN_ Logic Input High Current		$V_{EN\_}$ = 5V		1	30	μA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0, R_L = 100Ω to $V_{CC}/2$, V_{CM} = $V_{CC}/2$, MAX4265/MAX4268 A_V = +1V/V, MAX4266/MAX4269 A_V = +2V/V, MAX4267/MAX4270 A_V = +5V/V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{-3dB}	V_{OUT} = 100mVp-p	MAX4265/MAX4268		300		MHz
			MAX4266/MAX4269		350		
			MAX4267/MAX4270		200		
Full-Power Bandwidth	FPBW	V_{OUT} = 1Vp-p	MAX4265/MAX4268		175		MHz
			MAX4266/MAX4269		200		
			MAX4267/MAX4270		200		
0.1dB Gain Flatness	$BW_{0.1dB}$	V_{OUT} = 100mVp-p	MAX4265/MAX4268		100		MHz
			MAX4266/MAX4269		35		
			MAX4267/MAX4270		35		
All-Hostile Crosstalk		f = 10MHz			85		dB
Slew Rate	SR	V_{OUT} = 1V step			900		V/µs
Rise/Fall Times	t_R, t_F	V_{OUT} = 1V step			1		ns
Settling Time (0.1%)	$t_{S,0.1}$	V_{OUT} = 1V step			15		ns
Spurious-Free Dynamic Range	SFDR	V_{OUT} = 1Vp-p (MAX4269)	f_C = 1MHz		88		dBc
			f_C = 5MHz		90		
			f_C = 10MHz		87		
			f_C = 20MHz		78		
			f_C = 60MHz		68		
			f_C = 100MHz		60		
Second Harmonic Distortion		V_{OUT} = 1Vp-p (MAX4269)	f_C = 1MHz		88		dBc
			f_C = 5MHz		90		
			f_C = 10MHz		87		
			f_C = 20MHz		78		
			f_C = 60MHz		68		
			f_C = 100MHz		60		
Third Harmonic Distortion		V_{OUT} = 1Vp-p (MAX4269)	f_C = 1MHz		96		dBc
			f_C = 5MHz		95		
			f_C = 10MHz		92		
			f_C = 20MHz		86		
			f_C = 60MHz		72		
			f_C = 100MHz		68		

Ultra-Low-Distortion, Single-Supply, 300MHz Op Amps with Enable

AC ELECTRICAL CHARACTERISTICS (continued)

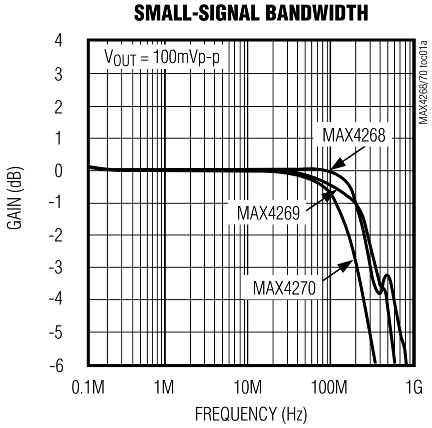
(V_{CC} = +5V, V_{EE} = 0, R_L = 100Ω to V_{CC}/2, V_{CM} = V_{CC}/2, MAX4265/MAX4268 A_V = +1V/V, MAX4266/MAX4269 A_V = +2V/V, MAX4267/MAX4270 A_V = +5V/V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Two-Tone, Third-Order Intercept Distortion	IP3	V_{OUT} = 1Vp-p, f_{CA} = 20MHz, f_{CB} = 21.25MHz (MAX4269)			35		dBm
Input -1dB Compression Point		f_C = 20MHz			12		dBm
Differential Gain	D_G	NTSC, f = 3.58MHz, R_L = 150Ω to V_{CC}/2			0.015		%
Differential Phase	D_P	NTSC, f = 3.58MHz, R_L = 150Ω to V_{CC}/2			0.03		degrees
Input Capacitance	C_{IN}				2		pF
Output Impedance	R_{OUT}	f = 10MHz			1		Ω
Disabled Output Capacitance		$V_{EN\_}$ = 0			5		pF
Enable Time	t_{EN}	V_{IN} = 1V			100		ns
Disable Time	t_{DIS}	V_{IN} = 1V			750		µs
Capacitive Load Stability		No sustained oscillation	MAX4265/MAX4268		15		pF
			MAX4266/MAX4269		15		
			MAX4267/MAX4270		22		
Input Voltage Noise Density	e_n	f = 1kHz			8		nV/√Hz
Input Current Noise Density	i_n	f = 1kHz			1		pA/√Hz

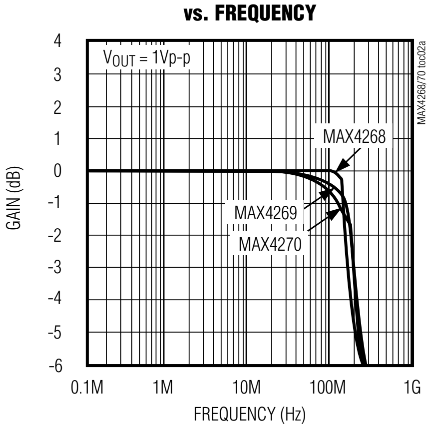
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0, EN_ = 5V, R_L = 100Ω to V_{CC}/2, MAX4268 A_V = +1V/V, MAX4269 A_V = +2V/V, MAX4270 A_V = +5V/V, T_A =+25°C, unless otherwise noted.)

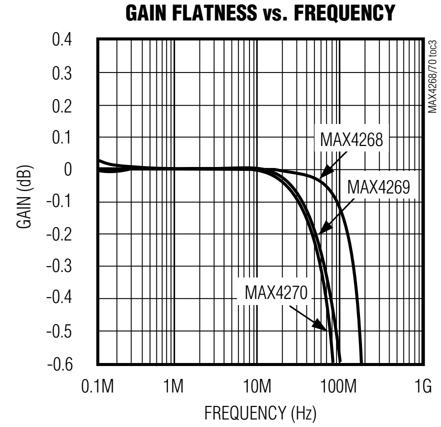
SMALL-SIGNAL BANDWIDTH



LARGE-SIGNAL GAIN vs. FREQUENCY



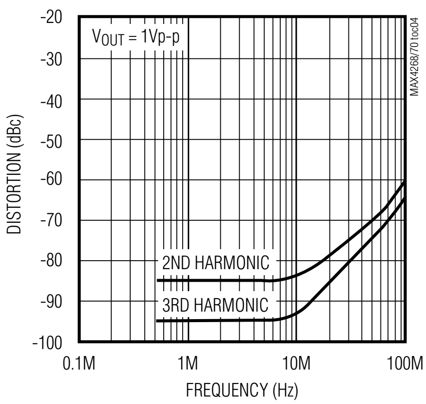
GAIN FLATNESS vs. FREQUENCY



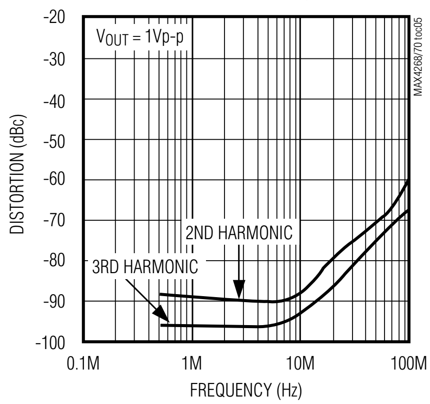
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, EN_ = 5V, R_L = 100Ω to V_{CC}/2, MAX4268 A_V = +1V/V, MAX4269 A_V = +2V/V, MAX4270 A_V = +5V/V, T_A =+25°C, unless otherwise noted.)

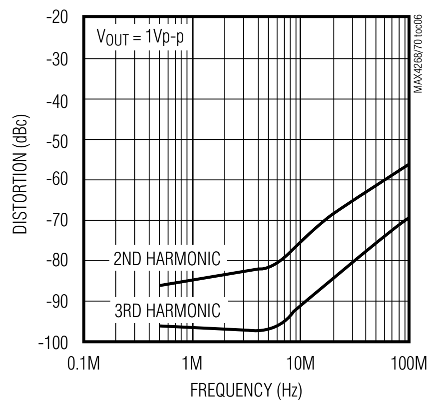
MAX4268
DISTORTION vs. FREQUENCY



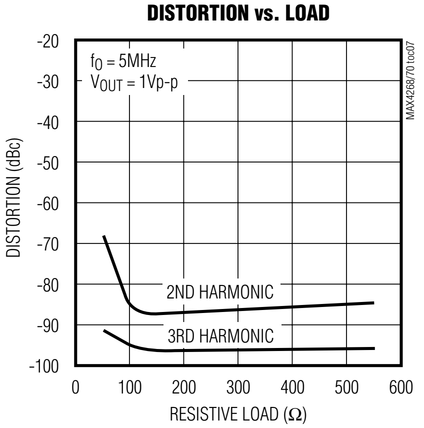
MAX4269
DISTORTION vs. FREQUENCY



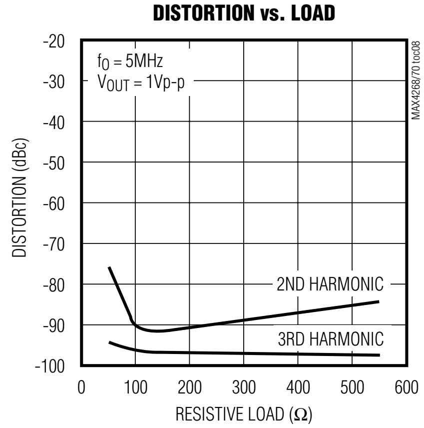
MAX4270
DISTORTION vs. FREQUENCY



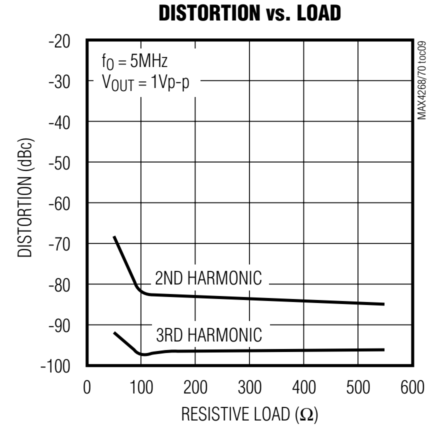
MAX4268
DISTORTION vs. LOAD



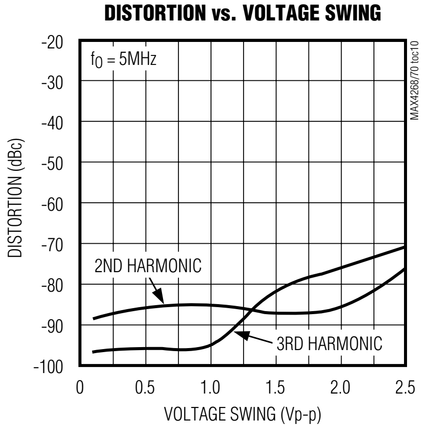
MAX4269
DISTORTION vs. LOAD



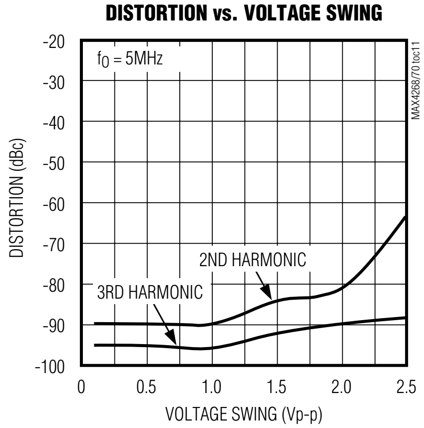
MAX4270
DISTORTION vs. LOAD



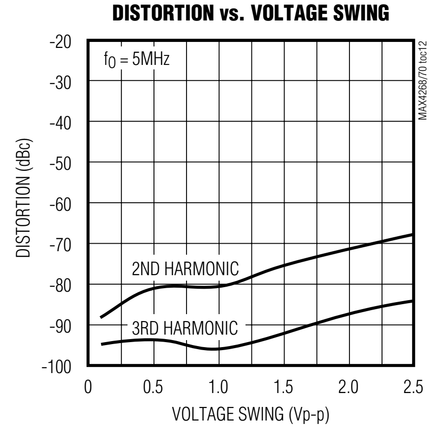
MAX4268
DISTORTION vs. VOLTAGE SWING



MAX4269
DISTORTION vs. VOLTAGE SWING



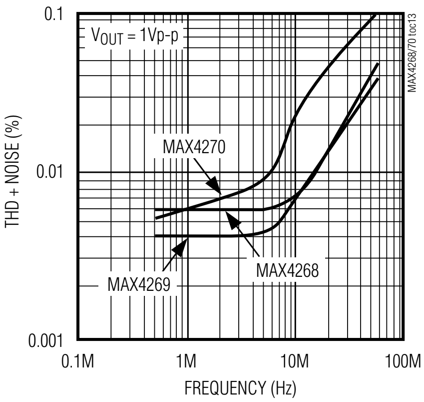
MAX4270
DISTORTION vs. VOLTAGE SWING



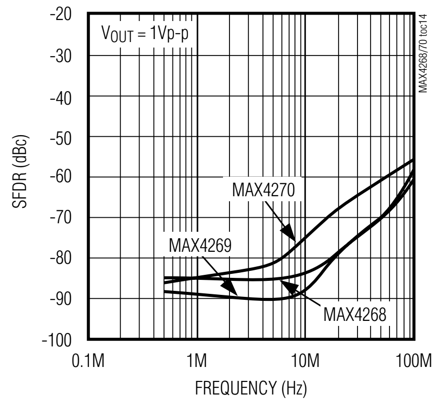
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, EN_ = 5V, R_L = 100Ω to V_{CC}/2, MAX4268 A_V = +1V/V, MAX4269 A_V = +2V/V, MAX4270 A_V = +5V/V, T_A =+25°C, unless otherwise noted.)

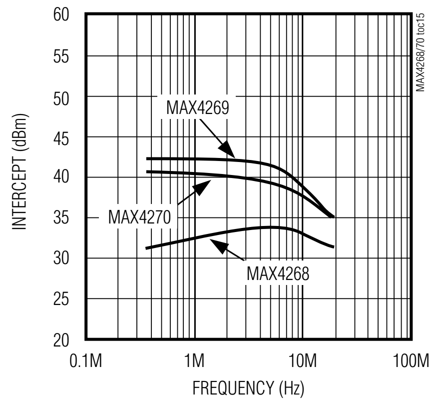
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



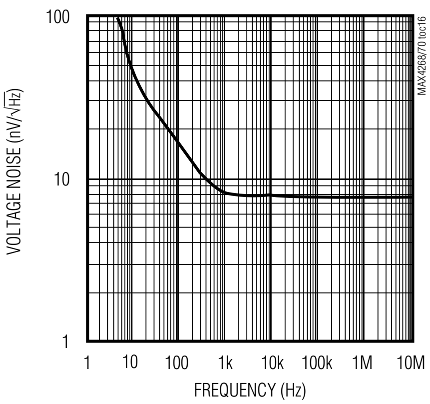
SPURIOUS-FREE DYNAMIC RANGE vs. FREQUENCY



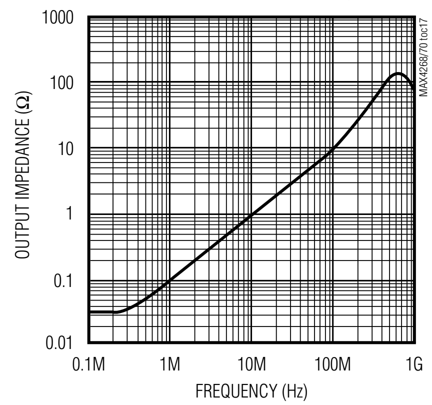
TWO-TONE THIRD-ORDER INTERCEPT vs. FREQUENCY



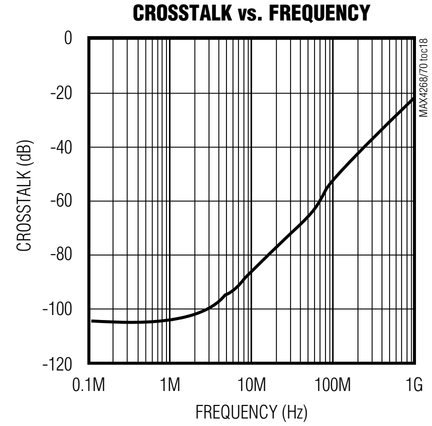
VOLTAGE NOISE vs. FREQUENCY



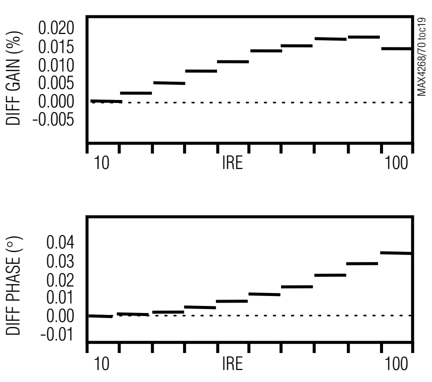
OUTPUT IMPEDANCE vs. FREQUENCY



MAX4268/MAX4269/MAX4290 CROSSTALK vs. FREQUENCY

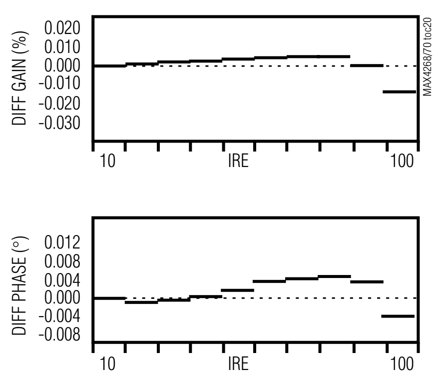


MAX4268 DIFFERENTIAL GAIN AND PHASE



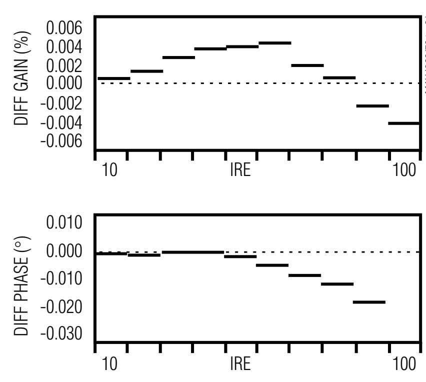
R_L = 150Ω

MAX4269 DIFFERENTIAL GAIN AND PHASE



R_L = 150Ω

MAX4270 DIFFERENTIAL GAIN AND PHASE

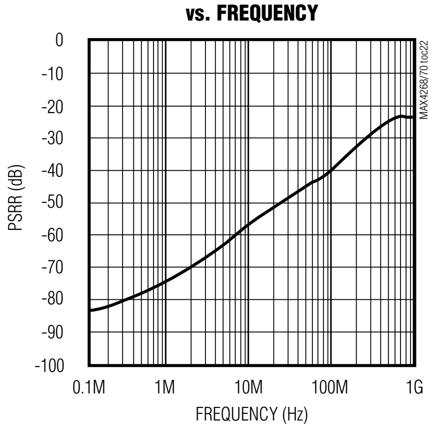


R_L = 150Ω

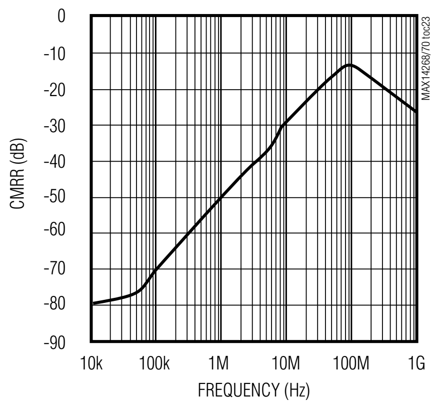
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, EN_ = 5V, R_L = 100Ω to V_{CC}/2, MAX4268 A_V = +1V/V, MAX4269 A_V = +2V/V, MAX4270 A_V = +5V/V, T_A =+25°C, unless otherwise noted.)

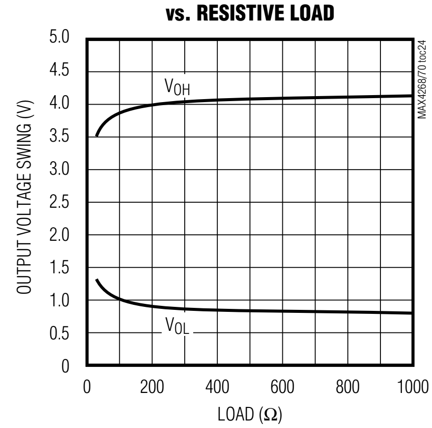
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



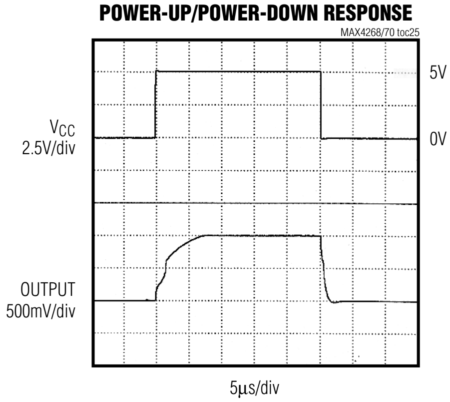
COMMON-MODE REJECTION RATIO vs. FREQUENCY



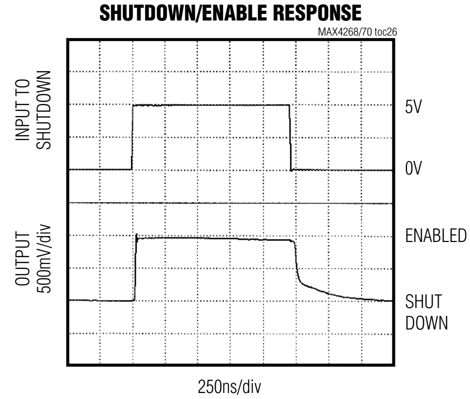
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



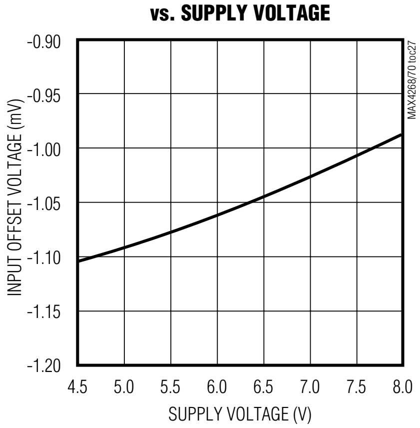
POWER-UP/POWER-DOWN RESPONSE



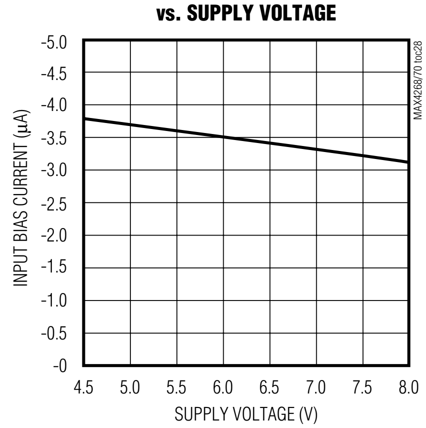
SHUTDOWN/ENABLE RESPONSE



INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



INPUT BIAS CURRENT vs. SUPPLY VOLTAGE

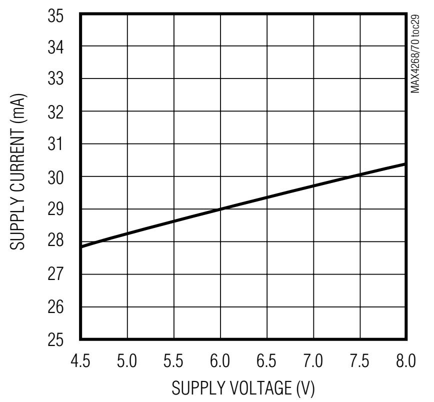


Ultra-Low-Distortion, Single-Supply, 300MHz Op Amps with Enable

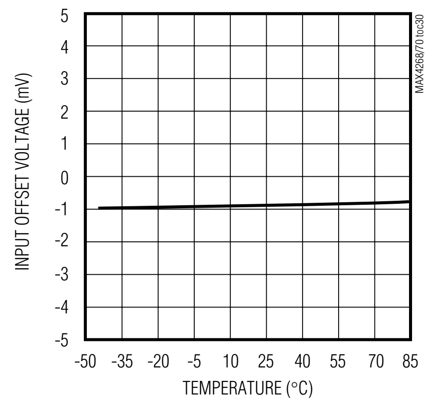
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, EN_ = 5V, R_L = 100Ω to V_{CC}/2, MAX4268 A_V = +1V/V, MAX4269 A_V = +2V/V, MAX4270 A_V = +5V/V, T_A =+25°C, unless otherwise noted.)

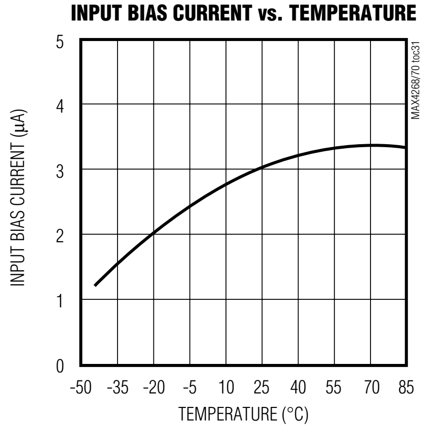
SUPPLY CURRENT (PER AMPLIFIER) vs. SUPPLY VOLTAGE



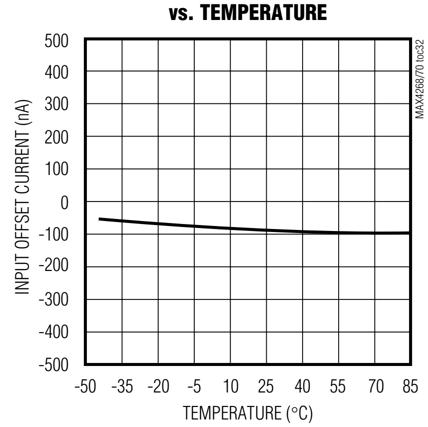
INPUT OFFSET VOLTAGE vs. TEMPERATURE



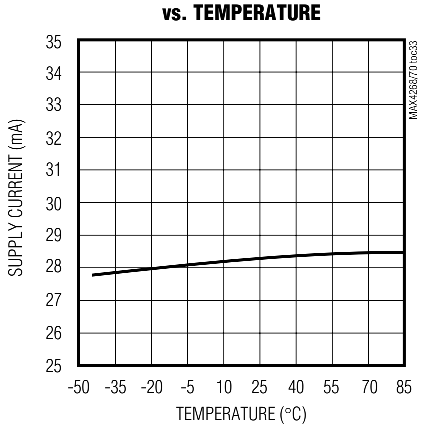
INPUT BIAS CURRENT vs. TEMPERATURE



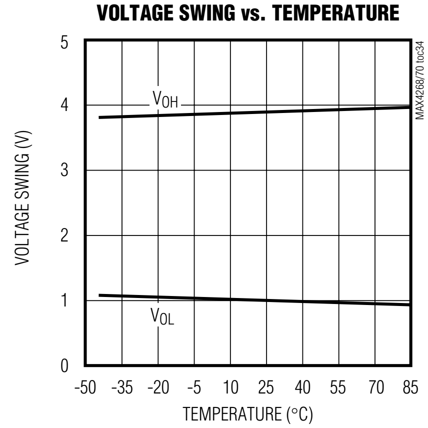
INPUT OFFSET CURRENT vs. TEMPERATURE



SUPPLY CURRENT (PER AMPLIFIER) vs. TEMPERATURE



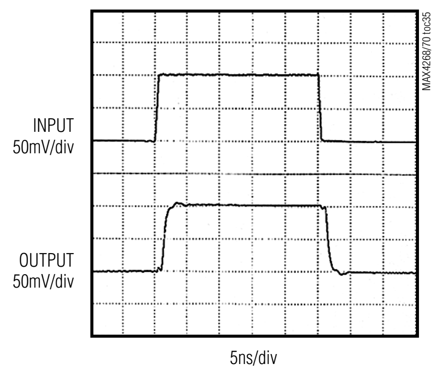
VOLTAGE SWING vs. TEMPERATURE



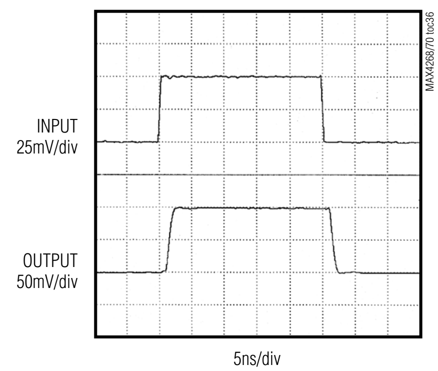
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0, EN_ = 5V, R_L = 100Ω to V_{CC}/2, MAX4268 A_V = +1V/V, MAX4269 A_V = +2V/V, MAX4270 A_V = +5V/V, T_A =+25°C, unless otherwise noted.)

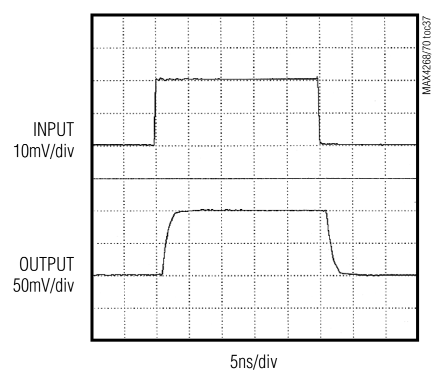
MAX4268
SMALL-SIGNAL PULSE RESPONSE



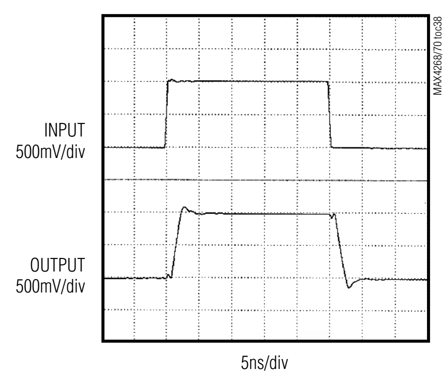
MAX4269
SMALL-SIGNAL PULSE RESPONSE



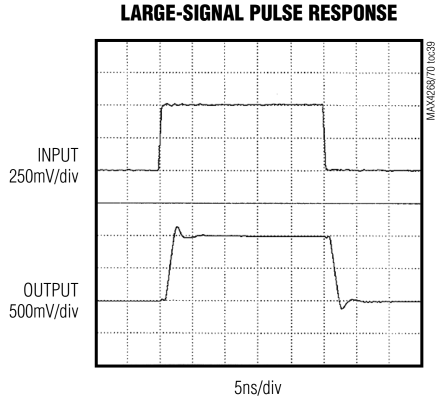
MAX4270
SMALL-SIGNAL PULSE RESPONSE



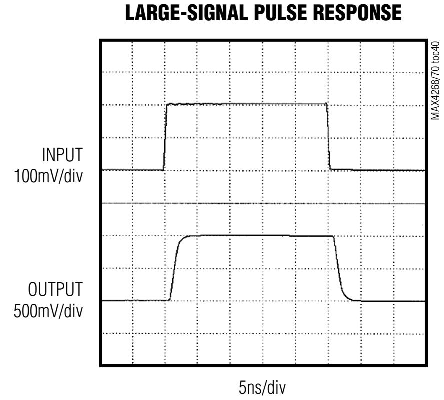
MAX4268
LARGE-SIGNAL PULSE RESPONSE



MAX4269
LARGE-SIGNAL PULSE RESPONSE



MAX4270
LARGE-SIGNAL PULSE RESPONSE



Ultra-Low-Distortion, Single-Supply, 300MHz Op Amps with Enable

Pin Description

PIN			NAME	FUNCTION
MAX4265 MAX4266 MAX4267	MAX4268 MAX4269 MAX4270			
8 µMAX/SO	14 SO	16 QSOP		
1	—	—	EN	Enable Input. Active high. Connect to V_{CC} for normal operation.
—	4, 5	4, 5	ENA, ENB	Enable Input. Active high. Connect to V_{CC} for normal operation.
2	—	—	IN-	Inverting Input
—	2, 9	2, 11	INA-, INB-	Inverting Input
3	—	—	IN+	Noninverting Input
—	3, 10	3, 12	INA+, INB+	Noninverting Input
4, 5	6, 7	6, 7	V_{EE}	Negative Power Supply
6	—	—	OUT	Amplifier Output
—	1, 8	1, 10	OUTA, OUTB	Amplifier Output
7, 8	13, 14	15, 16	V_{CC}	Positive Power Supply. Connect to a +4.5V to +8.0V supply and bypass with a 0.1µF capacitor for single-supply operation.
—	11, 12	8, 9, 13, 14	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX4265–MAX4270 single-supply operational amplifiers feature ultra-low distortion and wide bandwidth. Their low distortion and low noise make them ideal for driving high-speed analog-to-digital converters (ADCs) up to 16 bits in telecommunications applications and high-performance signal processing.

These devices can drive loads as low as 100Ω and deliver 45mA while maintaining DC accuracy and AC performance. The input common-mode voltage ranges from (V_{EE} + 1.6V) to (V_{CC} - 1.6V), while the output swings to within 1.1V of the rails.

Low Distortion

The MAX4265–MAX4270 use proprietary bipolar technology to achieve minimum distortion in single-supply systems—a feature typically available only in dual-supply op amps.

Several factors can affect the noise and distortion that a device contributes to the input signal. The following guidelines explain how various design choices impact the total harmonic distortion (THD).

- Choose the proper feedback-resistor and gain-resistor values for the application. In general, the smaller the closed-loop gain, the smaller the THD generated—especially when driving heavy resistive loads. Large-value feedback resistors can significantly improve distortion. The MAX4265–MAX4270's THD normally increases at approximately 20dB per decade at frequencies above 1MHz; this is a lower rate than that of comparable dual-supply op amps.
- Operating the device near or above the full-power bandwidth significantly degrades distortion (see the Total Harmonic Distortion vs. Frequency graph in the *Typical Operating Characteristics*).
- The decompensated devices (MAX4266/MAX4267/MAX4269/MAX4270) deliver the best distortion performance since they have a slightly higher slew rate and provide a higher amount of loop gain for a given closed-loop gain setting.

Choosing Resistor Values

Unity-Gain Configurations

The MAX4265 and MAX4268 are internally compensated for unity gain. When configured for unity gain, they require a small resistor (R_F) in series with the feedback path (Figure 1). This resistor improves AC response by reducing the Q of the tank circuit, which is formed by parasitic feedback inductance and capacitance.

Inverting and Noninverting Configurations

The values of the gain-setting feedback and input resistors are important design considerations. Large resistor values will increase voltage noise and interact with the amplifier's input and PC board capacitance to generate undesirable poles and zeros, which can decrease bandwidth or cause oscillations. For example, a noninverting gain of +2V/V (Figure 1) using $R_F = R_G = 1k\Omega$ combined with 2pF of input capacitance and 0.5pF of board capacitance will cause a feedback pole at 128MHz. If this pole is within the anticipated amplifier bandwidth, it will jeopardize stability. Reducing the 1kΩ resistors to 100Ω extends the pole frequency to 1.28GHz, but could limit output swing by adding 200Ω in parallel with the amplifier's load. Clearly, the selection of resistor values must be tailored to the specific application.

Distortion Considerations

The MAX4265–MAX4270 are ultra-low-distortion, high-bandwidth op amps. Output distortion will degrade as the total load resistance seen by the amplifier decreases. To minimize distortion, keep the input and gain-setting resistor values relatively large. A 500Ω feedback resistor combined with an appropriate input resistor to set the gain will provide excellent AC performance without significantly increasing distortion.

Noise Considerations

The amplifier's input-referred noise-voltage density is dominated by flicker noise at lower frequencies and by thermal noise at higher frequencies. Because the thermal noise contribution is affected by the parallel combination of the feedback resistive network, those resistor values should be reduced in cases where the system bandwidth is large and thermal noise is dominant. This noise-contribution factor decreases, however, with increasing gain settings. For example, the input noise voltage density at the op amp input with a gain of +10V/V using $R_F = 100k\Omega$ and $R_G = 11k\Omega$ is $e_n = 18nV/\sqrt{Hz}$. The input noise can be reduced to $8nV/\sqrt{Hz}$ by choosing $R_F = 1k\Omega$, $R_G = 110\Omega$.

Driving Capacitive Loads

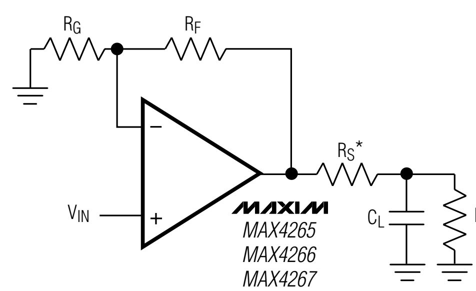
The MAX4265–MAX4270 are not designed to drive highly reactive loads; stability is maintained with loads up to 15pF with less than 2dB peaking in the frequency response. To drive higher capacitive loads, place a small isolation resistor in series between the amplifier's output and the capacitive load (Figure 1). This resistor improves the amplifier's phase margin by isolating the capacitor from the op amp's output.

To ensure a load capacitance that limits peaking to less than 2dB, select a resistance value from Figure 2. For example, if the capacitive load is 100pF, the corresponding isolation resistor is 6Ω (MAX4269). Figures 3 and 4 show the peaking that occurs in the frequency response with and without an isolation resistor.

Coaxial cable and other transmission lines are easily driven when terminated at both ends with their characteristic impedance. When driving back-terminated transmission lines, the capacitive load of the transmission line is essentially eliminated.

ADC Input Buffer

Input buffer amplifiers can be a source of significant errors in high-speed ADC applications. The input buffer is usually required to rapidly charge and discharge the ADC's input, which is often capacitive (see *Driving Capacitive Loads*). In addition, since a high-speed ADC's input impedance often changes very rapidly during the conversion cycle, measurement accuracy must



PART	R_F (Ω)	R_G (Ω)	GAIN (V/V)
MAX4265	24	∞	1
MAX4266	500	500	2
MAX4267	500	125	5

*OPTIONAL, USED TO MINIMIZE PEAKING FOR C_L > 15pF.

Figure 1. Noninverting Configuration

be maintained using an amplifier with very low output impedance at high frequencies. The combination of high speed, fast slew rate, low noise, and a low and stable distortion over load makes the MAX4265–MAX4270 ideally suited for use as buffer amplifiers in high-speed ADC applications.

Low-Power Disable Mode

The MAX4265–MAX4270 feature an active-high enable pin that can be used to save power and place the outputs in a high-impedance state. Drive EN_ with logic levels or connect EN_ to V_{CC} for normal operation. In the dual versions (MAX4268/MAX4269/MAX4270), each individual op amp is enabled separately, allowing the devices to be used in a multiplex configuration. The supply current in low-power mode is reduced to 1.6mA per device. Enable time is typically 100ns, and disable time is typically 750µs.

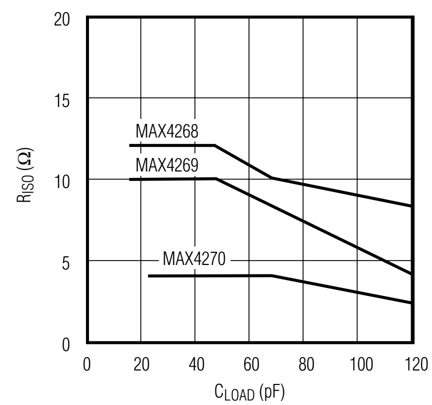


Figure 2. MAX4268/MAX4269/MAX4270 Isolation Resistance vs. Capacitive Load

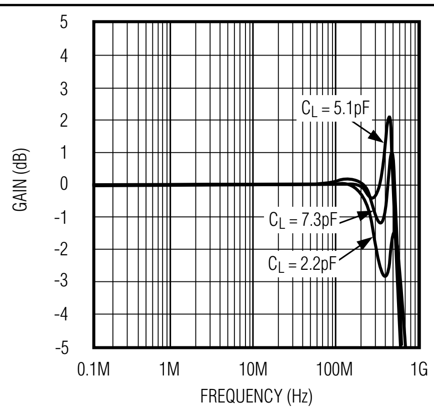


Figure 3a. MAX4268 Small-Signal Gain vs. Frequency Without Isolation Resistor

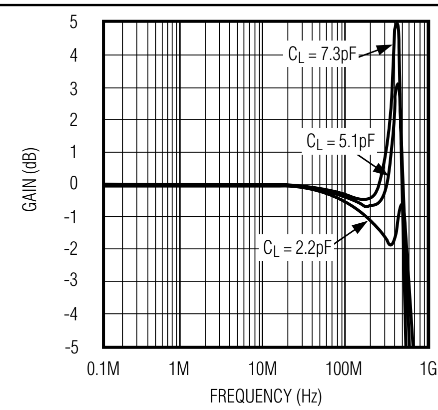


Figure 3b. MAX4269 Small-Signal Gain vs. Frequency Without Isolation Resistor

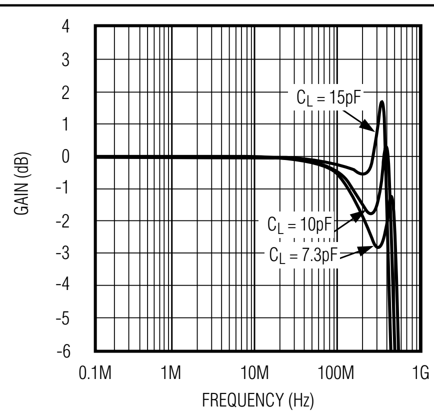


Figure 3c. MAX4270 Small-Signal Gain vs. Frequency Without Isolation Resistor

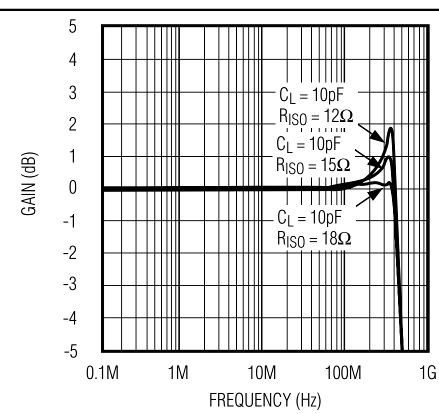


Figure 4a. MAX4268 Small-Signal Gain vs. Frequency With Isolation Resistor

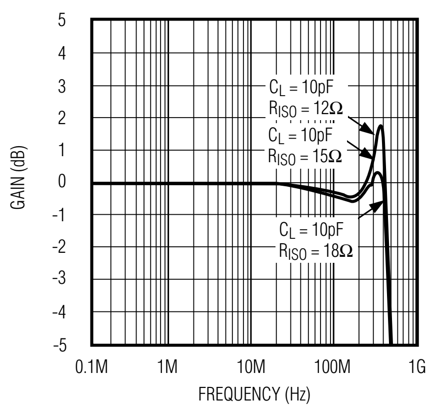


Figure 4b. MAX4269 Small-Signal Gain vs. Frequency With Isolation Resistor

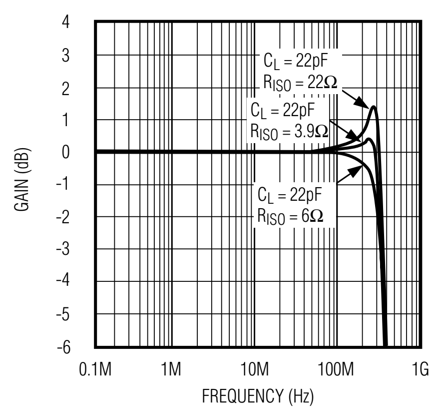


Figure 4c. MAX4270 Small-Signal Gain vs. Frequency With Isolation Resistor

Power Supplies and Layout

The MAX4265–MAX4270 operate from a single +4.5V to +8.0V power supply or from dual ±2.25V to ±4.0V supplies. For single-supply operation, bypass each power-supply input with a 0.1µF ceramic capacitor placed close to the V_{CC} pins, and an additional 10µF to V_{EE}. When operating from dual supplies, bypass each supply to ground.

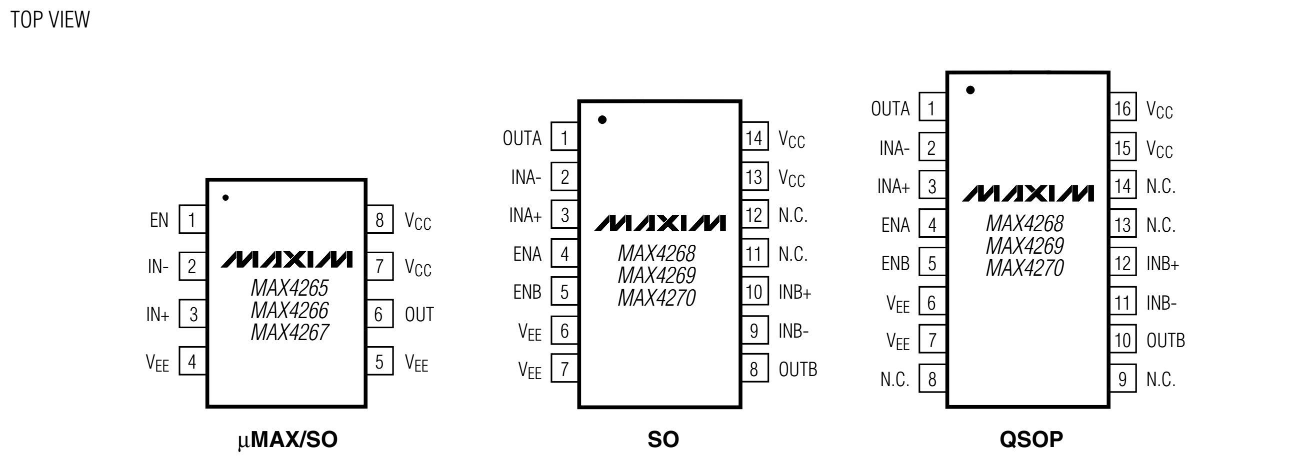
Good layout improves performance by decreasing the amount of stray capacitance and noise at the op amp's inputs and output. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components close to the op amp's pins.

Chip Information

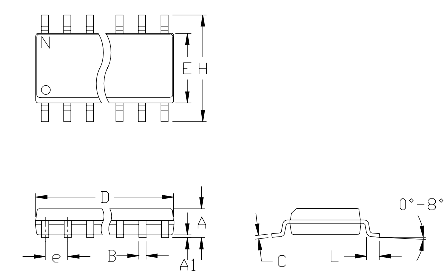
TRANSISTOR COUNT: MAX4265/66/67: 132
MAX4268/69/70: 285

Ultra-Low-Distortion, Single-Supply, 300MHz Op Amps with Enable

Pin Configurations



Package Information

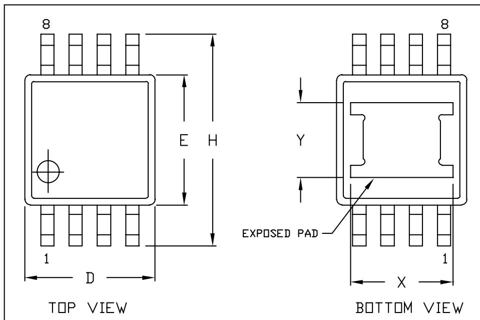


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

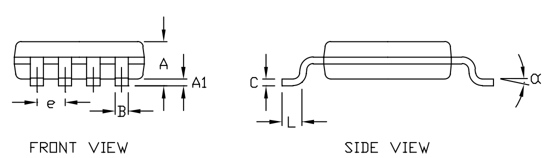
MAXIM — 120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194 — PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | DOCUMENT CONTROL NUMBER: 21-0041 | REV: A



8LUMAXD.EPS

	INCHES		MILLIMETERS		JEDEC INCHES		JEDEC MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10	---	0.043	---	1.10
A1	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15
B	0.010	0.014	0.25	0.36	0.010	0.016	0.25	0.40
C	0.005	0.007	0.13	0.18	0.005	0.009	0.13	0.23
D	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.64 BSC	
E	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
H	0.188	0.198	4.78	5.03	0.193 BSC		4.9 BSC	
L	0.016	0.026	0.41	0.66	0.016	0.027	0.40	0.70
α	0°	6°	0°	6°	0°	6°	0°	6°
*X	0.087	0.099	2.210	2.515				
*Y	0.062	0.074	1.575	1.880				

* EXPOSED PAD

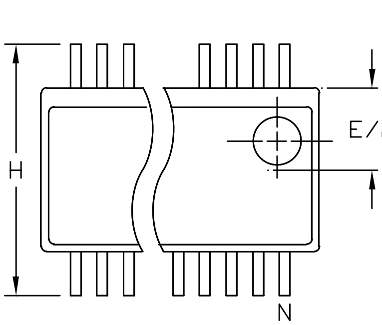


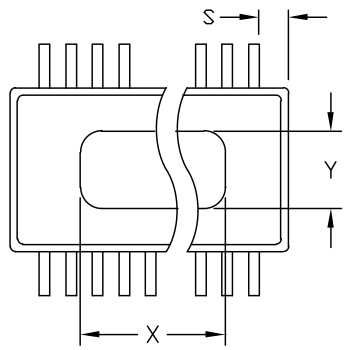
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.
5. DIMENSIONS X & Y APPLY TO EXPOSED PAD VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM — PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 8L uMAX
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV G | 1/1

Package Information (continued)

QSOP.EPS

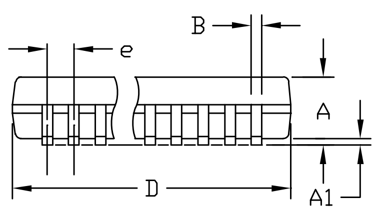


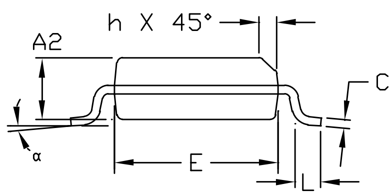


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		





NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV B | 1/1