International
IOR Rectifier

PD - 94114

PROVISIONAL

SMPS MOSFET

IRFB42N20D
IRFS42N20D
IRFSL42N20D

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	I_D
200V	**0.055Ω**	**42.6A**

Applications

- High frequency DC-DC converters

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

TO-220AB IRFB42N20D | D^2Pak IRFS42N20D | TO-262 IRFSL42N20D

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	42.6	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	30	
I_{DM}	Pulsed Drain Current ①	170	
P_D @T_A = 25°C	Power Dissipation ⑦	3.8	W
P_D @T_C = 25°C	Power Dissipation	300	
	Linear Derating Factor	2	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	TBD	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	260 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Telecom 48V input DC-DC Active Clamp Reset Forward Converter

Notes ① through ⑦ are on page 6

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	TBD	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.055	Ω	V_{GS} = 10V, I_D = 25.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	TBD	—	—	S	V_{DS} = 25V, I_D = 25.5A
Q_g	Total Gate Charge	—	103	—	nC	I_D = 25.5A
Q_{gs}	Gate-to-Source Charge	—	26	—		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	48	—		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	—	TBD	—	ns	V_{DD} = 100V
t_r	Rise Time	—	TBD	—		I_D = 25.5A
$t_{d(off)}$	Turn-Off Delay Time	—	TBD	—		R_G = TBDΩ
t_f	Fall Time	—	TBD	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	3470	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	560	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	120	—		f = 1.0MHz⑥
C_{oss}	Output Capacitance	—	TBD	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	TBD	—		V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	TBD	—		V_{GS} = 0V, V_{DS} = 0V to 160V ⑤

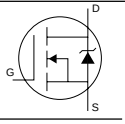
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	TBD	mJ
I_{AR}	Avalanche Current①	—	25.5	A
E_{AR}	Repetitive Avalanche Energy①	—	30	mJ

Thermal Resistance

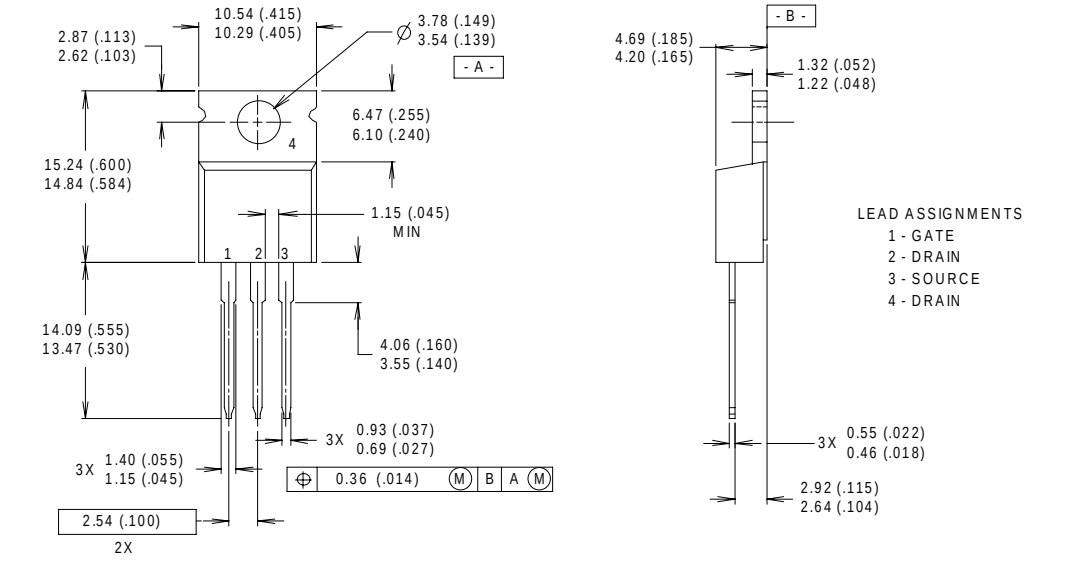
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient⑥	—	62	
$R_{\theta JA}$	Junction-to-Ambient⑦	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	42.6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	170		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 25.5A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	TBD	TBD	ns	T_J = 25°C, I_F = 25.5A
Q_{rr}	Reverse RecoveryCharge	—	2.4	3.6	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

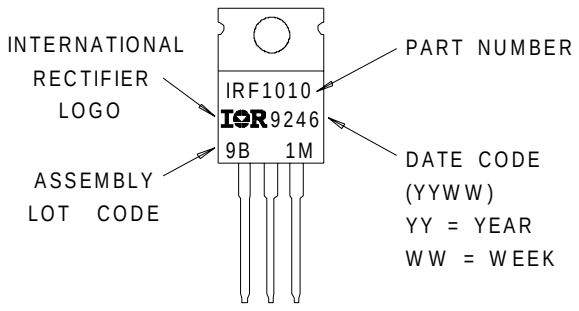


NOTES:

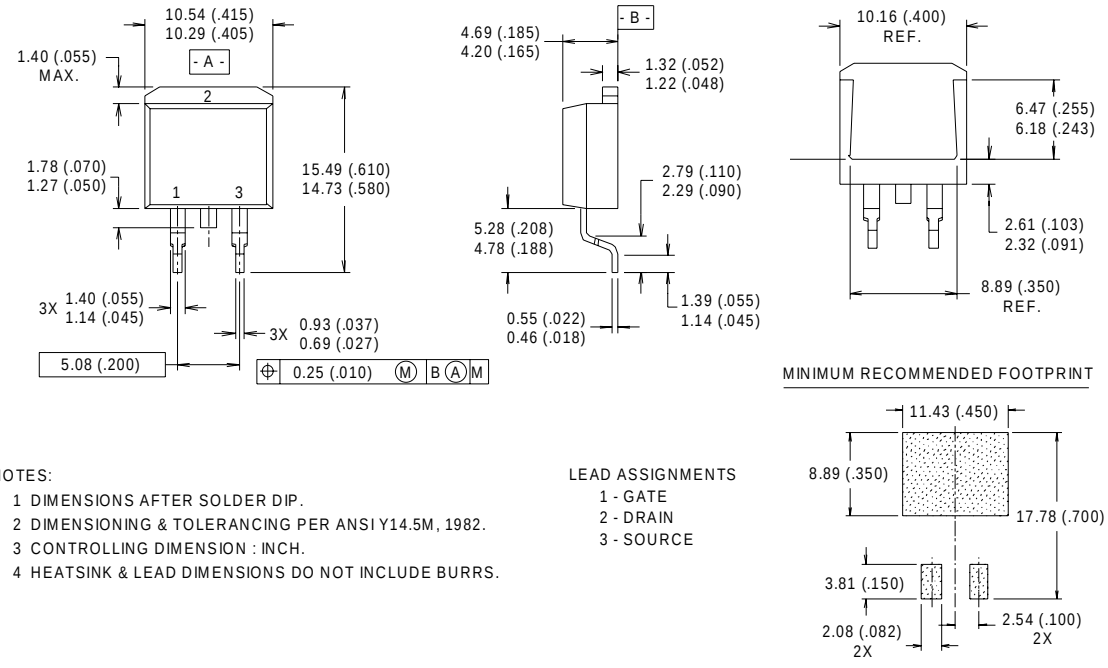
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



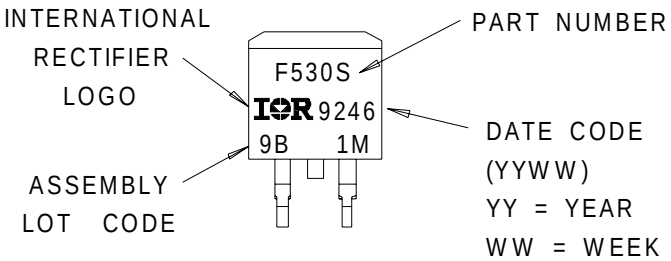
D²Pak Package Outline



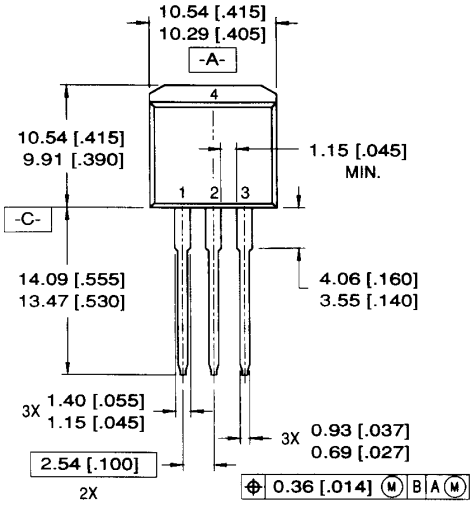
NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

D²Pak Part Marking Information

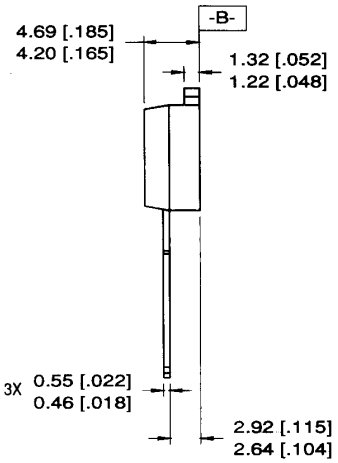


TO-262 Package Outline



LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

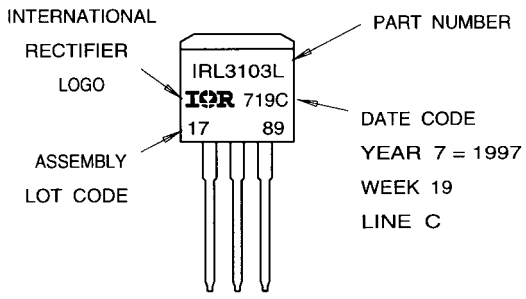


NOTES:

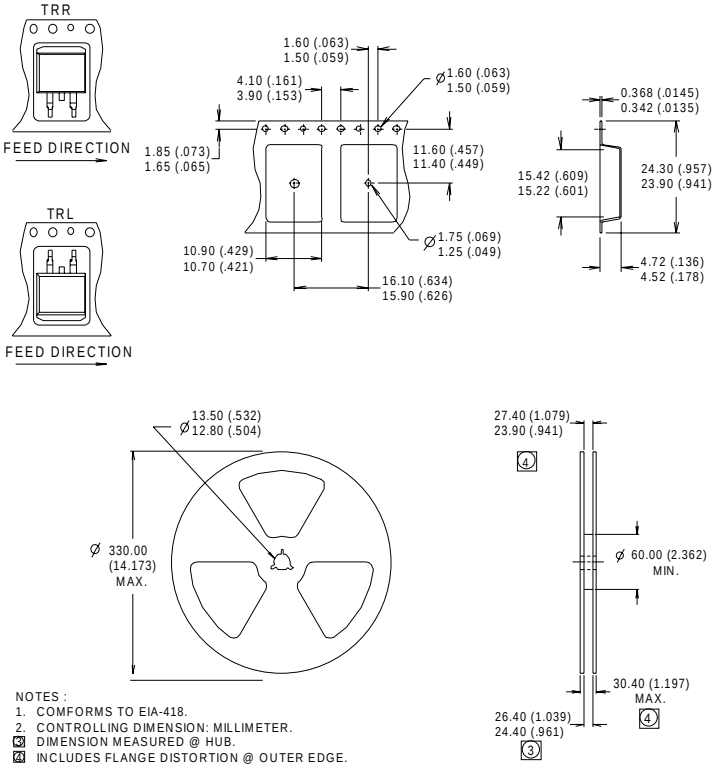
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = TBDmH R_G = TBDΩ, I_{AS} = 25.5A.

③ $I_{SD} \leq$ 25.5A, di/dt ≤ TBDA/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ This is only applied to TO-220AB package

⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

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Data and specifications subject to change without notice. 9/00