PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8543

LOW SKEW, 1-TO-4 LVDS FANOUT BUFFER

GENERAL DESCRIPTION

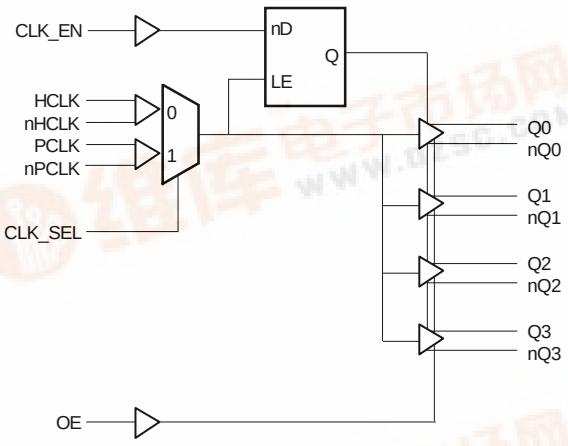
The ICS8543 is a low skew, high performance 1-to-4 clock fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. Utilizing Low Voltage Differential Signaling (LVDS) the ICS8543 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS8543 accepts any differential input level and translates it to 3.3V LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the ICS8543 ideal for those applications demanding well defined performance and repeatability.

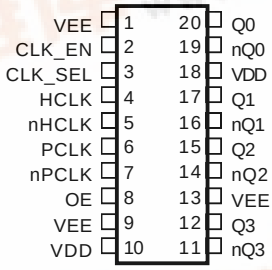
FEATURES

- 4 LVDS outputs
- Designed to meet or exceed the requirements of ANSI TIA/EIA-644
- Selectable differential HSTL or LVPECL clock inputs
- LVCMOS / LVTTL control inputs
- 3.3V operating supply
- 20 lead TSSOP
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8543

20-Lead TSSOP
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 9, 13	VEE	Power		Power supply ground. Connect to ground.
2	CLK_EN	Input	Pullup	Synchronous clock enable. When HIGH clock outputs follows clock input. When LOW, Q outputs are force low, nQ outputs are force high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH selects differential PECL inputs. When LOW selects differential HSTL inputs. LVCMOS / LVTTL interface levels.
4	HCLK	Input	Pulldown	Non-inverting differential HSTL clock input.
5	nHCLK	Input	Pullup	Inverting differential HSTL clock input.
6	PCLK	Input	Pulldown	Non-inverting differential PECL clock input.
7	nPCLK	Input	Pullup	Inverting differential PECL clock input.
8	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0, nQ0 thru Q3, nQ3
10, 18	VDD	Power		Power supply pin. Connect to 3.3V.
11, 12	nQ3, Q3	Output		Differential clock outputs. LVDS interface levels.
14, 15	nQ2, Q2	Output		Differential clock outputs. LVDS interface levels.
16, 17	nQ1, Q1	Output		Differential clock outputs. LVDS interface levels.
19, 20	nQ0, Q0	Output		Differential clock outputs. LVDS interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	HCLK, nHCLK				4	pF
		PCLK, nPLCK				4	pF
		CLK_EN, CLK_SEL				4	pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

TABLE 3A. CONTROL INPUTS FUNCTION TABLE

Inputs			Outputs	
OE	**CLK_EN**	**CLK_SEL**	**Q1 thru Q3**	**nQ1 thru nQ3**
0	X	X	Hi Z	Hi Z
1	0	0	Low	High
1	0	1	Low	High
1	1	0	ACTIVE	ACTIVE
1	1	1	ACTIVE	ACTIVE

In the active mode the state of the output is a function of the HCLK, nHCLK and PCLK, nPCLK inputs as described in Table 3B.

TABLE 3B. CLOCK INPUTS FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
HCLK, PCLK	**nHCLK, nPCLK**	**Q0 thru Q3**	**nQ0 thru nQ3**		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Single ended use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTL levels the recommended input bias network is a resistor to VCC, a resistor of equal value to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is approximately VCC/2 ± 300mV.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDD + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD	Power Supply Voltage		3.135	3.3	3.465	V
IEE	Power Supply Current				50	mA

TABLE 4B. LVPECL DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	PCLK				150	µA
		nPCLK				5	µA
IIL	Input Low Current	PCLK		-5			µA
		nPCLK		-150			µA
VPP	Peak-to-Peak Input Voltage			0.15		1.3	V
VCMR	Common Mode Input Voltage; NOTE 1			1.5		3.3	V

NOTE 1: Common mode voltage for LVPECL is defined as the minimum VIH.

TABLE 4C. LVHSTL DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	HCLK	3.135V ≤ VDDI ≤ 3.465V			150	µA
		nHCLK	3.135V ≤ VDDI ≤ 3.465V			5	µA
IIL	Input Low Current	HCLK	3.135V ≤ VDDI ≤ 3.465V	-5			µA
		nHCLK	3.135V ≤ VDDI ≤ 3.465V	-150			µA
VPP	Peak-to-Peak Input Voltage			0.15		1.3	V
VCMR	Common Mode Input Voltage; NOTE 1			0.5		VDD - 0.85	V

NOTE 1: Common mode voltage for HSTL is defined as the crossover voltage. VCMR is compatible with DCM, LVDS and SSTL inputs.

TABLE 4D. LVCMOS / LVTTL DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK_EN, CLK_SEL, OE		2			V
VIL	Input Low Voltage	CLK_EN, CLK_SEL, OE				0.8	V
IIH	Input High Current	CLK_EN, OE				5	µA
		CLK_SEL				150	µA
IIL	Input Low Current	CLK_EN, OE		-150			µA
		CLK_SEL		-5			µA

TABLE 4E. LVDS DC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOD	Differential Output Voltage		250	350	450	mV
Δ VOD	VOD Magnitude Change			4	35	mV
VOS	Offset Voltage		1.125	1.25	1.375	V
Δ VOS	VOS Magnitude Change			5	25	mV
IOZ	High Impedance Leakage Current		-10	±1	+10	µA
IOFF	Power Off Leakage		-20	±1	+20	µA
IOSD	Differential Output Short Circuit Current			3.0		mA
IOS	Output Short Circuit Current			3.0		mA

TABLE 5. AC CHARACTERISTICS, VDD = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				650	MHz
tpLH	Propagation Delay, Low-to-High	0 ≤ f ≤ 650MHz	1.8		2.4	ns
tsk(o)	Output Skew; NOTE 2				50	ps
tsk(pp)	Part-to-Part Skew; NOTE 3				300	ps
tR	Output Rise Time	R_L = 100Ω	200	400	600	ps
tF	Output Fall Time	R_L = 100Ω	200	400	600	ps
tPW	Output Pulse Width		tCYCLE/2 - TBD		tCYCLE/2 + TBD	ns
tEN	Output Enable Time				TBD	ns
tDIS	Output Disable Time				TBD	ns

NOTE 1: All parameters measured at fMAX unless noted otherwise.
NOTE 2: Defined as skew across outputs at the same supply voltages and with equal load conditions. Measured from the 50% point of the input to the differential output crossing point.
NOTE 3: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions. Measured from 50% of like inputs to the differential output crossing point.

PACKAGE OUTLINE - G SUFFIX

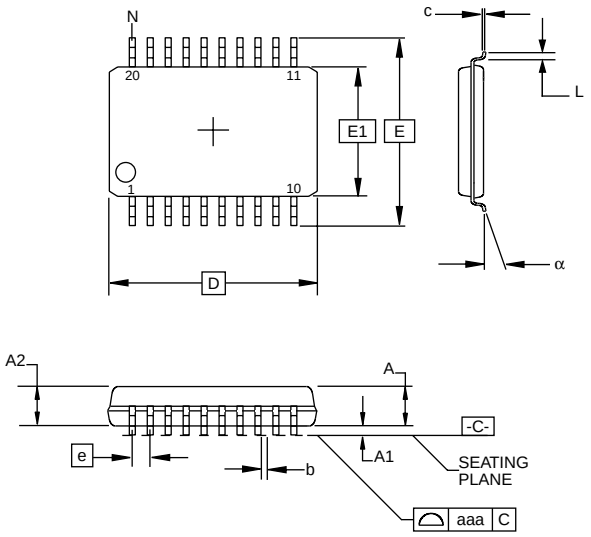


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
N	20			
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.0035	0.008
D	6.40	6.60	0.252	0.260
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8543BG	ICS8543BG	20 lead TSSOP	72 per tube	0°C to 70°C
ICS8543BGT	ICS8543BG	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C