

# MC14543B

## BCD-to-Seven Segment Latch/Decoder/Driver for Liquid Crystals

The MC14543B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to V<sub>SS</sub>).
- Chip Complexity: 207 FETs or 52 Equivalent Gates

### MAXIMUM RATINGS\* (Voltages referenced to V<sub>SS</sub>)

Rating	Symbol	Value	Unit
DC Supply Voltage	V <sub>DD</sub>	- 0.5 to + 18	V
Input Voltage, All Inputs	V <sub>in</sub>	- 0.5 to V <sub>DD</sub> + 0.5	V
DC Input Current per Pin	I <sub>in</sub>	± 10	mA
Operating Temperature Range	T <sub>A</sub>	- 55 to + 125	°C
Power Dissipation, per Package†	P <sub>D</sub>	500	mW
Storage Temperature Range	T <sub>stg</sub>	- 65 to + 150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I <sub>OHmax</sub> I <sub>OLmax</sub>	10	mA
Maximum Continuous Output Power* (Source or Sink) per Output	P <sub>OHmax</sub> P <sub>OLmax</sub>	70	mW

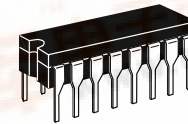
\* P<sub>OHmax</sub> = I<sub>OH</sub> (V<sub>OH</sub> - V<sub>DD</sub>) and P<sub>OLmax</sub> = I<sub>OL</sub> (V<sub>OL</sub> - V<sub>SS</sub>)

\* Maximum Ratings are those values beyond which damage to the device may occur.

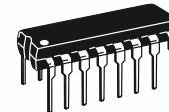
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



L SUFFIX  
CERAMIC  
CASE 620



P SUFFIX  
PLASTIC  
CASE 648



D SUFFIX  
SOIC  
CASE 751B

### ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T<sub>A</sub> = - 55° to 125°C for all packages.

### TRUTH TABLE

Inputs				Outputs							
LD	BI	Ph*	D C B A	a	b	c	d	e	f	g	Display
X	1	0	X X X X	0	0	0	0	0	0	0	Blank
1	0	0	0 0 0 0	1	1	1	1	1	1	0	0
1	0	0	0 0 0 1	0	1	1	0	0	0	0	1
1	0	0	0 0 1 0	1	1	0	1	1	0	1	2
1	0	0	0 0 1 1	1	1	1	0	0	1	1	3
1	0	0	0 1 0 0	0	1	1	0	0	1	1	4
1	0	0	0 1 0 1	1	0	1	1	0	1	1	5
1	0	0	0 1 1 0	1	0	1	1	1	1	1	6
1	0	0	0 1 1 1	1	1	1	0	0	0	0	7
1	0	0	1 0 0 0	1	1	1	1	1	1	1	8
1	0	0	1 0 0 1	1	1	1	1	0	1	1	9
1	0	0	1 0 1 0	0	0	0	0	0	0	0	Blank
1	0	0	1 0 1 1	0	0	0	0	0	0	0	Blank
1	0	0	1 1 0 0	0	0	0	0	0	0	0	Blank
1	0	0	1 1 0 1	0	0	0	0	0	0	0	Blank
1	0	0	1 1 1 0	0	0	0	0	0	0	0	Blank
1	0	0	1 1 1 1	0	0	0	0	0	0	0	Blank
0	0	0	X X X X	**							**
†	†	†	†	Inverse of Output Combinations Above							Display as above

X = Don't care

† = Above Combinations

\* = For liquid crystal readouts, apply a square wave to Ph

For common cathode LED readouts, select Ph = 0

For common anode LED readouts, select Ph = 1

\*\* = Depends upon the BCD code previously applied when LD = 1

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55 °C		25 °C			125 °C		Unit		
			Min	Max	Min	Typ #	Max	Min	Max			
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc		
		10	—	0.05	—	0	0.05	—	0.05			
		15	—	0.05	—	0	0.05	—	0.05			
	"1" Level $V_{in} = 0$ or $V_{DD}$	$V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95		—	Vdc
			10	9.95	—	9.95	10	—	9.95		—	
			15	14.95	—	14.95	15	—	14.95		—	
Input Voltage ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)	"0" Level $V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc		
		10	—	3.0	—	4.50	3.0	—	3.0			
		15	—	4.0	—	6.75	4.0	—	4.0			
	"1" Level ( $V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	$V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5		—	Vdc
			10	7.0	—	7.0	5.50	—	7.0		—	
			15	11	—	11	8.25	—	11		—	
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 0.5$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)	Source $I_{OH}$	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc		
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—			
		10	—	—	—	-10.1	—	—	—			
		10	-1.6	—	-1.3	-2.25	—	-0.9	—			
		15	-4.2	—	-3.4	-8.8	—	-2.4	—			
	Sink $I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc	
10	1.6	—	1.3	2.25	—	0.9	—					
10	—	—	—	10.1	—	—	—	—				
15	4.2	—	3.4	8.8	—	2.4	—	—				
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc		
Input Capacitance	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF		
Quiescent Current (Per Package) $V_{in} = 0$ or $V_{DD}$ , $I_{out} = 0 \mu A$	$I_{DD}$	5.0	—	5.0	—	0.005	5.0	—	150	$\mu$ Adc		
		10	—	10	—	0.010	10	—	300			
		15	—	20	—	0.015	20	—	600			
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0	$I_T = (1.6 \mu A/kHz) f + I_{DD}$ $I_T = (3.1 \mu A/kHz) f + I_{DD}$ $I_T = (4.7 \mu A/kHz) f + I_{DD}$							$\mu$ Adc		

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 V min @  $V_{DD} = 5.0$  V  
 2.0 V min @  $V_{DD} = 10$  V  
 2.5 V min @  $V_{DD} = 15$  V

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V_{DD}$  in V, and  $f$  in kHz is input frequency.

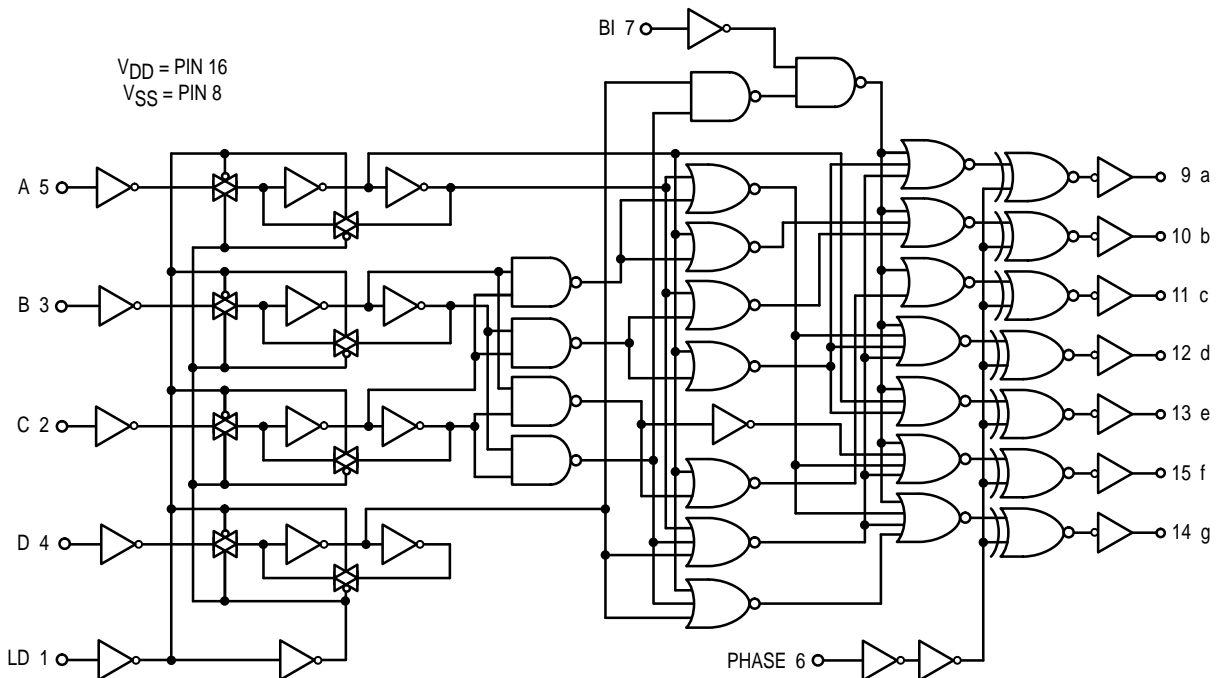
\*\*The formulas given are for the typical characteristics only at 25 °C.

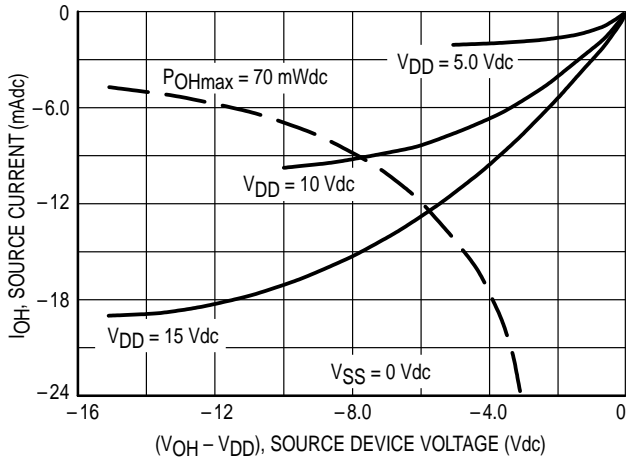
**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub>	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off Delay Time $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 520 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 217 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 160 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	605 250 185	1210 500 370	ns
Turn-On Delay Time $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 420 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 172 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 130 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	505 205 155	1650 660 495	ns
Setup Time	$t_{su}$	5.0 10 15	350 450 500		— — —	ns
Hold Time	$t_h$	5.0 10 15	40 30 20		— — —	ns
Latch Disable Pulse Width (Strobing Data)	$t_{WH}$	5.0 10 15	250 100 80	125 50 40	— — —	ns

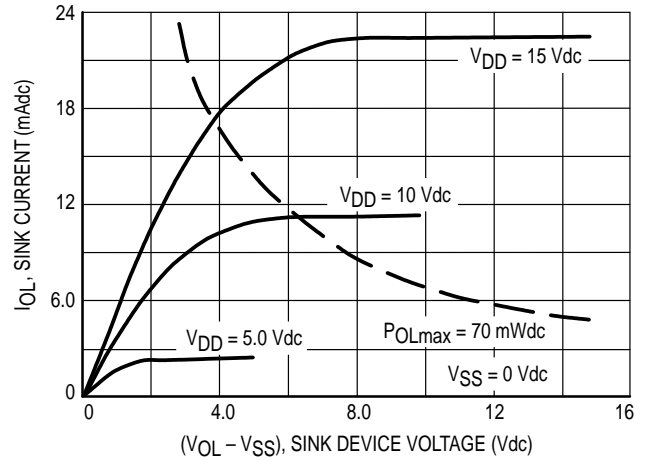
\* The formulas given are for the typical characteristics only.

**LOGIC DIAGRAM**





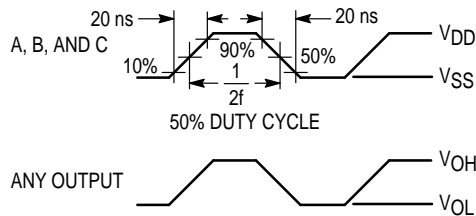
**Figure 1. Typical Output Source Characteristics**



**Figure 2. Typical Output Sink Characteristics**

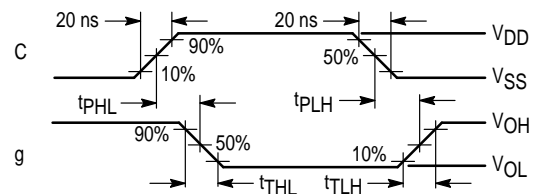
Inputs BI and Ph low, and Inputs D and LD high.  
f in respect to a system clock.

All outputs connected to respective  $C_L$  loads.

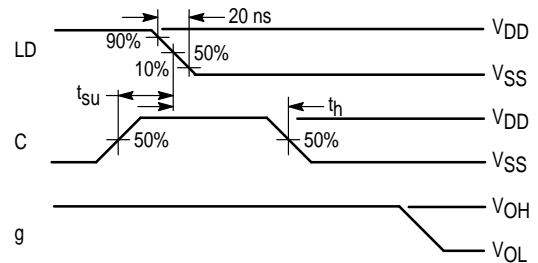


**Figure 3. Dynamic Power Dissipation Signal Waveforms**

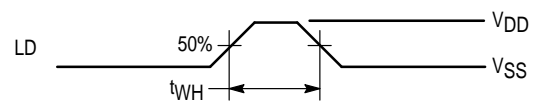
(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.



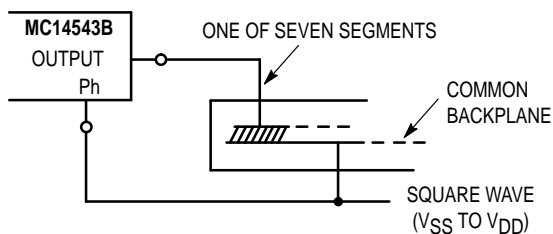
(c) Data DCBA strobed into latches



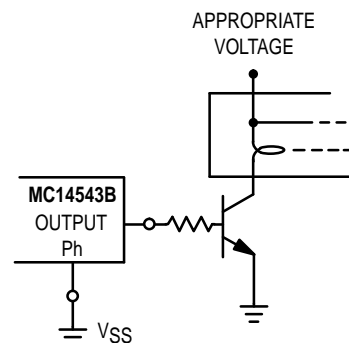
**Figure 4. Dynamic Signal Waveforms**

## CONNECTIONS TO VARIOUS DISPLAY READOUTS

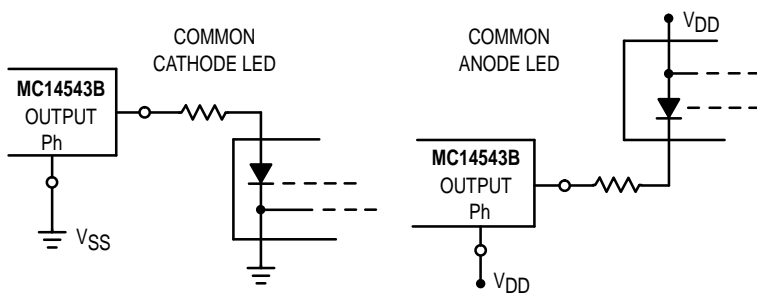
### LIQUID CRYSTAL (LC) READOUT



### INCANDESCENT READOUT

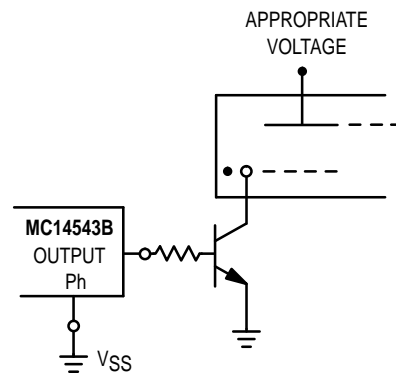


### LIGHT EMITTING DIODE (LED) READOUT

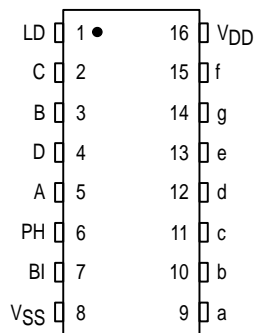


NOTE: Bipolar transistors may be added for gain (for  $V_{DD} \leq 10\text{ V}$  or  $I_{out} \geq 10\text{ mA}$ ).

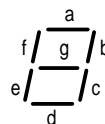
### GAS DISCHARGE READOUT



### PIN ASSIGNMENT

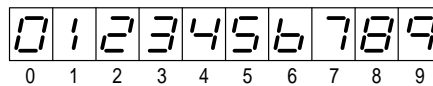


### CONNECTIONS TO SEGMENTS



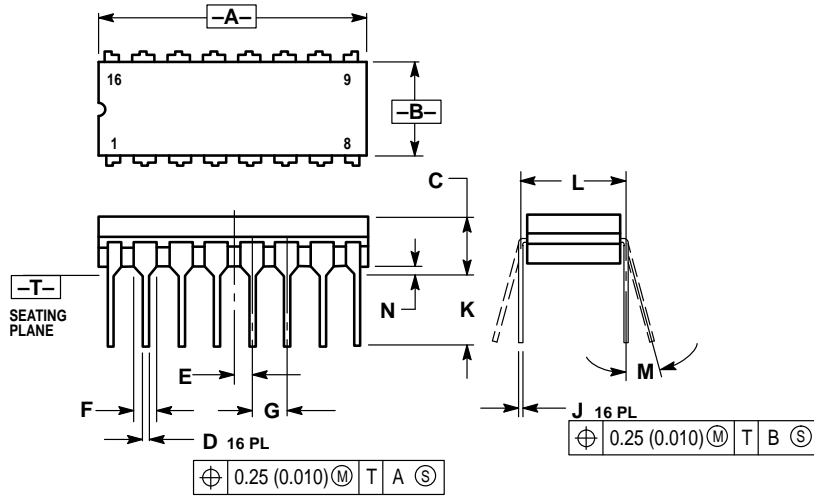
$V_{DD}$  = PIN 16  
 $V_{SS}$  = PIN 8

### DISPLAY



## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

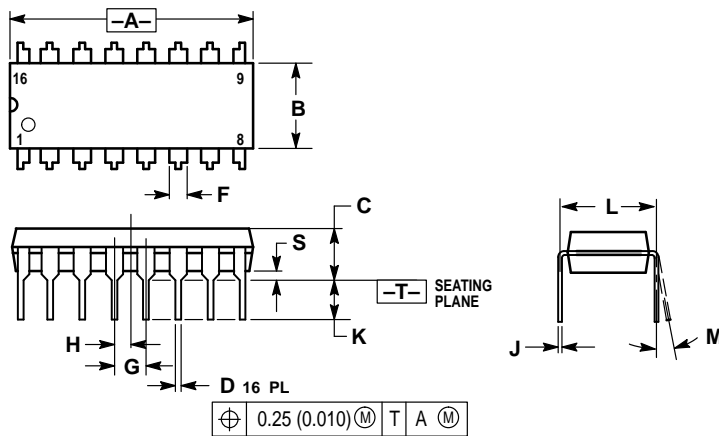


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



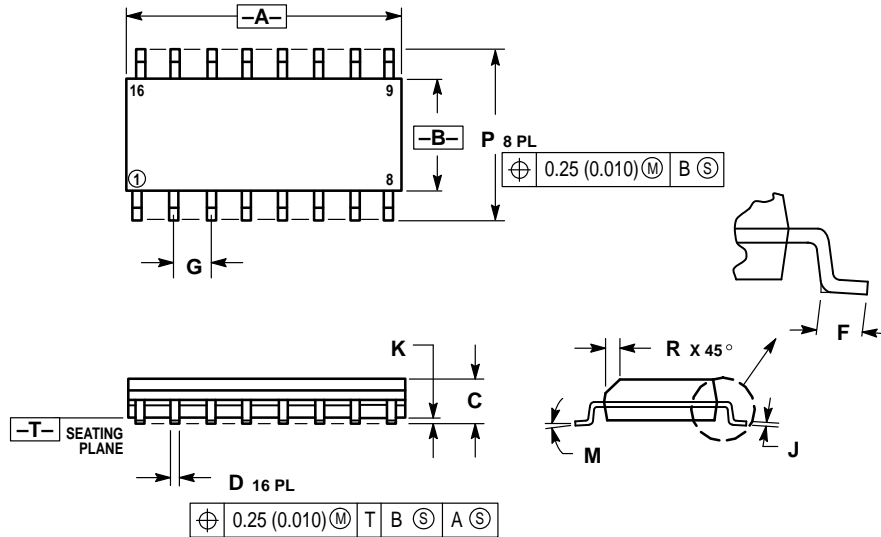
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS


### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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