



MICROCLOCK

PRELIMINARY INFORMATION

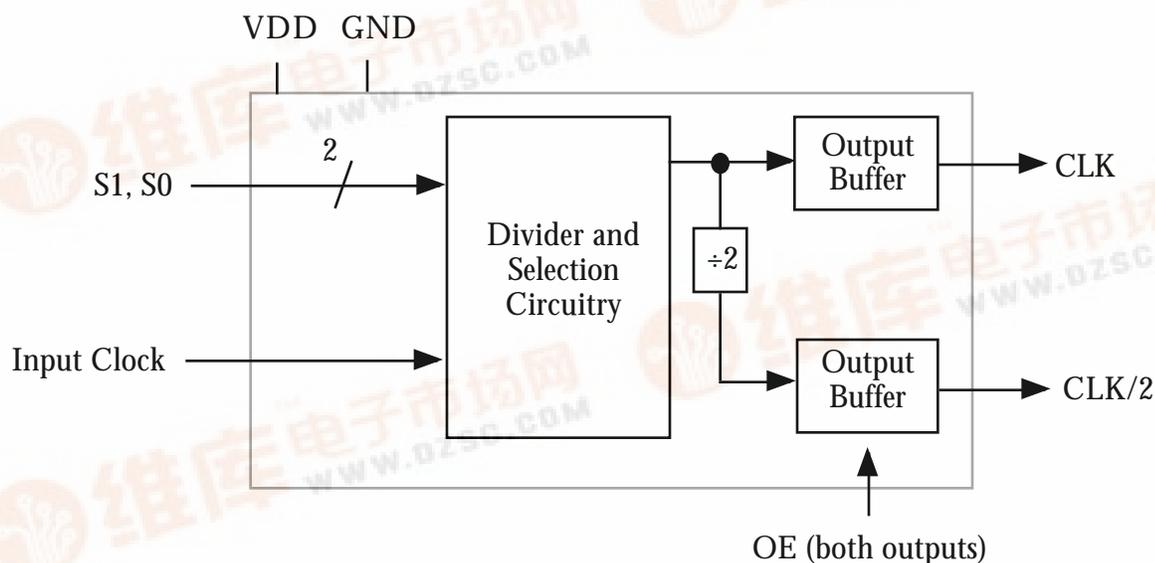
ICS543 Clock Divider and 2X Multiplier

Description

The ICS543 is a cost effective way to produce a high quality clock output divided from a clock input. The chip accepts a clock input up to 90 MHz at 5.0 V, and by using proprietary Phase Locked Loop (PLL) techniques, produces a divide by 3, 5, 6, or 10, or a multiply by 2 of the input clock. There are two outputs on the chip, one being a low-skew divide by two of the other. So, for instance, if an 81 MHz input clock is used, the ICS543 can produce low skew 27 MHz and 13.5 MHz clocks. The chip has an all-chip power down mode that stops the outputs low, and an OE pin that tri-states the outputs.

The ICS543 is a member of the ICS ClockBlocks™ family of clock building blocks. See the ICS541 and ICS542 for other clock dividers, and the ICS300, 501, 502, and 503 for clock multipliers.

Block Diagram



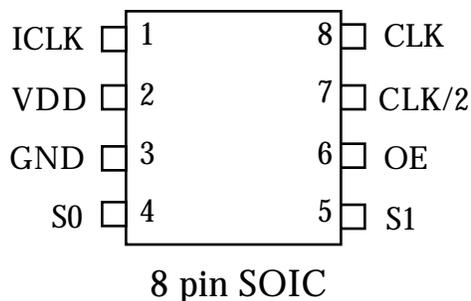
Features

- Packaged in 8 pin SOIC 
- Low cost clock divider and 2X multiplier
- Low skew (500ps) outputs. One is ÷ 2 of other.
- Easy to use with other generators and buffers
- Input clock frequency up to 90 MHz at 5 V
- Output clock duty cycle of 45/55
- Power Down turns off chip
- Output Enable
- Full CMOS clock swings with 25 mA drive capability at TTL levels
- Advanced, low power CMOS process
- Operating voltages of 3.0 to 5.5 V





Pin Assignment



Clock Decoding Table

S1 #5	S0 #4	CLK pin #8	CLK/2 pin #7	Max. Input at 5V	Max. Input at 3.3V
0	0	Power Down All		-	-
0	1	Input x 2	Input	67 MHz	50 MHz
1	0	Input/5	Input/10	60 MHz	40 MHz
1	1	Input/3	Input/6	90 MHz	60 MHz

0 = connect directly to ground.
1 = connect directly to VDD.

Pin Descriptions

Number	Name	Type	Description
1	ICLK	CI	Clock input.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	S0	I	Select 0 for output clock. Connect to GND or VDD, per decoding table above.
5	S1	I	Select 1 for output clock. Connect to GND or VDD, per decoding table above.
6	OE	I	Output Enable. Tri-states both output clocks when low.
7	CLK/2	O	Clock output per Table above. Low skew divide by two of pin 8 clock.
8	CLK	O	Clock output per Table above.

Key: CI = clock input, I = input, O = output, P = power supply connection

External Components

The ICS543 requires a 0.01 μ F decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS543 to minimize lead inductance. No external power supply filtering is required for this device. A 33 Ω terminating resistor can be used next to each output pin. If a 3.3 V input clock is applied to the ICLK pin, with the ICS543 at 5 V, the clock must be AC coupled.



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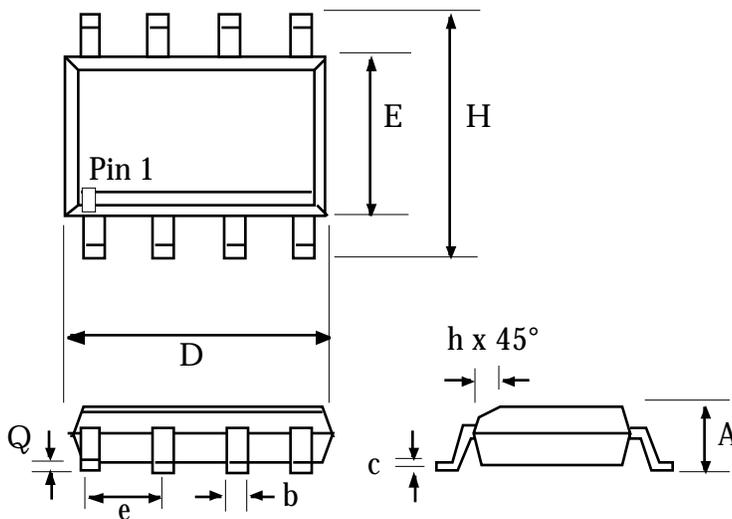
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ICS543
Clock Divider and 2X Multiplier**Electrical Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	C
Soldering Temperature	Max of 10 seconds			260	C
Storage temperature		-65		150	C
DC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, ICLK only	ICLK (Pin 1)	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, ICLK only	ICLK (Pin 1)		VDD/2	(VDD/2)-1	V
Input High Voltage, VIH	S0, S1, OE	2			V
Input Low Voltage, VIL	S0, S1, OE			0.8	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
IDD Operating Supply Current, 50 MHz input	No Load, 5.0V, +5, +10		17		mA
IDD Operating Supply Current, 50 MHz input	No Load, 3.3V, +5, 10		9		mA
Short Circuit Current	Each Output		±70		mA
Input Capacitance, S1, S0, OE	Pins 4, 5, 6		4		pF
AC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Input Frequency, clock input	at VDD = 5V	4		See page 2	MHz
Input Frequency, clock input	at VDD = 3.3V	4		See page 2	MHz
Skew of output clocks	rising edges at VDD/2			500	ps
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle	at VDD/2	45	49 to 51	55	%



Package Outline and Package Dimensions



8 pin SOIC

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.055	0.068	1.397	1.7272
b	0.013	0.019	0.330	0.483
D	0.185	0.200	4.699	5.080
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.015		0.381
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS543M	ICS543M	8 pin SOIC	0 to 70 C
ICS543MT	ICS543M	8 pin SOIC on tape and reel	0 to 70 C

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