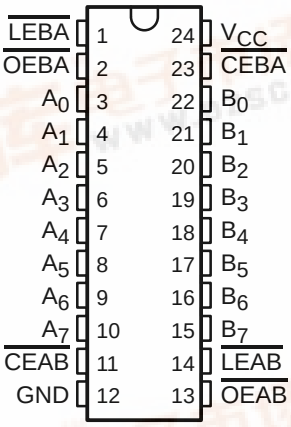
- **Function and Pinout Compatible With FCT and F Logic**
- **25-Ω Output Series Resistors to Reduce Transmission-Line Reflection Noise**
- **Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **12-mA Output Sink Current 15-mA Output Source Current**
- **Separation Controls for Data Flow in Each Direction**
- **Back-to-Back Latches for Storage**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **3-State Outputs**

Q OR SO PACKAGE
(TOP VIEW)



description

The CY74FCT2543T octal latched transceiver contains two sets of eight D-type latches. Separate latch enable ($\overline{LEAB}$, $\overline{LEBA}$) and output enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs permit each latch set to have independent control of inputting and outputting in either direction of data flow. For example, for data flow from A to B, the A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to take data from B, as indicated in the function table. With $\overline{CEAB}$ low, a low signal on the A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B output buffers are active and reflect data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs. On-chip termination resistors at the outputs reduce system noise caused by reflections. The CY74FCT2543T can replace the CY74FCT543T to reduce noise in an existing design.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION
$\overline{OEAB}$	A-to-B output-enable input (active low)
$\overline{OEBA}$	B-to-A output-enable input (active low)
$\overline{CEAB}$	A-to-B enable input (active low)
$\overline{CEBA}$	B-to-A enable input (active low)
$\overline{LEAB}$	A-to-B latch-enable input (active low)
$\overline{LEBA}$	B-to-A latch-enable input (active low)
A	A-to-B data inputs or B-to-A 3-state outputs
B	B-to-A data inputs or A-to-B 3-state outputs

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.3	CY74FCT2543CTQCT	FCT2543C
	SOIC – SO	Tube	5.3	CY74FCT2543CTSOC	FCT2543C
		Tape and reel	5.3	CY74FCT2543CTSOCT	
	QSOP – Q	Tape and reel	6.5	CY74FCT2543ATQCT	FCT2543A
	SOIC – SO	Tube	6.5	CY74FCT2543ATSOC	FCT2543A
		Tape and reel	6.5	CY74FCT2543ATSOCT	
	QSOP – Q	Tape and reel	8.5	CY74FCT2543TQCT	FCT2543

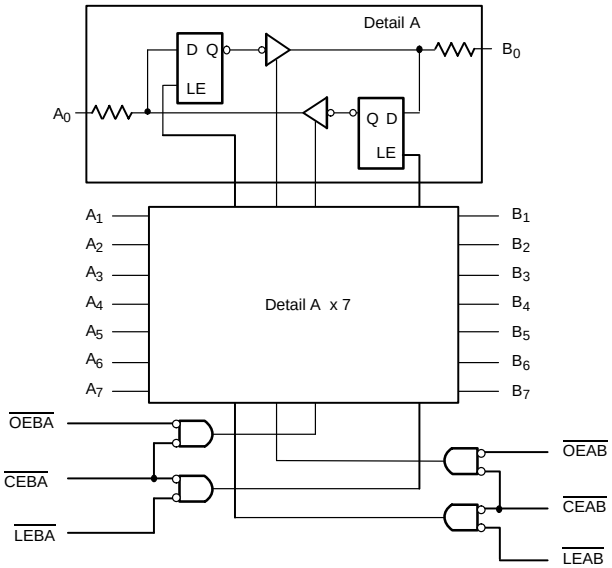
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			LATCH A-TO-B‡	OUTPUT B
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Storing	Z
X	H	X	Storing	X
X	X	H	X	Z
L	L	L	Transparent	Current A inputs
L	H	L	Storing	Previous A inputs

‡ Before $\overline{LEAB}$ low-to-high transition
H = High logic level, L = Low logic level, X = Don't care,
Z = High-impedance state
A-to-B data flow shown; B-to-A is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

functional block diagram



absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential . . . . . –0.5 V to 7 V
DC input voltage range . . . . . –0.5 V to 7 V
DC output voltage range . . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package . . . . . 61°C/W
SO package . . . . . 46°C/W
Ambient temperature range with power applied, T_A . . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_{IN} = –18 mA			–0.7	–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –15 mA		2.4	3.3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 12 mA			0.3	0.55	V
R_{out}	V_{CC} = 4.75 V,	I_{OL} = 12 mA		20	25	40	Ω
V_{hys}	All inputs				0.2		V
I_{IH}	V_{CC} = 5.25 V	$V_{IN} = V_{CC}$				5	µA
		V_{IN} = 2.7 V				±1	
I_{IL}	V_{CC} = 5.25 V,	V_{IN} = 0.5 V				±1	µA
I_{OZH}	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V				15	µA
I_{OZL}	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V				–15	µA
I_{OS}‡	V_{CC} = 5.25 V,	V_{OUT} = 0 V		–60	–120	–225	mA
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V				±1	µA
I_{CC}	V_{CC} = 5.25 V,	$V_{IN} \le 0.2$V,	$V_{IN} \ge V_{CC} - 0.2$ V		0.1	0.2	mA
ΔI_{CC}	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open				0.5	2	mA
I_{CCD}¶	V_{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, CEAB and OEAB = LOW, CEBA = HIGH, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V				0.06	1.2	mA/ MHz
I_C#	V_{CC} = 5.25 V, f_0 = 10 MHz, Outputs open, CEAB and OEAB = LOW, CEBA = HIGH, f_0 = LEAB = 10 MHz	One bit switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		0.7	1.4	mA
			V_{IN} = 3.4 V or GND		1.2	3.4	
		Eight bits switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		2.8	5.6‖	
			V_{IN} = 3.4 V or GND		5.1	14.6‖	
C_i					5	10	pF
C_o					9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current
I_{CC} = Power-supply current with CMOS input levels
ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_0 = Clock frequency for registered devices, otherwise zero
f_1 = Input signal frequency
N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

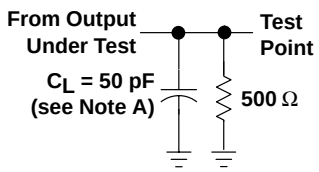
timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			CY74FCT2543T		CY74FCT2543AT		CY74FCT2543CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEBA}$ or $\overline{LEAB}$ low		5		5		5		ns
t_{su}	Setup time, high or low	A or B before $\overline{LEBA}\downarrow$ or $\overline{LEAB}\downarrow$	2		2		2		ns
t_h	Hold time, high or low	A or B after $\overline{LEBA}\downarrow$ or $\overline{LEAB}\downarrow$	2		2		2		ns

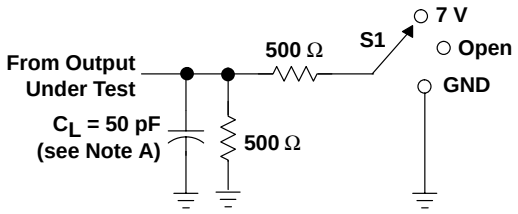
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT2543T		CY74FCT2543AT		CY74FCT2543CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.5	8.5	2.5	6.5	2.5	5.5	ns
t_{PHL}									
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	2.5	12.5	2.5	8	2.5	7	ns
t_{PHL}									
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2	12	2	9	2	8	ns
t_{PZL}			2	12	2	9	2	8	
t_{PZH}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	2	12	2	9	2	8	ns
t_{PZL}			2	12	2	9	2	8	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2	9	2	7.5	2	6.5	ns
t_{PLZ}			2	9	2	7.5	2	6.5	
t_{PHZ}	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	2	9	2	7.5	2	6.5	ns
t_{PLZ}			2	9	2	7.5	2	6.5	

PARAMETER MEASUREMENT INFORMATION

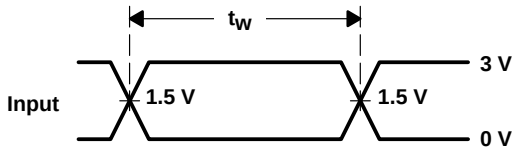


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

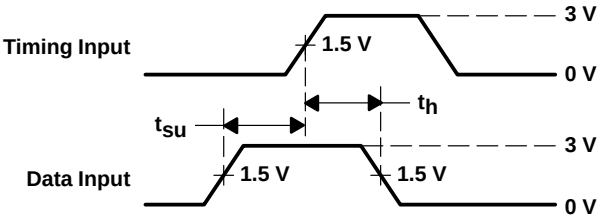


LOAD CIRCUIT FOR 3-STATE OUTPUTS

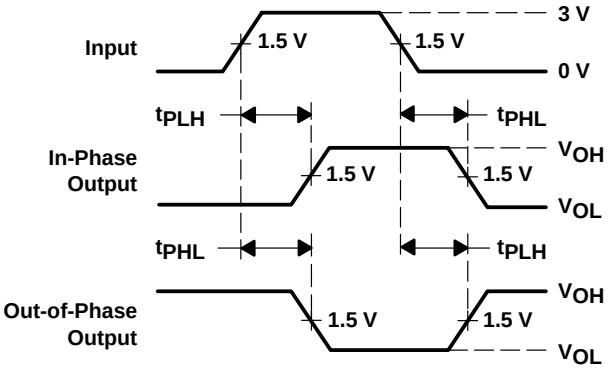
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



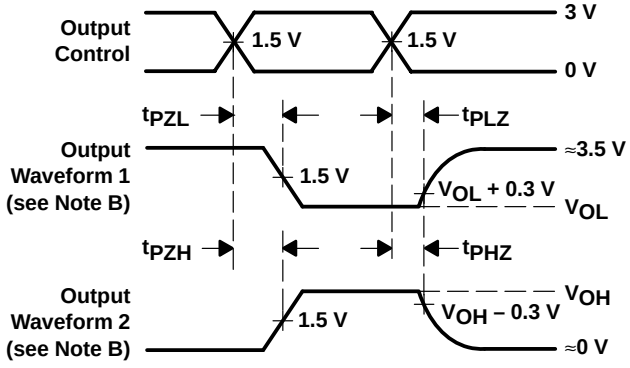
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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