

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- B-Port Outputs Have Equivalent $22\text{-}\Omega$ Series Resistors, So No External Resistors Are Required
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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SN54LVTH2245, SN74LVTH2245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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description (continued)

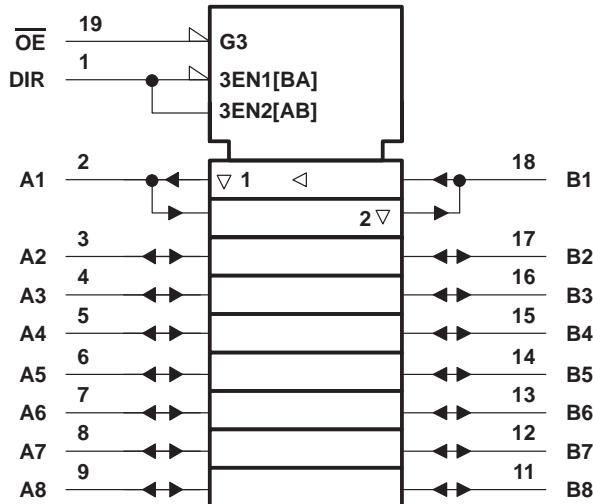
These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH2245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH2245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

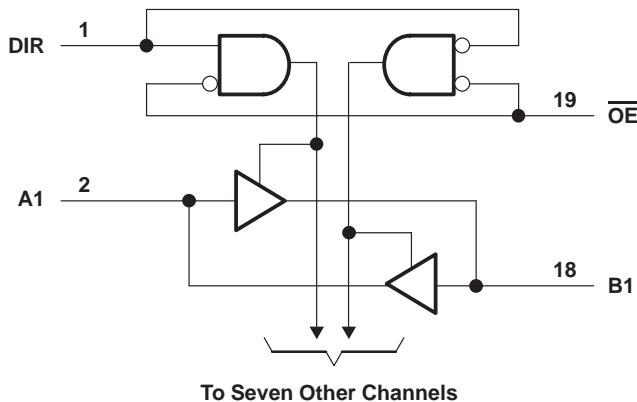
INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O :	
SN54LVTH2245 (A port)	96 mA
SN74LVTH2245 (A port)	128 mA
B port	30 mA
Current into any output in the high state, I_O (see Note 2):	
SN54LVTH2245 (A port)	48 mA
SN74LVTH2245 (A port)	64 mA
B port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JEDEC 51.

recommended operating conditions (see Note 4)

		SN54LVTH2245		SN74LVTH2245		UNIT	
		MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V	
V _{IH}	High-level input voltage	2		2		V	
V _{IL}	Low-level input voltage			0.8	0.8	V	
V _I	Input voltage			5.5	5.5	V	
I _{OH}	High-level output current	A port		-24	-32	mA	
		B port		-12	-12		
I _{OL}	Low-level output current	A port		48	64	mA	
		B port		12	12		
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V	
Δt/ΔV _{CC}	Power-up ramp rate		200	200		μs/V	
T _A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH2245			SN74LVTH2245			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	A port	$V_{CC} = 2.7 \text{ V}$ to 3.6 V , $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$		$V_{CC} - 0.2$			V
		$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4		2.4			
		$V_{CC} = 3 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2			2	
			$I_{OH} = -32 \text{ mA}$					
	B port	$V_{CC} = 2.7 \text{ V}$ to 3.6 V , $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$		$V_{CC} - 0.2$			V
V_{OL}	A port	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$	0.2	0.2			V
			$I_{OL} = 24 \text{ mA}$	0.5	0.5			
		$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$	0.4	0.4			
			$I_{OL} = 32 \text{ mA}$	0.5	0.5			
			$I_{OL} = 48 \text{ mA}$	0.55				
		B port	$I_{OL} = 64 \text{ mA}$			0.55		
			$V_{CC} = 2.7 \text{ V}$ to 3.6 V , $I_{OL} = 100 \mu\text{A}$	0.2	0.2			
			$V_{CC} = 3 \text{ V}$, $I_{OL} = 12 \text{ mA}$	0.8	0.8			
I_I	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ or GND		± 1	± 1			μA
		$V_{CC} = 0$ or 3.6 V , $V_I = 5.5 \text{ V}$		10	10			
	A or B ports‡	$V_{CC} = 3.6 \text{ V}$	$V_I = 5.5 \text{ V}$	20	20			
			$V_I = V_{CC}$	1	1			
		$V_{CC} = 3.6 \text{ V}$	$V_I = 0$	-5	-5			
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V					± 100	μA	
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	75	75			μA
			$V_I = 2 \text{ V}$	-75	-75			
		$V_{CC} = 3.6 \text{ V}$ §, $V_I = 0$ to 3.6 V				500 -750		
I_{OZPU}	$V_{CC} = 0$ to 1.5 V , $V_O = 0.5 \text{ V}$ to 3 V , $OE = \text{don't care}$			$\pm 100^*$		± 100	μA	
I_{OZPD}	$V_{CC} = 1.5 \text{ V}$ to 0 , $V_O = 0.5 \text{ V}$ to 3 V , $OE = \text{don't care}$			$\pm 100^*$		± 100	μA	
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high		0.19	0.1	0.19		mA
		Outputs low		5	3	5		
		Outputs disabled		0.19	0.1	0.19		
$\Delta I_{CC}¶$	$V_{CC} = 3 \text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND			0.2		0.2	mA	
C_i	$V_I = 3 \text{ V}$ or 0			4		4	pF	
C_{io}	$V_O = 3 \text{ V}$ or 0			9		9	pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals are at V_{CC} or GND.

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

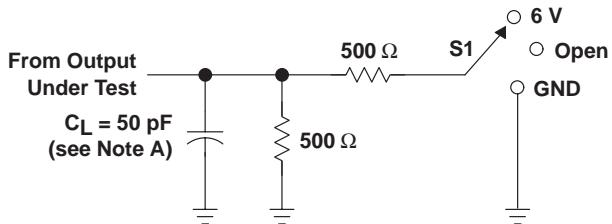
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH2245				SN74LVTH2245				UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYPT [†]	MAX	MIN	MAX
t _{PLH}	A	B	1	4.6		5.3	1.1	2.9	4.4		5.1
t _{PHL}			1	4.6		5.3	1.1	2.6	4.4		5.1
t _{PLH}	B	A	1	3.7		4.2	1.1	2.2	3.5		4
t _{PHL}			1	3.7		4.2	1.1	2	3.5		4
t _{PZH}	$\overline{\text{OE}}$	A	1.2	5.7		7.4	1.3	3.1	5.5		7.1
t _{PZL}			1.6	5.7		6.8	1.7	3.2	5.5		6.5
t _{PHZ}	$\overline{\text{OE}}$	A	2	6.2		6.8	2.2	3.6	5.9		6.5
t _{PLZ}			2	5.3		5.5	2.2	3.4	5		5.1
t _{PZH}	$\overline{\text{OE}}$	B	1.2	6.4		7.6	1.3	3.5	6.2		7.3
t _{PZL}			1.6	6.4		7.5	1.7	3.7	6.2		7.3
t _{PHZ}	$\overline{\text{OE}}$	B	2	6.1		6.8	2.2	3.9	5.9		6.5
t _{PLZ}			2	5.7		5.9	2.2	3.7	5.4		5.7

[†]All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

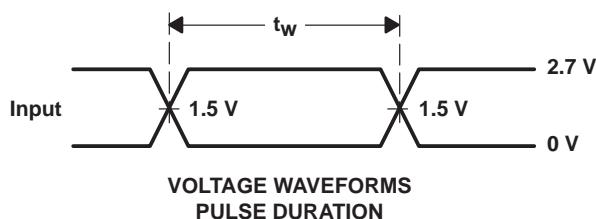
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PARAMETER MEASUREMENT INFORMATION

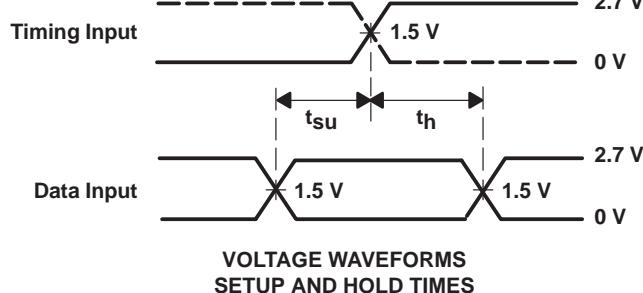


LOAD CIRCUIT

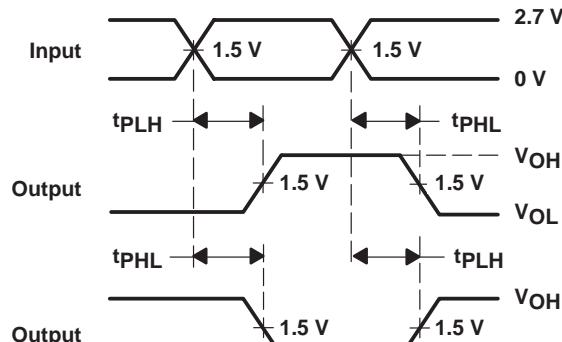


VOLTAGE WAVEFORMS
PULSE DURATION

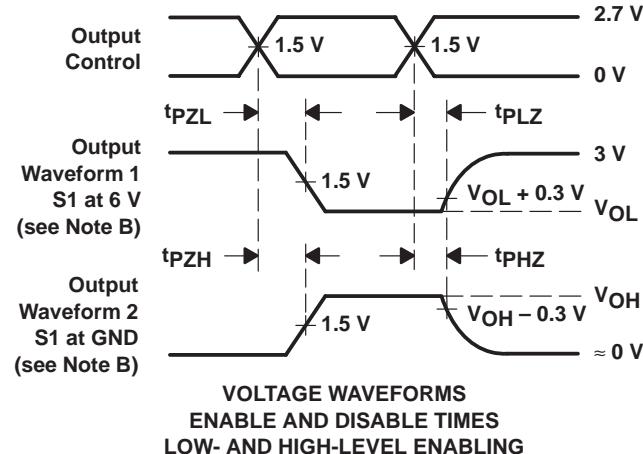
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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