CMOS LSI

LC74795, 74795M

On-Screen Display Controller LSI

Preliminary

Overview

The LC74795 and LC74795M are CMOS LSIs for on-screen display, a function that displays characters and patterns on a TV screen under microprocessor control. They feature a built-in PDC/VPS/UDT interface circuit. These LSIs support 12 × 18 dot characters and can display 12 lines by 24 characters of text.

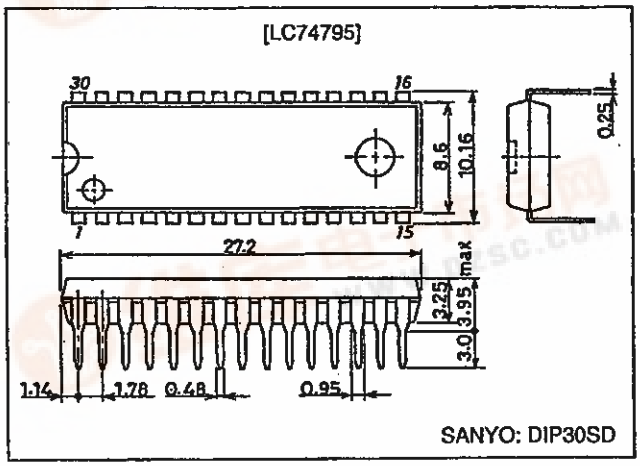
Features

- Display format: 24 characters by 12 rows (Up to 288 characters)
- Character format: 12 (horizontal) × 18 (vertical) dots
- Character sizes: Three sizes each in the horizontal and vertical directions
- Characters in font: 128
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable in character units
- Blinking types: Two periods supported: 1.0 second and 0.5 second
- Blanking: Over the whole font (12 × 18 dots)
- Background color
  - — Background coloring: 8 colors (internal synchronization mode): 4fsc
  - — Background coloring: 6 colors (internal synchronization mode): 2fsc
- Line background color
  - — Can be set for 3 lines
  - — Line background coloring: 8 colors (internal synchronization mode): 4fsc
  - — Line background coloring: 6 colors (internal synchronization mode): 2fsc
  - — Blue background only: NTSC
- External control input: 8-bit serial input format
- Sync separator circuit and AFC circuit
- PDC/VPS/UDT interface circuit that supports the I²C bus
- Composite video output in the PAL or NTSC format

Package Dimensions

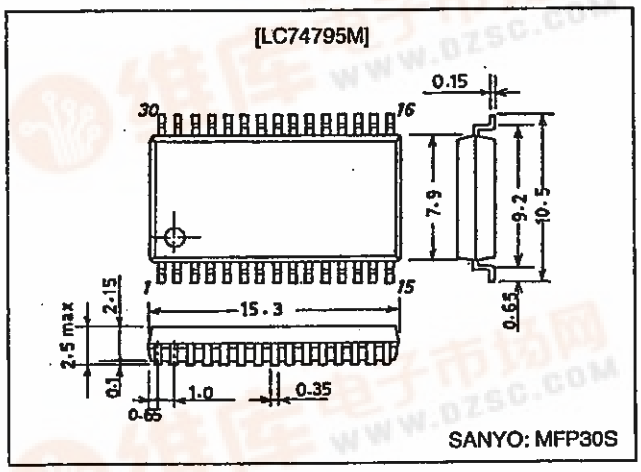
unit: mm

3196-DIP30SD

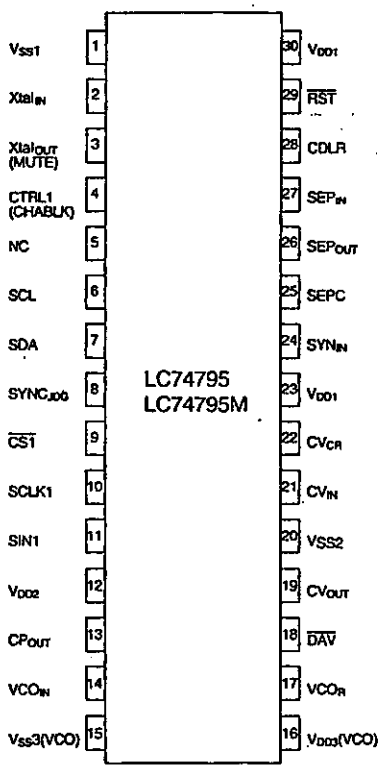


unit: mm

3216A-MFP30S



Pin Assignment



Top view

A05053

Pin Functions

Pin no.	Pin	Function	Notes
1	V_{SS}	Ground	Ground connection (digital system ground)
2	$Xtal_{IN}$	Crystal oscillatoR (MUTE input)	These pins are used either to connect the crystal and capacitor used to form an external crystal oscillator used to generate the internal synchronizing signals, or to input and external clock signal (2fsc or 4fsc). As a mask option, the X'talout pin can be set to function as the MUTE input pin. When this pin is set low, the video output is held at the pedestal level. (A pull-up resistor is built in and the input has hysteresis characteristics.)
3	$Xtal_{OUT}$ (MUTE)		
4	CTRL1 (CHABLK)	Crystal oscillator input switching (CHABLK output)	Switches the mode between external clock input and crystal oscillator operation. A low level selects crystal oscillator operation and a high level selects external clock input. As a mask option, the CTRL1 input pin can be set to function as the CHABLK (character * border) output. This is a 3-value output.
5	NC		Not connected
6	SCL	Clock input pin	Clock input for PDC/VPS data output. I²C bus.
7	SDA	Data input/output pin	PDC/VPS data input/output pin. I²C bus. Address [XXXX XXXX] Write address: 0111 1100 Read address: 0111 1101
8	$SYNC_{JDG}$	External synchronizing signal judgment output	Outputs the state of the external synchronizing signal presence/absence judgment. Outputs a high level when synchronizing signals are present. Outputs the crystal oscillator clock when $\overline{CS1}$ is low and $\overline{RST}$ is low. (This signal is not output on command resets.)
9	$\overline{SCI}$	Enable input 1	Enable input pin for the OSD serial data input function. Serial data input is enabled when this pin is low. A pull-up resistor is built in and the input has hysteresis characteristics.
10	SCLK1	Clock input 1	Input for the serial data input clock. A pull-up resistor is built in. (The input has hysteresis characteristics.)
11	SIN1	Data input 1	Serial data input. A pull-up resistor is built in. (The input has hysteresis characteristics.)
12	$V_{DD}2$	Power supply	Composite video signal level adjustment power supply (analog system power supply)
13	CP_{OUT}	Charge pump output	The charge pump output. Connect a low-pass filter to this pin.
14	VCO_{IN}	Oscillator control voltage input	Used for the VCO control voltage input.
15	$V_{SS}3$	Ground	Ground connection (VCO ground)

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Pin no.	Pin	Function	Notes
16	$V_{DD}3$	Power supply (+5 V)	The VCO power supply: +5 V
17	VCO_R	Oscillator range adjustment	Connection for the VCO oscillator range adjustment resistor
18	$\overline{DAV}$	Data present output	Outputs a low level when PDC/VPS data has been received.
19	CV_{OUT}	Video signal output	Composite video signal output
20	$V_{SS}2$	Ground	Ground connection (analog system ground)
21	CV_{IN}	Video signal input	Composite video signal input
22	CV_{CR}	Video signal input	SECAM chrominance signal input
23	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)
24	SYN_{IN}	Sync separator circuit input	Video signal output for the built-in sync separator circuit
25	SEPC	Sync separator circuit adjustment	Built-in sync separator circuit adjustment
26	SEP_{OUT}	Composite synchronizing signal output	Video signal output for the built-in sync separator circuit. Can be swithced to function as an output for signal (high or ST. pulse) due to MOD0 by setting SEL0 high.
27	SEP_{IN}	Vertical synchronizing signal input	Inputs the vertical synchronizing signal created by integrating the SEP_{OUT} pin output signal. An integration circuit must be connected to the SEP_{OUT} pin. This pin must be tied to $V_{DD}1$ if unused.
28	CDLR	Background color phase adjustment	Background color phase adjustment. Connect to ground through a resistor.
29	$\overline{RST}$	Reset input	System reset input A pull-up resistor is built in and the input has hysteresis characteristics.
30	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Specifications

Absolute Maximum at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	$V_{DD}max$	$V_{DD}1$ and $V_{DD}2$	$V_{SS}-0.3$ to $V_{SS}+7.0$	V
Input voltage	V_{IN}	All input pins	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output voltage	V_{OUT}	$\overline{DAV}$, SDA,, SEP_{OUT}, and $SYNC_{JDG}$	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Allowable power dissipation	Pd max		350	mW
Operating temperature	Topr		−30 to + 70	°C
Storage temperature	Tstg		−40 to + 125	°C

Allowable Operating Ranges at Ta = −30 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	$V_{DD}1$ and $V_{DD}2$	4.5	5.0	5.5	V
	$V_{DD}2$	$V_{DD}2$	4.5	5.0	$1.27V_{DD}1$	V
Input high-level voltage	$V_{IH}1$	$\overline{RST}$, $\overline{CS1}$, SIN1, SCLK1, MUTE, SCL, and SDA	$0.8V_{DD}1$		$V_{DD}1+0.3$	V
	$V_{IH}2$	CTRL1	$0.7V_{DD}1$		$V_{DD}1+0.3$	V
Input low-level voltage	$V_{IL}1$	$\overline{RST}$, $\overline{CS1}$, SIN1, SCLK1, MUTE, SCL, and SDA	$V_{SS}-0.3$		$0.2V_{DD}1$	V
	$V_{IL}2$	CTRL1	$V_{SS}-0.3$		$0.3V_{DD}1$	V
Pull-up resistance	R_{PU}	Applies to pins set for the $\overline{RST}$, $\overline{CS1}$, SIN1, SCLK1, and MUTE pin options.	25	50	90	kΩ
Composite video signal input voltage	$V_{IN}1$	CV_{IN}, CV_{CR}; $V_{DD}1 = 5$ V		2.0		Vp-p
	$V_{IN}2$	SYN_{IN}; $V_{DD}1 = 5$ V	1.5	2.0	2.5	Vp-p
Input voltage	$V_{IN}3$	$Xtal_{IN}$ (When external clock input is used) f_{in} = 2 fsc or 4 fsc ; $V_{DD}1 = 5$ V	0.10		5.0	Vp-p
Oscillator frequency	$F_{OSC}1$	The $Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (2 fsc: PAL)		8.867		MHz
	$F_{OSC}2$	The $Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (4 fsc: PAL)		17.734		MHz

Note: When the $Xtal_{IN}$ pin is used in clock input mode, extreme care must be taken to prevent noise from entering the input signal.

Electrical Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 V unless otherwise specified.

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Input off leakage current	$I_{leak}1$	CV_{IN}, CV_{CR}			1	μA
Output off leakage current	$I_{leak}2$	CV_{OUT}			1	μA
Output high-level voltage	V_{OH}	$\overline{DAV}$, SEP_{OUT}, CP_{OUT}, and $SYNC_{JDG}$; $V_{DD}1$ = 4.5 V, I_{OH} = –1.0 mA	3.5			V
Output low-level voltage	$V_{OL}1$	$\overline{DAV}$, SEP_{OUT}, CP_{OUT}, and $SYNC_{JDG}$; $V_{DD}1$ = 4.5 V, I_{OL} = 1.0 mA			1.0	V
	$V_{OL}2$	SDA; $V_{DD}1$ = 5.0 V, I_{OL} = 3.0 mA			0.4	V
Three-value output voltage	V_O	CHABLK; $V_{DD}1$ = 5.0 V H	3.3		5.0	V
		M	1.8		2.3	V
		L	0		0.8	V
Input current	I_{IH}	$\overline{RST}$, $\overline{CST}$, SIN, SCLK1, SDA, SCL, CTRL1, MUTE, SEP_{IN}, and VCO_{IN}; V_{IN} = $V_{DD}1$			1	μA
	I_{IL}	SDA, SCL, CTRL1, SEP_{IN}, and VCO_{IN}; V_{IN} = $V_{SS}1$	–1			μA
Operating mode current drain	$I_{DD}1$	$V_{DD}1$; All outputs open, Xtal: 17.734 MHz, VCO: 27 MHz			40	mA
	$I_{DD}2$	$V_{DD}2$: $V_{DD}2$ = 5 V			20	mA
SYNC level	V_{SN}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V *1		0.80		V
		*2		1.00		V
		*3		1.30		V
Pedestal level	V_{PD}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V *1		1.37		V
		*2		1.57		V
		*3		1.87		V
Color burst low level	V_{CBL}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V *1		1.07		V
		*2		1.27		V
		*3		1.57		V
Color burst high level	V_{CBH}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V *1		1.67		V
		*2		1.87		V
		*3		2.17		V
Background color low level	V_{RSL}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V *1		1.23 (1.16)		V
		*2		1.43 (1.36)		V
		*3		1.73 (1.66)		V
Background color high level	V_{RSH}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V *1		2.37 (2.01)		V
		*2		2.57 (2.21)		V
		*3		2.87 (2.51)		V
Frame level 0	$V_{BK}0$	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V *1		1.50		V
		*2		1.70		V
		*3		2.00		V
Frame level 1	$V_{BK}1$	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V *1		2.08		V
		*2		2.28		V
		*3		2.58		V
Character level	V_{CHA}	CV_{OUT}; $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V *1		2.65		V
		*2		2.85		V
		*3		3.15		V

Notes: 1. When the sync level is 0.8 V
2. When the sync level is 1.0 V
3. When the sync level is 1.3 V
The values in parentheses for the background high and low levels apply when the background color is blue.

Timing Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 ±0.5 V

OSD Write (See Figure 1.)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_{W(SCLK)}$	SCLK1	200			ns
	$t_{W(CS1)}$	$\overline{CS1}$ (The period when $\overline{CS1}$ is high)	1			µs
Data setup time	$t_{SU(CS1)}$	$\overline{CS1}$	200			ns
	$t_{SU(SIN)}$	SIN1	200			ns
Data hold time	$t_{h(CS1)}$	$\overline{CS1}$	2			µs
	$t_{h(SIN)}$	SIN1	200			ns
One word write time	t_{word}	The time to write 8 bits of data	4.2			µs
	t_{WI}	The RAM data write time	1			µs

PDC/VPS Write and Read (I²C timing)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SCL frequency	f_{SCL}				100	kHz
Bus release time	t_{BUF}		4.7			µs
Start/hold	t_{HD}; STA		4.0			µs
SCL low period	t_{LOW}		4.7			µs
SCL high period	t_{HIGH}		4.0			µs
Data hold	t_{HD}; DAT		0			µs
Data setup	t_{SU}; DAT		250			ns
Rise time	t_R				1000	ns
Fall time	t_F				300	ns
Stop setup	t_{SU}; STO		40			µs

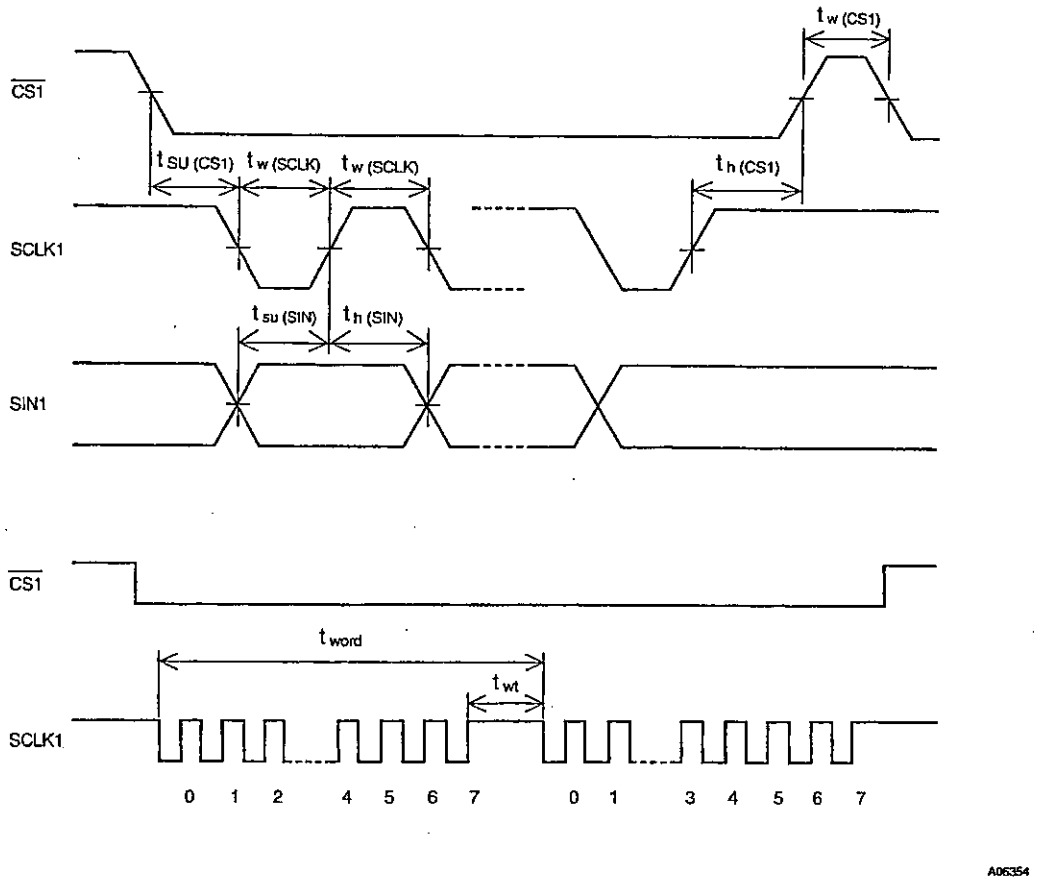


Figure 1 OSD Serial Data Input Timing

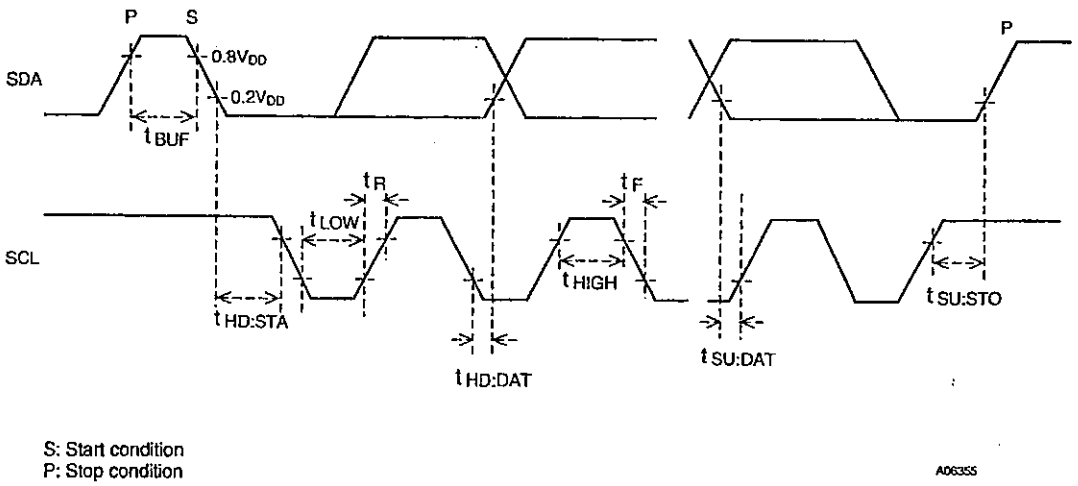
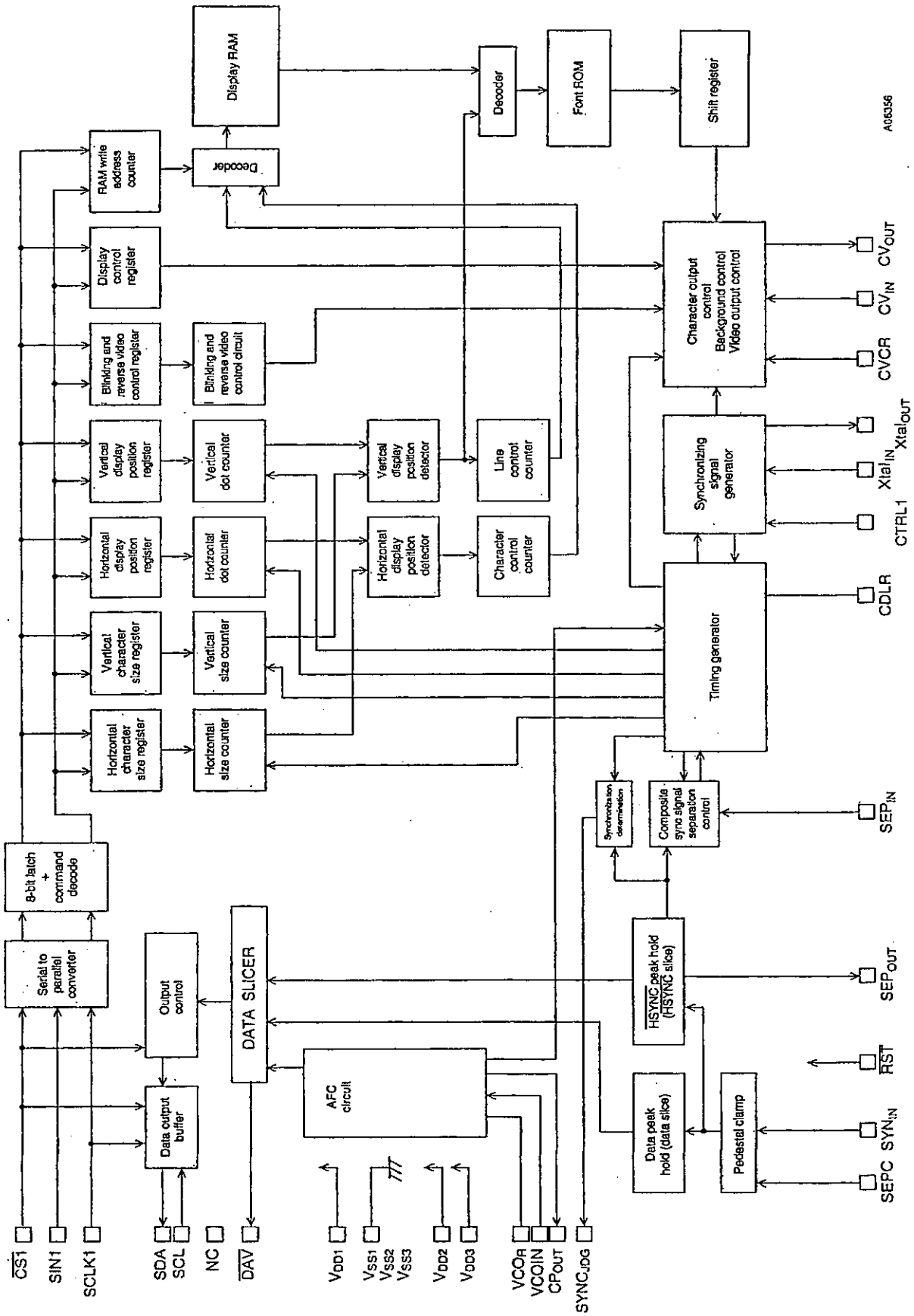


Figure 2 PDC/VPS Serial Timing (I²C bus)

System Block Diagram



Display Control Commands

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes. The following commands are supported.

1 COMMAND0: Display memory (VRAM) write address setup command
2 COMMAND1: Display character data write command
3 COMMAND2: Vertical display start position and vertical character size setup command
4 COMMAND3: Horizontal display start position and horizontal character size setup command
5 COMMAND4: Display control setup command
6 COMMAND5: Display control setup command
7 COMMAND6: Synchronizing signal detection setup command
8 COMMAND7 to 12: Display control setup command
9 COMMAND13 to 17: VPS/PDC commands [Only via I²C writes]

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Write address setup	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Character write	1	0	0	1	0	0	0	0	at	c6	c5	c4	c3	c2	c1	c0
COMMAND2 Vertical character size and vertical display start position	1	0	1	0	VS 21	VS 20	VS 11	VS 10	0	FS	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 Horizontal character size and horizontal display start position	1	0	1	1	HS 21	HS 20	HS 11	HS 10	0		HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 Display control	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	BLK 2	BLK 1	BLK 0	BK 1	BK 0	RV	DSP ON
COMMAND5 Display control	1	1	0	1	NP1	NP0	NON	INT	0	0	HLF INT	BCL	CB	PH 2	PH 1	PH 0
COMMAND6 Synchronizing signal detection	1	1	1	0	SEL 0	MOD 0	DIS LIN	MUT	0	RN 2	RN 1	RN 0	SN 3	SN 2	SN 1	SN 0
COMMAND7 Display control	1	1	1	1	0	0	0	0	0	CIN SEL	CIN CTL	VNP SEL	VSP SEL	MSK ERS	MSK SEL	EGL
COMMAND8 Display control	1	1	1	1	0	0	0	1	0	LNA 3	LNA 2	LNA 1	LNA 0	LPA 2	LPA 1	LPA 0
COMMAND9 Display control	1	1	1	1	0	0	1	0	0	LNB 3	LNB 2	LNB 1	LNB 0	LPB 2	LPB 1	LPB 0
COMMAND10 Display control	1	1	1	1	0	0	1	1	0	LNC 3	LNC 2	LNC 1	LNC 0	LPC 2	LPC 1	LPC 0
COMMAND11 Display control	1	1	1	1	0	1	0	0	0	0	0	0	LNC SEL	MOD 3	LNB SEL	MOD 2
COMMAND12 Display control	1	1	1	1	0	1	0	1	0	0	0	0	0	SEL 2	SEL 1	CTL 3
COMMAND13 (VPS/PDC control)	1	1	1	1	0	1	0	1	0	CPA 1	CPA 0	0	VPM 3	VPM 2	VPM 1	VPM 0
COMMAND14 (VPS/PDC control)	1	1	1	1	0	1	1	0	0	0	0	HBS 2	HBS 1	BMS	EMS	DCE
COMMAND15 (VPS/PDC control)	1	1	1	1	0	1	1	1	0	0	ECV 15	ECV 14	ECV 13	ECV 12	ECV 11	ECV 5
COMMAND16 (VPS/PDC control)	1	1	1	1	1	0	0	0	0	ECP 19	ECP 18	ECP 17	ECP 16	ECP 15	ECP 14	ECP 13
COMMAND17 (VPS/PDC control)	1	1	1	1	1	0	0	1	0	0	ECP 25	ECP 24	ECP 23	ECP 22	ECP 21	ECP 20

Once written, the command identification code in the first byte is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74795/M locks into the display character data write mode, and another first byte cannot be written.

When the $\overline{CS1}$ pin is set high, the LC74795/M is set to the COMMAND0 (display memory write address setup mode) state.

COMMAND0 (Display memory write address setup command)
First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 0 Identification code Sets the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory line address (0 to B hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification code	
6	—	0		
5	—	0		
4	H4	0	Display memory column address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND1 (Display character data write setup command)
First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 1 Identification code Sets up display character data write mode.	When this command is input, the LC74795/M locks in the display character data write mode until the $\overline{CS1}$ pin goes high.
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	—	0		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	at	0	Character attribute off	
		1	Character attribute on	
6	c6	0	Character code (00 to 7F hexadecimal)	
		1		
5	c5	0		
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND2 (Vertical display start position and vertical character size setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 2 identification code Sets the vertical display start position and the vertical character size.	
6	—	0		
5	—	1		
4	—	0		
3	VS21	0	VS21 \ VS20: 0 / 1 0: 1H/dot / 2H/dot 1: 3H/dot / 1H/dot	Second line vertical character size
		1		
2	VS20	0		
		1		
1	VS11	0	VS11 \ VS10: 0 / 1 0: 1H/dot / 2H/dot 1: 3H/dot / 1H/dot	First line vertical character size
		1		
0	VS10	0		
		1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	FS	0	Crystal oscillator frequency: 2fsc	
		1	Crystal oscillator frequency: 4fsc	
5	VP5 (MSB)	0	If VS is the vertical display start position then: $VS = H \times (2 \sum_{n=0}^{5} 2^n VP_n)$ H: the horizontal synchronization pulse period	The vertical display start position is set by the 6 bits VP0 to VP5. The weight of bit 1 is 2H.
		1		
4	VP4	0		
		1		
3	VP3	0		
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND3 (Horizontal display start position and horizontal size setup command)
First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 3 identification code Sets the horizontal display start position and the horizontal character size.	
6	—	0		
5	—	1		
4	—	1		
3	HS21	0		Second line horizontal character size
		1		
2	HS20	0		
		1		
1	HS11	0		First line horizontal character size
		1		
0	HS10	0		
		1		

HS21 \ HS20	0	1
0	1Tc/dot	2Tc/dot
1	3Tc/dot	1Tc/dot

HS11 \ HS10	0	1
0	1Tc/dot	2Tc/dot
1	3Tc/dot	1Tc/dot

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LC	0		The horizontal display start position is set by the 6 bits HP0 to HP5. The weight of bit 1 is 2Tc.
5	HP5 (MSB)	0	If HS is the horizontal start position then: $HS = Tc \times (2 \sum_{n=0}^{5} 2^n HP_n)$ Tc: Period of the oscillator in operating mode.	
		1		
4	HP4	0		
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND4 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 4 identification code Display control setup	
6	—	1		
5	—	0		
4	—	0		
3	TSTMOD	0	Normal operating mode	This bit must be set to 0.
		1	Test mode	
2	RAMERS	0		Erasing RAM takes about 500 µs. (This operation must be executed in the DSPOFF state.)
		1	Erase display RAM. (Set the RAM data to 7F hexadecimal.)	
1	OSCSTP	0	Do not stop the crystal and VCO oscillators.	Valid in external synchronization mode when character display is off. Note that VPS/PDC data cannot be detected in this mode.
		1	Stop the crystal and VCO oscillators.	
0	SYSRST	0		The registers are reset when the $\overline{CST}$ pin is low, and the reset state is cleared when $\overline{CST}$ is set high.
		1	Reset all registers and turn display off.	

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	BLK2	0	Character display area	Specifies the size for complete fil-in
		1	Video display area	
5	BLK1	0		Changes the blanking size
		1		
4	BLK0	0		
		1		

BLK1 \ BLK0	0	1
0	Blanking off	Character size
1	Border size	Complete fill in

DA 0 to 7	Register	Contents		Notes
		State	Function	
3	BK1	0	Blinking period: About 0.5 s	Switches the blinking period
		1	Blinking period: About 1.0 s	
2	BK0	0	Blinking off	Blinking in reverse video mode switches the display between normal character display and reverse video display.
		1	Blinking on	
1	RV	0	Reverse video off	
		1	Reverse video on	
0	DSPON	0	Character display off	
		1	Character display on	

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND5 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 5 Identification code Display control setup	
6	—	1		
5	—	0		
4	—	1		
3	NP1	0		Switches between NTSC and PAL modes. ( ) external input V
		1		
2	NP0	0		
		1		
1	NON	0	Interlaced	Switches between interlaced and noninterlaced video.
		1	Noninterlaced	
0	INT	0	External synchronization	Switches between external and internal synchronization
		1	Internal synchronization	

NP1 \ NP0	0	1
0	NTSC (525)	NTSC (625)
1	PAL (525)	PAL (625)

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	HLFINT	0	Normal mode	
		1	Half internal synchronization mode	
4	BCL	0	Background coloring on	Only valid in internal synchronization mode
		1	No background coloring (Only the background level is set)	
3	CB	0	Color burst signal output	Only valid when BCL is high.
		1	Color burst signal output stopped	
2	PH2	0		Background color specification
		1		
1	PH1	0		
		1		
0	PH0	0		
		1		

PH2	PH1	PH0	Background color (phase)
0	0	0	Cyan *
0	0	1	Yellow *
0	1	0	Red *
0	1	1	Blue *
1	0	0	Cyan - blue
1	0	1	Green *
1	1	0	Orange
1	1	1	Magenta *

*: When 2 fsc is used.

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND6 (Synchronizing signal detection setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 6 identification code Sets up synchronizing signal control.	
6	—	1		
5	—	1		
4	—	0		
3	SEL0	0	Sync separator signal	Switches the SEP_{OUT} (pin 26) output.
		1	Output signal set by MOD0	
2	MOD0	0	High-level output	Only valid when SEL0 is high.
		1	ST pulse signal	
1	DISLIN	0	12 lines	Switches the number of lines displayed.
		1	10 lines	
0	MUT	0	Normal output	CV_{OUT} switching
		1	CV_{IN} is cut and CV_{OUT} is held at the pedestal level.	

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	RN2	0		External synchronizing signal detection control Signal absent → signal present transition detection Sets the sampling period in which SYNC can be detected continuously in the horizontal synchronizing signal period (1H).
		1		
5	RN1	0		
		1		
4	RN0	0		
		1		

RN2	RN1	RN0	Number of times HSYNC detected
0	0	0	0 times
0	0	1	4 times
0	1	0	8 times
1	0	0	16 times

DA 0 to 7	Register	State	Notes
3	SN3	0	External synchronizing signal detection control Signal present → signal absent transition detection Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).
		1	
2	SN2	0	
		1	
1	SN1	0	
		1	
0	SN0	0	
		1	

SN3	SN2	SN1	SN0	Number of times HSYNC detected
0	0	0	0	Not detected
0	0	0	1	32 times
0	0	1	0	64 times
0	1	0	0	128 times
1	0	0	0	256 times

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND7 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended 0 identification code	
2	—	0		
1	—	0		
0	—	0		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	CINSEL	0	Blank area (the logical OR of the character and frame signals)	CV_{CR} on signal switching
		1	Video signal display area	
5	CINCTL	0	CV_{CR}: Off	Turns CV_{CR} on or off.
		1	CV_{CR}: On	
4	VNPSEL	0	V falling edge detection	Switches the V acquisition polarity in external mode when internal V separation is used.
		1	V rising edge detection	
3	VSPSEL	0	VSEP: about 8.9 μs (NTSC)	Switches the internal V separation period.
		1	VSEP: about 17.8 μs (NTSC)	
2	MSKERS	0	Mask valid	Clears the HSYNC and VSYNK masks.
		1	Mask invalid	
1	MSKSEL	0	3H (NTSC)	Switches the VSYNC mask.
		1	20H (NTSC)	
0	EGL	0	Border level 0 only (VBK0)	Switches the border level. (Only valid when BLK0 is 0 and BLK1 is 1.)
		1	Two-stage border level (VBK0 and VBK1)	

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND8 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended 1 identification code	
2	—	0		
1	—	0		
0	—	1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LNA3	0		Specifies the line whose background is to be changed (Specification of LNA*, LNB*, and LNC* on the same line is not allowed.)
		1		
5	LNA2	0		
		1		
4	LNA1	0		
		1		
3	LNA0	0		
		1		
2	LPA2	0		Specifies the background color.
		1		
1	LPA1	0		
		1		
0	LPA0	0		
		1		

LNA3	LNA2	LNA1	LNA0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	—	—	Line 12

LPA2	LPA1	LPA0	Background color (phase)
0	0	0	Cyan *
0	0	1	Yellow *
0	1	0	Red *
0	1	1	Blue *
1	0	0	Cyan - blue
1	0	1	Green *
1	1	0	Orange
1	1	1	Magenta *

*: When 2 fsc is used.

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND9 (Display control setup command)
First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended 2 identification code	
2	—	0		
1	—	1		
0	—	0		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LNB3	0		Specifies the line whose background is to be changed (Specification of LNA*, LNB*, and LNC* on the same line is not allowed.)
		1		
5	LNB2	0		
		1		
4	LNB1	0		
		1		
3	LNB0	0		
		1		
2	LPB2	0		Specifies the background color.
		1		
1	LPB1	0		
		1		
0	LPB0	0		
		1		

LNB3	LNB2	LNB1	LNB0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	—	—	Line 12

LPB2	LPB1	LPB0	Background color (phase)
0	0	0	Cyan *
0	0	1	Yellow *
0	1	0	Red *
0	1	1	Blue *
1	0	0	Cyan - blue
1	0	1	Green *
1	1	0	Orange
1	1	1	Magenta *

*: When 2 fsc is used.

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND10 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended 3 identification code	
2	—	0		
1	—	1		
0	—	1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LNC3	0		Specifies the line whose background is to be changed (Specification of LNA*, LNB*, and LNC* on the same line is not allowed.)
		1		
5	LNC2	0		
		1		
4	LNC1	0		
		1		
3	LNC0	0		
		1		
2	LPC2	0		Specifies the background color.
		1		
1	LPC1	0		
		1		
0	LPC0	0		
		1		

LNC3	LNC2	LNC1	LNC0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	—	—	Line 12

LPC2	LPC1	LPC0	Background color (phase)
0	0	0	Cyan *
0	0	1	Yellow *
0	1	0	Red *
0	1	1	Blue *
1	0	0	Cyan - blue
1	0	1	Green *
1	1	0	Orange
1	1	1	Magenta *

*: When 2 fsc is used.

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND11 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended 4 identification code	
2	—	1		
1	—	0		
0	—	0		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	—	0		
3	LNCSEL	0	Normal line background color operation	Switches the background color in RV mode for RV specified characters on LNB* specified lines.
		1	RV characters have the color of the PH* specified background color and RV characters have a white background.	
2	MOD3	0	The specifications when LNCSEL is set to 1.	Valid when LNCSEL is high.
		1	RV characters have the background color specified by PH* and the RV characters themselves are white.	
1	LNBSEL	0	Normal line background color operation	Switches the background color in RV mode for RV specified characters on LNB* specified lines.
		1	RV characters have the color of the PH* specified background color and RV characters have a white background.	
0	MOD2	0	The specifications when LNBSEL is set to 1.	Valid when LNBSEL is high.
		1	RV characters have the background color specified by PH* and the RV characters themselves are white.	

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND12 (Display control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended 5 identification code	
2	—	1		
1	—	0		
0	—	1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	—	0		
3	—	0		
2	SEL2	0	External synchronizing signal judgment output signal	Switches the $SYNC_{JDG}$ (pin 8) output.
		1	$\overline{O/E}$ signal	
1	SEL1	0	Internal slice data	When set to 1, the data is input from SEP_{IN} (pin 27).
		1	External slice data	
0	CTL3	0	Internal V separation used	V separation switching
		1	Internal V separation not used	

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND13 (VPS/PDC control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended 5 identification code	
2	—	1		
1	—	0		
0	—	1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	CPA1	0		Data acquisition clock switching
		1		
5	CPA0	0		
		1		
4	—	0		
3	VPM3	0		
		1		
2	VPM2	0		
		1		
1	VPM1	0		
		1		
0	VPM0	0		
		1		

CPA1	CPA0	Clock
0	0	No. 1
0	1	No. 2
1	0	No. 3
1	1	No. 4

VPM3	VPM2	VPM1	VPM0	Operating mode
0	0	0	0	VPS
0	0	0	1	8/30/2 (PDC)
0	0	1	0	Automatic PDC and VPS switching
0	0	1	1	8/30/1 (UDT)
0	1	0	0	Header time 1
0	1	0	1	Header time 2
0	1	1	0	Header time 3
0	1	1	1	Header time 4
1	0	0	0	Status display 1
1	0	0	1	Status display 2
1	0	1	0	Status display 3
1	0	1	1	Status display 4

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND14 (VPS/PDC control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended 6 identification code	
2	—	1		
1	—	1		
0	—	0		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	HBS2	0	Discrimination mode 1	Clock line
		1	Discrimination mode 2	
3	HBS1	0	Discrimination mode 1	Framing code
		1	Discrimination mode 2	
2	BMS	0	Error checking enabled (Error checking can be turned on or off on a per-byte basis.)	When 0, bytes for which error checking is specified and that have no errors are written to P-S. When 1, all bytes are written to P-S regardless of errors.
		1	Error checking disabled (Applications can select whether to hold or write data with errors on a per-byte basis.)	
1	EMS	0	Data hold	The handling at bytes for which error checking is turned off when error checking is enabled
		1	Data write (In VPS mode, the error bit is set to 0.)	
0	DCE	0	Error checking turned on for data unused bytes. VPS: bytes 3, 4, and 6 to 10. PDCC (8/30/2): bytes 7 to 12. Header 1: bytes 14 to 37. Header 2: bytes 14 to 29, Header 3: bytes 14 to 21. Status 1 (3): bytes 7 to 25. Status 2 (4): bytes 7 to 35.	Error checking specification for bytes whose data is unused Bi-phase (VPS), Hamming (PDC), or odd parity (header)
		1	Error checking turned off for data unused bytes. VPS: bytes 3, 4, and 6 to 10. PDCC (8/30/2): bytes 7 to 12. Header 1: bytes 14 to 37. Header 2: bytes 14 to 29, Header 3: bytes 14 to 21. Status 1 (3): bytes 7 to 25. Status 2 (4): bytes 7 to 35.	

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND15 (VPS/PDC control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended 7 identification code	
2	—	1		
1	—	1		
0	—	1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	ECV15	0	Byte 15 bi-phase error check on (data held)	Settings when the VPS data BMS = 0. Settings in parentheses apply when BMS = 1.
		1	Byte 15 bi-phase error check off (data written)	
4	ECV14	0	Byte 14 bi-phase error check on (data held)	
		1	Byte 14 bi-phase error check off (data written)	
3	ECV13	0	Byte 13 bi-phase error check on (data held))	
		1	Byte 13 bi-phase error check off (data written)	
2	ECV12	0	Byte 12 bi-phase error check on (data held)	
		1	Byte 12 bi-phase error check off (data written)	
1	ECV11	0	Byte 11 bi-phase error check on (data held)	
		1	Byte 11 bi-phase error check off (data written)	
0	ECV5	0	Byte 5 bi-phase error check on (data held)	
		1	Byte 5 bi-phase error check off (data written)	

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND16 (VPS/PDC control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended 8 identification code	
2	—	0		
1	—	0		
0	—	0		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	ECP19	0	Byte 19 Hamming error check on (data held) {Byte 44, 28, 36, 20, 32, 42, 32, and 42}	Settings when the PDC data (8/30/2) BMS = 0. Settings in parentheses apply when BMS = 1. The items in curly brackets are the bytes for which the odd parity check is turned on and off in header modes 1, 2, 3, and 4 and status modes 1, 2, 3, and 4, respectively.
		1	Byte 19 Hamming error check off (data written) {Byte 44, 28, 36, 20, 32, 42, 32, and 42}	
5	ECP18	0	Byte 18 Hamming error check on (data held) {Byte 43, 27, 35, 19, 31, 41, 31, and 41}	
		1	Byte 18 Hamming error check off (data written) {Byte 43, 27, 35, 19, 31, 41, 31, and 41}	
4	ECP17	0	Byte 17 Hamming error check on (data held) {Byte 42, 26, 34, 18, 30, 40, 30, and 40}	
		1	Byte 17 Hamming error check off (data written) {Byte 42, 26, 34, 18, 30, 40, 30, and 40}	
3	ECP16	0	Byte 16 Hamming error check on (data held) {Byte 41, 25, 33, 17, 29, 39, 29, and 39}	
		1	Byte 16 Hamming error check off (data written) {Byte 41, 25, 33, 17, 29, 39, 29, and 39}	
2	ECP15	0	Byte 15 Hamming error check on (data held) {Byte 40, 24, 32, 16, 28, 38, 28, and 38}	
		1	Byte 15 Hamming error check off (data written) {Byte 40, 24, 32, 16, 28, 38, 28, and 38}	
1	ECP14	0	Byte 14 Hamming error check on (data held) {Byte 39, 23, 31, 15, 27, 37, 27, and 37}	
		1	Byte 14 Hamming error check off (data written) {Byte 39, 23, 31, 15, 27, 37, 27, and 37}	
0	ECP13	0	Byte 13 Hamming error check on (data held) {Byte 38, 22, 30, 14, 26, 36, 26, and 36}	
		1	Byte 13 Hamming error check off (data written) {Byte 38, 22, 30, 14, 26, 36, 26, and 36}	

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

COMMAND17 (VPS/PDC control setup command)

First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code Display control setup	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended 9 identification code	
2	—	0		
1	—	0		
0	—	1		

Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	ECP25	0	Byte 25 Hamming error check on (data held)	Settings when the PDC data (8/30/2) BMS = 0. Settings in parentheses apply when BMS = 1. The items in curly brackets are the bytes for which the odd parity check is turned off in header modes 1, 2, 3, and 4 and status modes 1, 2, 3, and 4, respectively.
		1	Byte 25 Hamming error check off (data written)	
4	ECP24	0	Byte 24 Hamming error check on (data held)	
		1	Byte 24 Hamming error check off (data written)	
3	ECP23	0	Byte 23 Hamming error check on (data held)	
		1	Byte 23 Hamming error check off (data written)	
2	ECP22	0	Byte 22 Hamming error check on (data held) {Byte ,,, 35, 45, 35, and 45}	
		1	Byte 22 Hamming error check off (data written) {Byte ,,, 35, 45, 35, and 45}	
1	ECP21	0	Byte 21 Hamming error check on (data held) {Byte ,,, 34, 44, 34, and 44}	
		1	Byte 21 Hamming error check off (data written) {Byte ,,, 34, 44, 34, and 44}	
0	ECP20	0	Byte 20 Hamming error check on (data held) {Byte 45, 29, 37, 21, 33, 43, 33, and 43})	
		1	Byte 20 Hamming error check off (data written) {Byte 45, 29, 37, 21, 33, 43, 33, and 43}	

Note: All registers are set to 0 when the LC74795/M is reset by the $\overline{RST}$ pin.

PDC/VPS Output Data Formats

Data is read out in order starting with bytes 1 and 7

Output data	PDC 8/30 mode		VPS mode	Header time mode 1 (3)	Header time mode 2 (4)
	Format1	Format2			
Byte 1 Bit 7	byte 15 bit 0	byte 16 bit 0	byte 11 bit 0	byte 38 bit 0	byte 22 bit 0
6	1	1	1	(30) 1	(14) 1
5	2	2	2	2	2
4	3	3	3	3	3
3	4	byte 17 bit 0	4	4	4
2	5	1	5	5	5
1	6	2	6	6	6
0	7	3	7	7	7
Byte 2 Bit 7	byte 16 bit 0	byte 18 bit 0	byte 12 bit 0	byte 39 bit 0	byte 23 bit 0
6	1	1	1	(31) 1	(15) 1
5	2	2	2	2	2
4	3	3	3	3	3
3	4	byte 19 bit 0	4	4	4
2	5	1	5	5	5
1	6	2	6	6	6
0	7	3	7	7	7
Byte 3 Bit 7	byte 17 bit 0	byte 20 bit 0	byte 13 bit 0	byte 40 bit 0	byte 24 bit 0
6	1	1	1	(32) 1	(16) 1
5	2	2	2	2	2
4	3	3	3	3	3
3	4	byte 21 bit 0	4	4	4
2	5	1	5	5	5
1	6	2	6	6	6
0	7	3	7	7	7
Byte 4 Bit 7	byte 18 bit 0	byte 22 bit 0	byte 14 bit 0	byte 41 bit 0	byte 25 bit 0
6	1	1	1	(33) 1	(17) 1
5	2	2	2	2	2
4	3	3	3	3	3
3	4	byte 23 bit 0	4	4	4
2	5	1	5	5	5
1	6	2	6	6	6
0	7	3	7	7	7
Byte 5 Bit 7	byte 19 bit 0	byte 14 bit 0	byte 5 bit 0	byte 42 bit 0	byte 26 bit 0
6	1	1	1	(34) 1	(18) 1
5	2	2	2	2	2
4	3	3	3	3	3
3	4	byte 15 bit 0	4	4	4
2	5	1	5	5	5
1	6	2	6	6	6
0	7	3	7	7	7
Byte 6 Bit 7	byte 20 bit 0	byte 24 bit 0	byte 15 bit 0	byte 43 bit 0	byte 27 bit 0
6	1	1	1	(35) 1	(19) 1
5	2	2	2	2	2
4	3	3	3	3	3
3	4	byte 25 bit 0	4	4	4
2	5	1	5	5	5
1	6	2	6	6	6
0	7	3	7	7	7

Continued on next page.

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Output data	PDC 8/30 mode		VPS mode	Header time mode 1 (3)	Header time mode 2 (4)
	Format1	Format2			
Byte 7 Bit 7	byte 21 bit 0	byte 13 bit 0	1	byte 44 bit 0	byte 28 bit 0
6	1	1	1	(36) 1	(20) 1
5	2	2	1	2	2
4	3	3	1	3	3
3	4	1	1	4	4
2	5	1	1	5	5
1	6	1	1	6	6
0	7	1	0	7	7
Byte 8 Bit 7	byte 13 bit 0	Error byte 16	Error byte 11	byte 45 bit 0	byte 29 bit 0
6	1	Information 1 17	Information 1 12	(37) 1	(21) 1
5	2	18	13	2	2
4	3	19	14	3	3
3	4	20	5	4	4
2	5	21	15	5	5
1	6	22	0	6	6
0	7	23	0	7	7
Byte 9 Bit 7	byte 14 bit 0	Error byte 14		Error byte 38 (30)	Error byte 22 (14)
6	1	Information 2 15		Information 39 (31)	Information 23 (15)
5	2	24		40 (32)	24 (16)
4	3	25		41 (33)	25 (17)
3	4	13		42 (34)	26 (18)
2	5	0		43 (35)	27 (19)
1	6	0		44 (36)	28 (20)
0	7	0		45 (37)	29 (21)
Byte 10 Bit 7	byte 22 bit 0				
6	1				
5	2				
4	3				
3	4				
2	5				
1	6				
0	7				
Byte 11 Bit 7	byte 23 bit 0				
6	1				
5	2				
4	3				
3	4				
2	5				
1	6				
0	7				
Byte 12 Bit 7	byte 24 bit 0				
6	1				
5	2				
4	3				
3	4				
2	5				
1	6				
0	7				
Byte 13 Bit 7	byte 25 bit 0				
6	1				
5	2				
4	3				
3	4				
2	5				
1	6				
0	7				

Bits for which there is no data setting are 1.

Data is read out in order starting with bytes 1 and 7
1, 2 : 8/30/2 3, 4 : 8/30/1

Output data	Status display mode 1 (3)	Status display mode 2 (4)
Byte 1 Bit 7	byte 26 bit 0	byte 36 bit 0
6	(26) 1	(36) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7
Byte 2 Bit 7	byte 27 bit 0	byte 37 bit 0
6	(27) 1	(37) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7
Byte 3 Bit 7	byte 28 bit 0	byte 38 bit 0
6	(28) 1	(38) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7
Byte 4 Bit 7	byte 29 bit 0	byte 39 bit 0
6	(29) 1	(39) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7
Byte 5 Bit 7	byte 30 bit 0	byte 40 bit 0
6	(30) 1	(40) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7
Byte 6 Bit 7	byte 31 bit 0	byte 41 bit 0
6	(31) 1	(41) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7
Byte 7 Bit 7	byte 32 bit 0	byte 42 bit 0
6	(32) 1	(42) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7

Output data	Status display mode 1 (3)	Status display mode 2 (4)
Byte 8 Bit 7	byte 33 bit 0	byte 43 bit 0
6	(33) 1	(43) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7
Byte 9 Bit 7	byte 34 bit 0	byte 44 bit 0
6	(34) 1	(44) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7
Byte 10 Bit 7	byte 35 bit 0	byte 45 bit 0
6	(35) 1	(45) 1
5	2	2
4	3	3
3	4	4
2	5	5
1	6	6
0	7	7
Byte 11 Bit 7	Error byte 26 (26)	Error byte 36 (36)
6	information 1 27 (27)	information 1 37 (37)
5	28 (28)	38 (38)
4	29 (29)	39 (39)
3	30 (30)	40 (40)
2	31 (31)	41 (41)
1	32 (32)	42 (42)
0	33 (33)	43 (43)
Byte 12 Bit 7	Error byte 34 (34)	Error byte 44 (44)
6	information 2 35 (35)	information 2 45 (45)
5	0	0
4	0	0
3	0	0
2	0	0
1	0	0
0	0	0
Byte 13 Bit 7		
6		
5		
4		
3		
2		
1		
0		

Bits for which there is no data setting are 1.

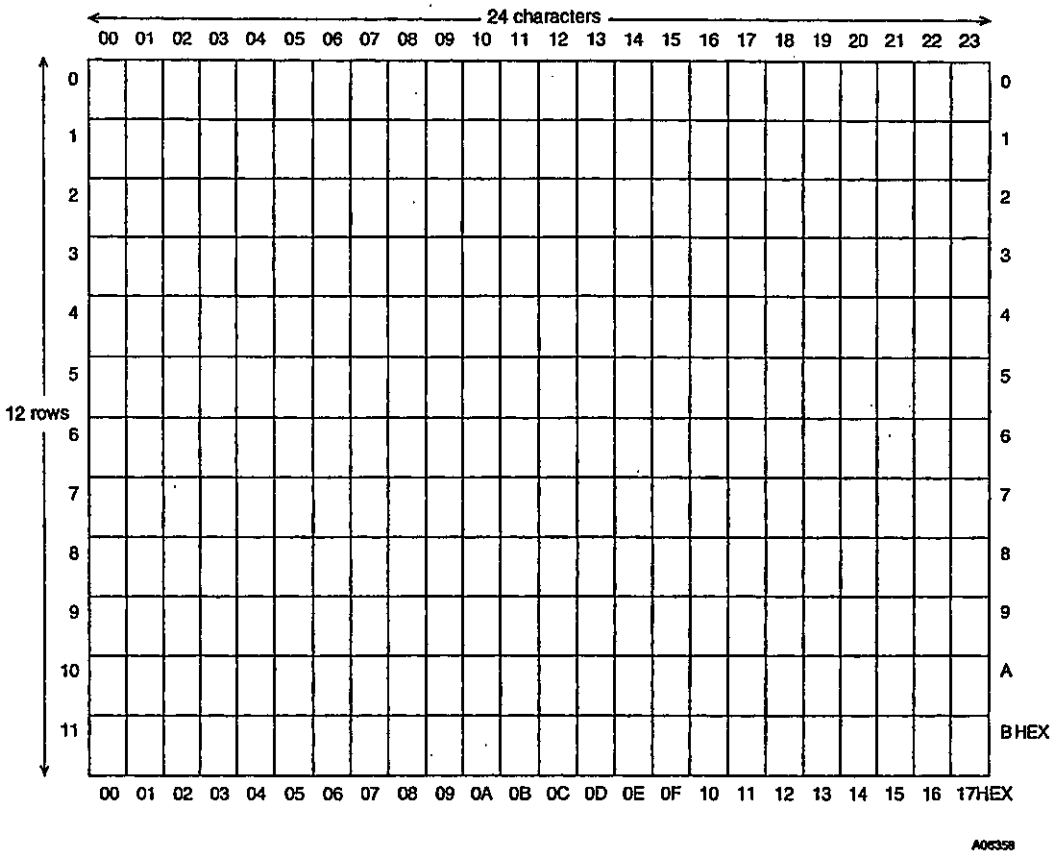
Display Screen Structure

The display consists of 12 lines of 24 characters.
Up to 288 characters can be displayed.
The number of characters that can be displayed is reduced from the normal total of 288 when enlarged characters are displayed.

Display memory addresses are specified as row (0 to B hexadecimal) and column (0 to 17 hexadecimal) addresses.

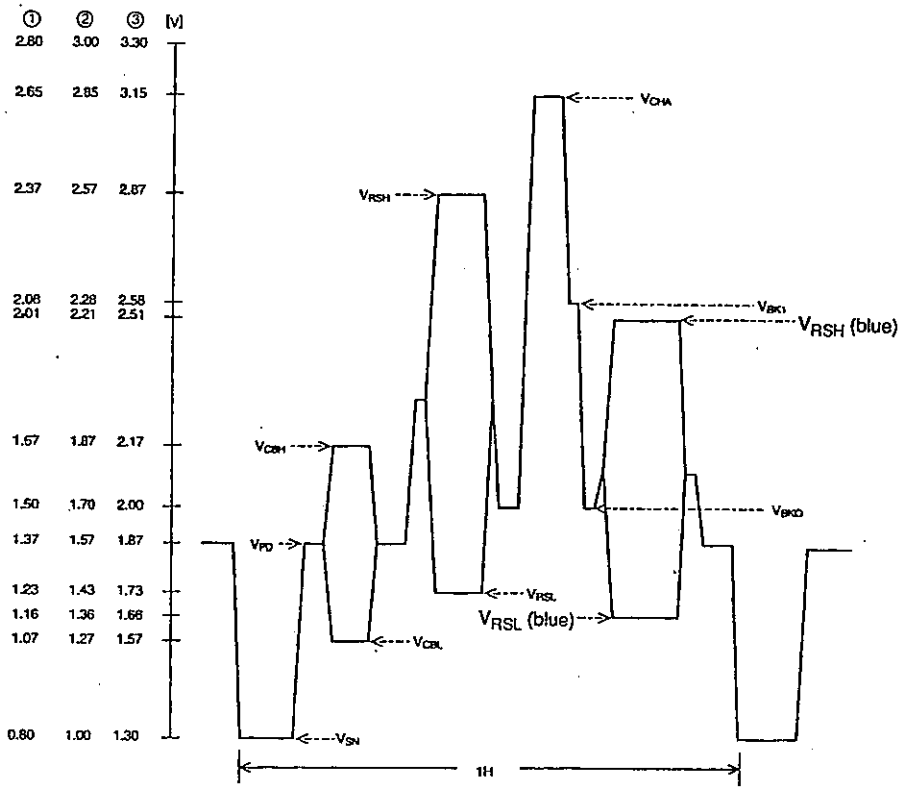
Display Screen Structure (display memory addresses)

24 characters × 12 rows



Composite Video Signal Output Levels (internally generated levels)

CV_{OUT} output level waveform ($V_{DD}2 = 5.00$ V)



Output level	Output voltage (1) [V]	Output voltage (2) [V]	Output voltage (3) [V]
V_{CHA}: Character	2.65	2.85	3.15
V_{RSH}: Background color high	2.37 (2.01)	2.57 (2.21)	2.87 (2.51)
V_{CBH}: Color burst high	1.67	1.87	2.17
V_{RSL}: Background color low	1.23 (1.16)	1.43 (1.36)	1.73 (1.66)
$V_{BK}1$: Border	2.08	2.28	2.58
$V_{BK}0$: Border	1.50	1.70	2.00
V_{PD}: Pedestal	1.37	1.57	1.87
V_{CBL}: Color burst low	1.07	1.27	1.57
V_{SN}: Sync	0.80	1.00	1.30

Note: $V_{DD}2 = 5.0$ V. Values in parentheses for V_{RSH} and V_{RSL} apply when the background color is blue.