

Typical Size
6,4 mm X 9,7 mm

TPS54873

SLVS444 – OCTOBER 2002

4-V TO 6-V INPUT, 8-A OUTPUT SYNCHRONOUS BUCK SWITCHER WITH DISABLED SINKING DURING START-UP

FEATURES

- 30-m Ω , 12-A Peak MOSFET Switches for High Efficiency at 8-A Continuous Output Source or Sink Current
- Disabled Current Sinking During Start-Up
- 0.9-V to 3.3-V Adjustable Output Voltage Range With 1.0% Accuracy
- Wide PWM Frequency: Fixed 350 kHz, 550 kHz or Adjustable 280 kHz to 700 kHz
- Synchronizable to 700 kHz
- Load Protected by Peak Current Limit and Thermal Shutdown
- Integrated Solution Reduces Board Area and Component Count

APPLICATIONS

- Low-Voltage, High-Density Distributed Power Systems
- Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors
- Broadband, Networking and Optical Communications Infrastructure
- Power PC Series Processors

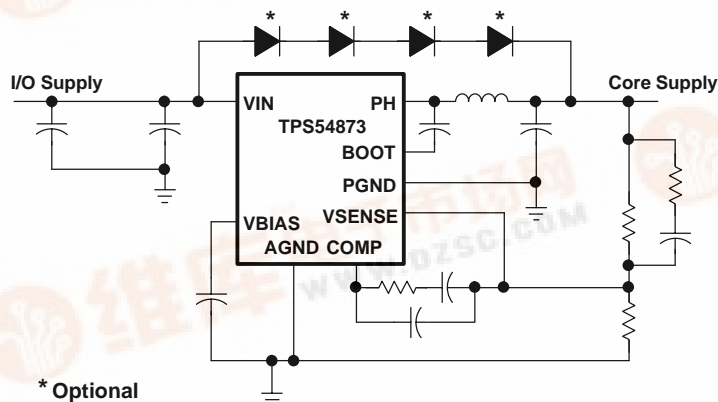
DESCRIPTION

As a member of the SWIFT™ family of dc/dc regulators, the TPS54873 low-input voltage high-output current synchronous buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 4 V; an internally or externally set slow-start circuit to limit inrush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

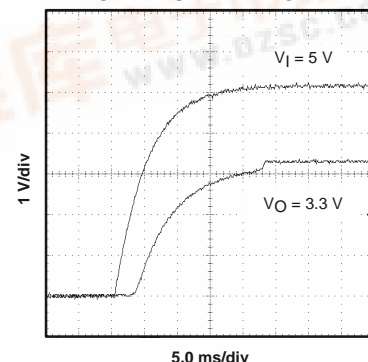
For reliable power up in output precharge applications, the TPS54873 is designed to only source current during startup.

The TPS54873 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

TYPICAL APPLICATION



START-UP WAVEFORM



TPS54873

SLVS444 – OCTOBER 2002



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
–40°C to 85°C	0.9 V to 3.3 V	Plastic HTSSOP (PWP) ⁽¹⁾	TPS54873PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54873PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

		TPS54873
Input voltage range, V _I	VIN, SS/ENA, SYNC	–0.3 V to 7 V
	RT	–0.3 V to 6 V
	VSENSE	–0.3 V to 4V
	BOOT	–0.3 V to 17 V
Output voltage range, V _O	VBIAS, COMP, PWRGD	–0.3 V to 7 V
	PH	–0.6 V to 10 V
Source current, I _O	PH	Internally limited
	COMP, VBIAS	6 mA
Sink current, I _S	PH	12 A
	COMP	6 mA
	SS/ENA, PWRGD	10 mA
Voltage differential	AGND to PGND	±0.3 V
Operating virtual junction temperature range, T _J		–40°C to 125°C
Storage temperature, T _{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V _I	4		6	V
Operating junction temperature, T _J	–40		125	°C

DISSIPATION RATINGS⁽¹⁾⁽²⁾

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T _A = 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
28 Pin PWP with solder	18.2 °C/W	5.49 W ⁽³⁾	3.02 W	2.20 W
28 Pin PWP without solder	40.5 °C/W	2.48 W	1.36 W	0.99 W

(1) For more information on the PWP package, refer to TI technical brief, literature number SLMA002.

(2) Test board conditions:

1. 3" x 3", 4 layers, thickness: 0.062"
2. 1.5 oz. copper traces located on the top of the PCB
3. 1.5 oz. copper ground plane on the bottom of the PCB
4. 0.5 oz. copper ground planes on the 2 internal layers
5. 12 thermal vias (see “Recommended Land Pattern” in applications section of this data sheet)

(3) Maximum power dissipation may be limited by over current protection.

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN							
Input voltage range, VIN				4.0		6.0	V
I(Q)	Quiescent current	fS = 350 kHz, SYNC ≤ 0.8 V, RT open, PH pin open			11	15.8	mA
		fS = 550 kHz, SYNC ≥ 2.5 V, RT open, PH pin open			16	23.5	
		Shutdown, SS/ENA = 0 V			1	1.4	
UNDER VOLTAGE LOCK OUT							
Start threshold voltage, UVLO					3.8	3.85	V
Stop threshold voltage, UVLO				3.40	3.50		V
Hysteresis voltage, UVLO				0.14	0.16		V
Rising and falling edge deglitch, UVLO(1)					2.5		μs
BIAS VOLTAGE							
Output voltage, VBIAS		I(VBIAS) = 0		2.70	2.80	2.90	V
Output current, VBIAS (2)						100	μA
CUMULATIVE REFERENCE							
Vref	Accuracy			0.882	0.891	0.900	V
REGULATION							
Lineregulation(1)(3)		IL = 3 A, fS = 350 kHz, TJ = 85°C				0.04	%V
		IL = 3 A, fS = 550 kHz, TJ = 85°C				0.04	
Loadregulation(1)(3)		IL = 0 A to 6 A, fS = 350 kHz, TJ = 85°C				0.03	%A
		IL = 0 A to 6 A, fS = 550 kHz, TJ = 85°C				0.03	
OSCILLATOR							
Internally set—free running frequency		SYNC ≤ 0.8 V, RT open		280	350	420	kHz
		SYNC ≥ 2.5 V, RT open		440	550	660	
Externally set—free running frequency range		RT = 180 kΩ (1% resistor to AGND)		252	280	308	kHz
		RT = 100 kΩ (1% resistor to AGND)		460	500	540	
		RT = 68 kΩ (1% resistor to AGND)		663	700	762	
High level threshold, SYNC				2.5			V
Low level threshold, SYNC						0.8	V
Pulse duration, external synchronization, SYNC(1)				50			ns
Frequency range, SYNC(1)				330		700	kHz
Ramp valley(1)					0.75		V
Ramp amplitude (peak-to-peak)(1)					1		V
Minimum controllable on time(1)						200	ns
Maximum duty cycle				90%			

(1) Specified by design

(2) Static resistive loads only

(3) Specified by the circuit used in Figure 9

TPS54873

SLVS444 – OCTOBER 2002

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

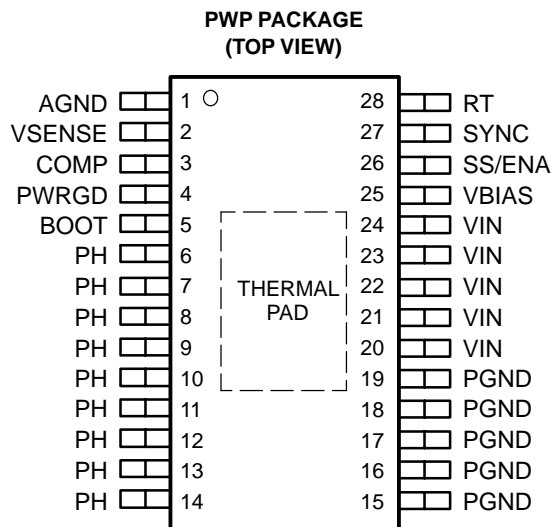
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER					
Error amplifier open loop voltage gain	1 k Ω COMP to AGND ⁽¹⁾	90	110		dB
Error amplifier unity gain bandwidth	Parallel 10 k Ω , 160 pF COMP to AGND ⁽¹⁾	3	5		MHz
Error amplifier common mode input voltage range	Powered by internal LDO ⁽¹⁾	0		V _{BIAS}	V
Input bias current, V _{SENSE}	V _{SENSE} = V _{ref}		60	250	nA
Output voltage slew rate (symmetric), COMP		1.0	1.4		V/ μ s
PWM COMPARATOR					
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive ⁽¹⁾		70	85	ns
SLOW-START/ENABLE					
Enable threshold voltage, SS/ENA		0.82	1.20	1.40	V
Enable hysteresis voltage, SS/ENA			0.03		V
Falling edge deglitch, SS/ENA ⁽¹⁾			2.5		μ s
Internal slow-start time		2.6	3.35	4.1	ms
Charge current, SS/ENA	SS/ENA = 0 V	3	5	8	μ A
Discharge current, SS/ENA	SS/ENA = 1.3 V, V _I = 1.5 V	2.0	2.3	4.0	mA
POWER GOOD					
Power good threshold voltage	V _{SENSE} falling		90		%V _{ref}
Power good hysteresis voltage ⁽¹⁾			3		%V _{ref}
Power good falling edge deglitch ⁽¹⁾			35		μ s
Output saturation voltage, PWRGD	I _(sink) = 2.5 mA		0.18	0.3	V
Leakage current, PWRGD	V _I = 5.5 V			1	μ A
CURRENT LIMIT					
Current limit trip point	V _I = 4.5 V Output shorted ⁽¹⁾	9	10		A
	V _I = 6 V Output shorted ⁽¹⁾	11	12		
Current limit leading edge blanking time			100		ns
Current limit total response time			200		ns
THERMAL SHUTDOWN					
Thermal shutdown trip point ⁽¹⁾		135	150	165	°C
Thermal shutdown hysteresis ⁽¹⁾			10		°C
OUTPUT POWER MOSFETS					
r _{DS(on)} Power MOSFET switches	V _I = 6 V ⁽⁴⁾		26	47	m Ω
	V _I = 4.5 V ⁽⁴⁾		30	60	

(1) Specified by design

(2) Static resistive loads only

(3) Specified by the circuit used in Figure 9

(4) Matched MOSFETs low-side r_{DS(on)} production tested, high-side r_{DS(on)} specified by design



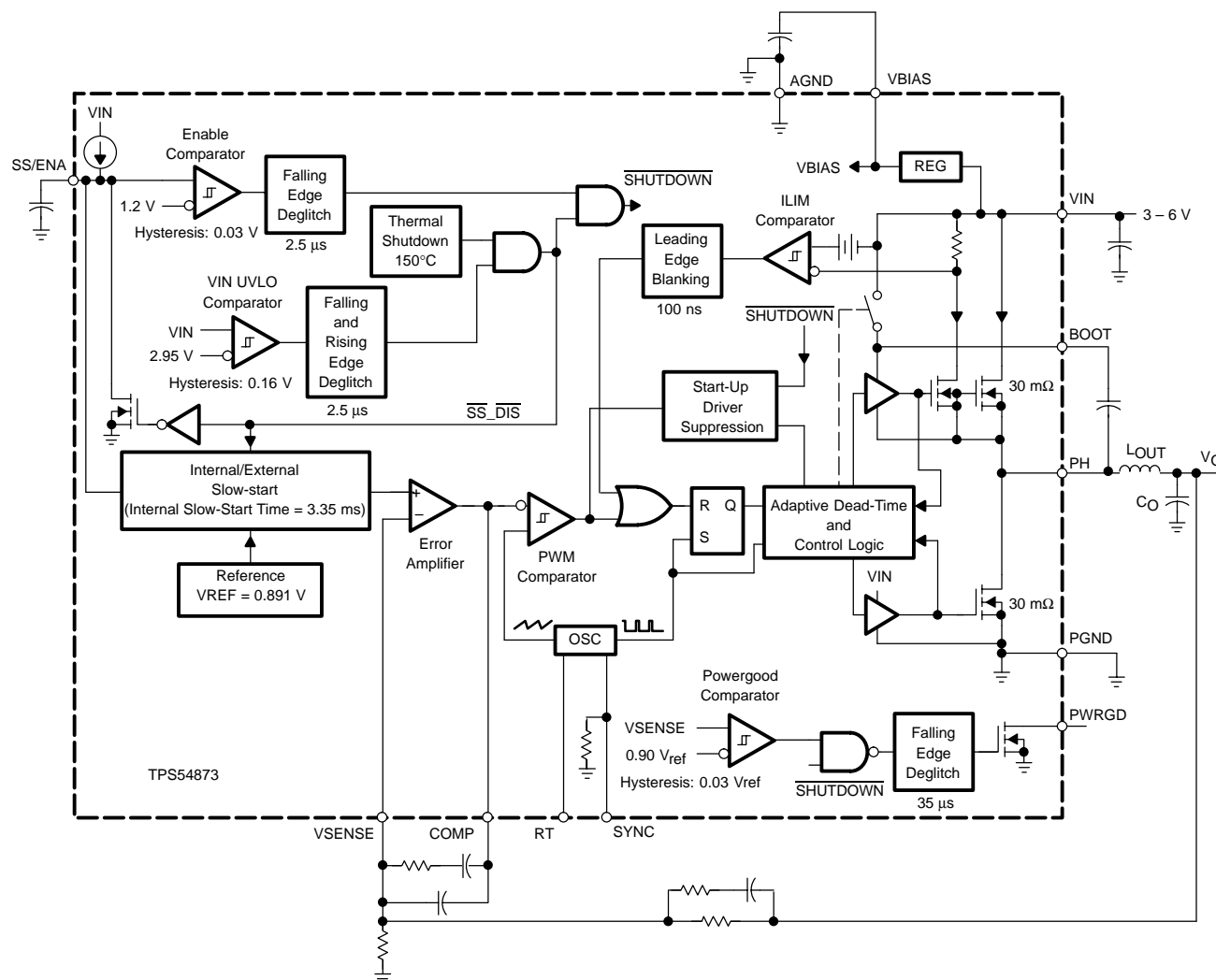
TERMINAL FUNCTIONS

TERMINAL NAME	NO.	DESCRIPTION
AGND	1	Analogground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor and SYNC pin. Connect PowerPAD to AGND.
BOOT	5	Bootstrap output. 0.022-μF to 0.1-μF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
PGND	15–19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6–14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PWRGD	4	Power good open drain output. High when VSENSE ≥ 90% V _{ref} , otherwise PWRGD is low. Note that output is low when SS/ENA is low, or the internal shutdown signal is active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency. When using the SYNC pin, set the RT value for a frequency at or slightly lower than the external oscillator frequency.
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	27	Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1-μF to 1.0-μF ceramic capacitor.
VIN	20–24	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low-ESR 10-μF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage through compensation network/output divider.

TPS54873

SLVS444 – OCTOBER 2002

INTERNAL BLOCK DIAGRAM



ADDITIONAL 6A SWIFT™ DEVICES, (REFER TO SLVS397 AND SLVS400)

DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE
TPS54611	0.9 V	TPS54614	1.8 V	TPS54672	Active termination
TPS54612	1.2 V	TPS54615	2.5 V	TPS54610	Adjustable
TPS54613	1.5 V	TPS54616	3.3 V	TPS54680	Sequencing

RELATED DC/DC PRODUCTS

- TPS54673 – DC/DC Converter (integrated switch)
- TPS40000 – DC/DC Controller
- TPS40002 – DC/DC Controller

TYPICAL CHARACTERISTICS

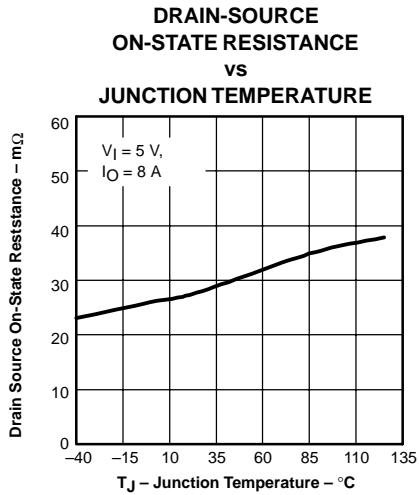


Figure 1

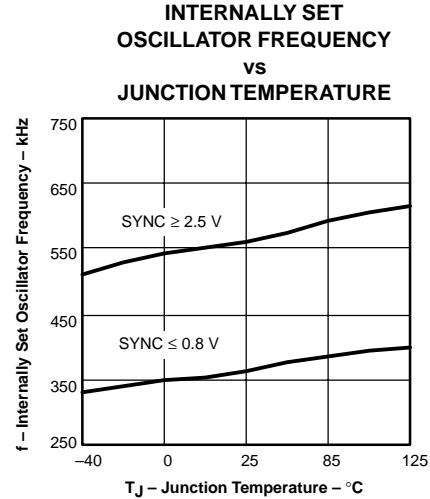


Figure 2

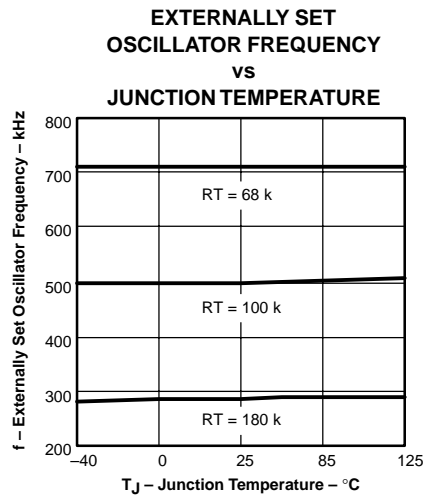


Figure 3

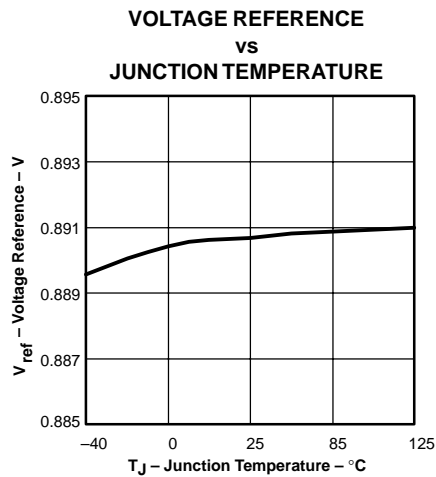


Figure 4

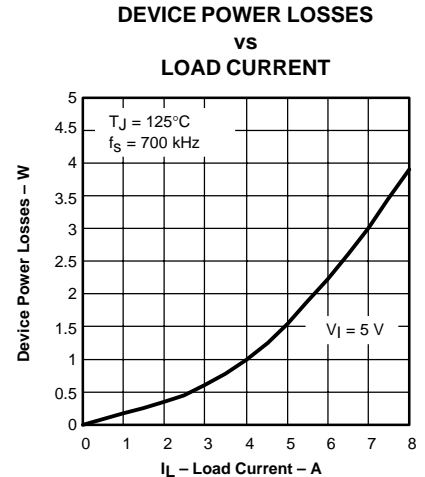


Figure 5

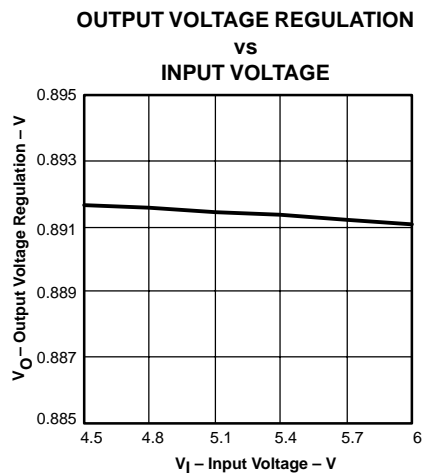


Figure 6

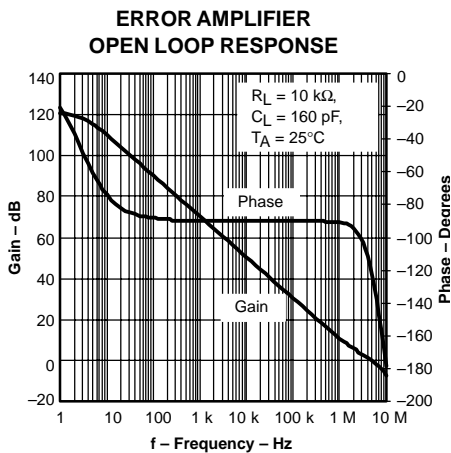


Figure 7

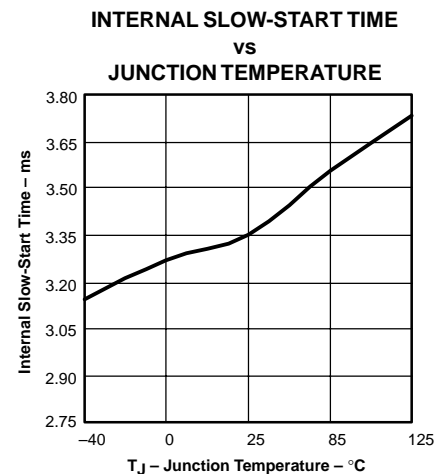


Figure 8

TPS54873

SLVS444 – OCTOBER 2002

APPLICATION INFORMATION

Figure 9 shows the schematic diagram for a typical TPS54873 application. The TPS54873 (U1) can provide up to 8 A of output current at a nominal output voltage of 0.9 V to 3.3 V, and for this application, the output voltage

is set at 3.3 V. For proper operation, the PowerPAD underneath the integrated circuit TPS54873 must be soldered properly to the printed-circuit board.

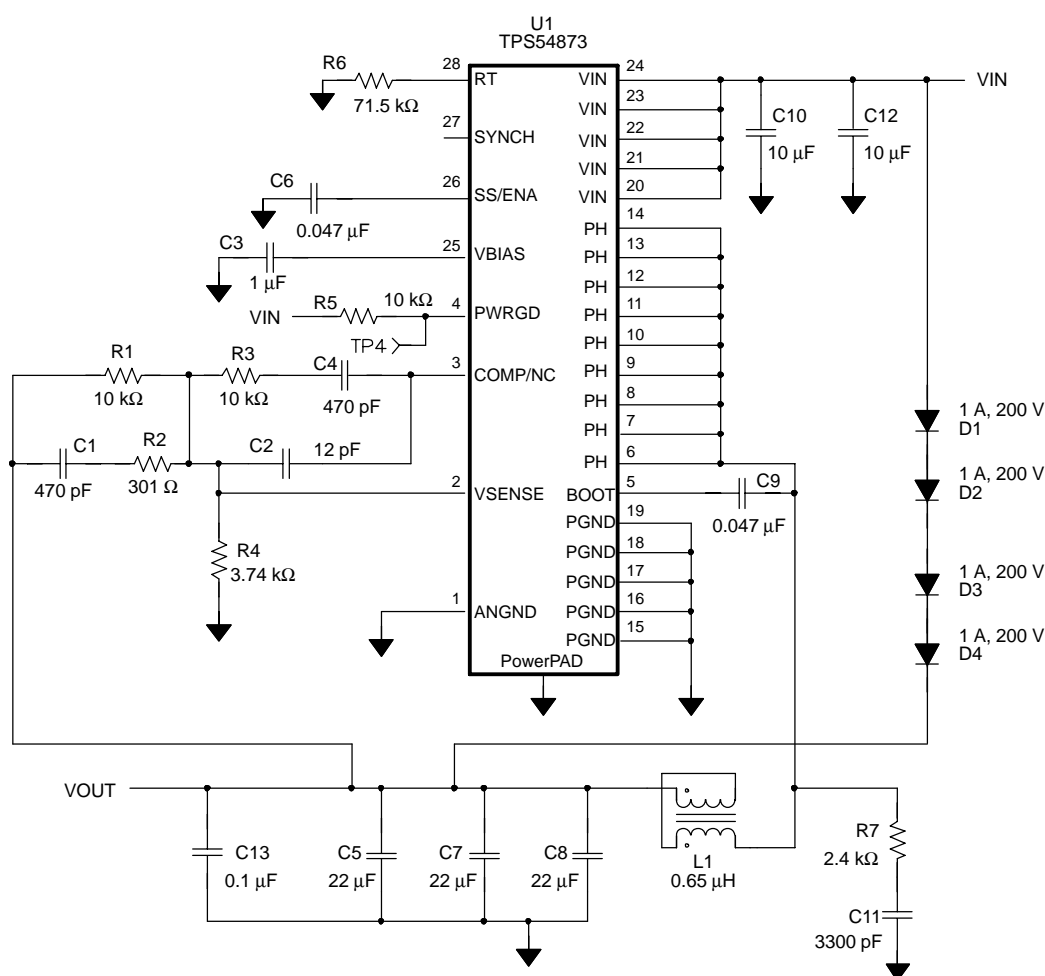


Figure 9. Application Circuit

COMPONENT SELECTION

The values for the components used in this design example are selected for low output ripple and small PCB area. Ceramic capacitors are utilized in the output filter circuit. A small size, small value output inductor is also used. Compensation network components are chosen to maximize closed loop bandwidth and provide good transient response characteristics. Additional design information is available at www.ti.com.

INPUT VOLTAGE

The input voltage is a nominal 5. VDC. The input filter (C12) is a 10-µF ceramic capacitor (Taiyo Yuden). C10, also a 10-µF ceramic capacitor (Taiyo Yuden) that provides high frequency decoupling of the TPS54873 from

the input supply, must be located as close as possible to the device. Ripple current is carried in both C10 and C12, and the return path to PGND should avoid the current circulating in the output capacitors C5, C7, C8, and C13.

FEEDBACK CIRCUIT

The values for these components are selected to provide fast transient response times. R1, R2, R3, R4, C1, C2, and C4 forms the loop-compensation network for the circuit. For this design, a Type 3 topology is used. The transfer function of the feedback network is chosen to provide maximum closed loop gain available with open loop characteristics of the internal error amplifier. Closed loop crossover frequency is typically between 80 kHz and 135 kHz for input from 3 V to 6 V.

OPERATING FREQUENCY

In the application circuit, the RT pin is grounded through a 71.5-k Ω resistor (R6) to select the operating frequency of 700 kHz. To set a different frequency, place a 68-k Ω to 180-k Ω resistor between RT (pin 28) and analog ground or leave RT floating to select the default of 350 kHz. The resistance can be approximated using the following equation:

$$R = \frac{500 \text{ kHz}}{\text{Switching Frequency}} \times 100 \text{ [k}\Omega\text{]} \quad (1)$$

OUTPUT FILTER

The output filter is composed of a 0.65- μ H inductor (L1) and 3 x 22- μ F capacitors (C5, C7 and C8). The inductor is a low dc resistance (.017 Ω) type, Pulse PA0277 0.65 μ H. The capacitors used are 22- μ F, 6.3-V ceramic types with X5R dielectric. An additional high frequency bypass capacitor, C13 is also used.

PRECHARGE CIRCUIT

VIN precharges the output of the application circuit through series diodes (D1 and D2) during start-up. As the input voltage increases at start-up, the output is precharged to VIN minus the forward bias voltage of the two diodes. When the internal reference has ramped up to a value greater than the voltage fed back to the VSENSE pin, the output of the internal error amplifier begins to increase. When this output reaches the maximum ramp amplitude, the output of the PWM comparator reaches 100 percent duty cycle and the internal logic enables the high-side FET driver and switching begins. The output tracks the internal reference until the preset output voltage is reached. Under no circumstances should the precharge voltage be allowed to increase above the preset output value.

GROUNDING AND POWERPAD LAYOUT

The TPS54873 has two internal grounds (analog and power). Inside the TPS54873, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD must be tied

directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54873, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground areas are recommended. The analog ground area should be tied to the power ground area directly at the IC to reduce noise between the two grounds. The only components that should tie directly to the power ground area are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54873. The power ground areas as well as the PowerPAD mounting area should be tied to any internal ground planes using multiple vias. The layout of the TPS54873 evaluation module is representative of a recommended layout for a 4-layer board with the two internal layers representing the system ground plane. Documentation for the TPS54873 evaluation module can be found on the Texas Instruments web site under the TPS54873 product folder.

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 6 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Eight vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the ten recommended that enhance thermal performance should be included in areas not under the device package.

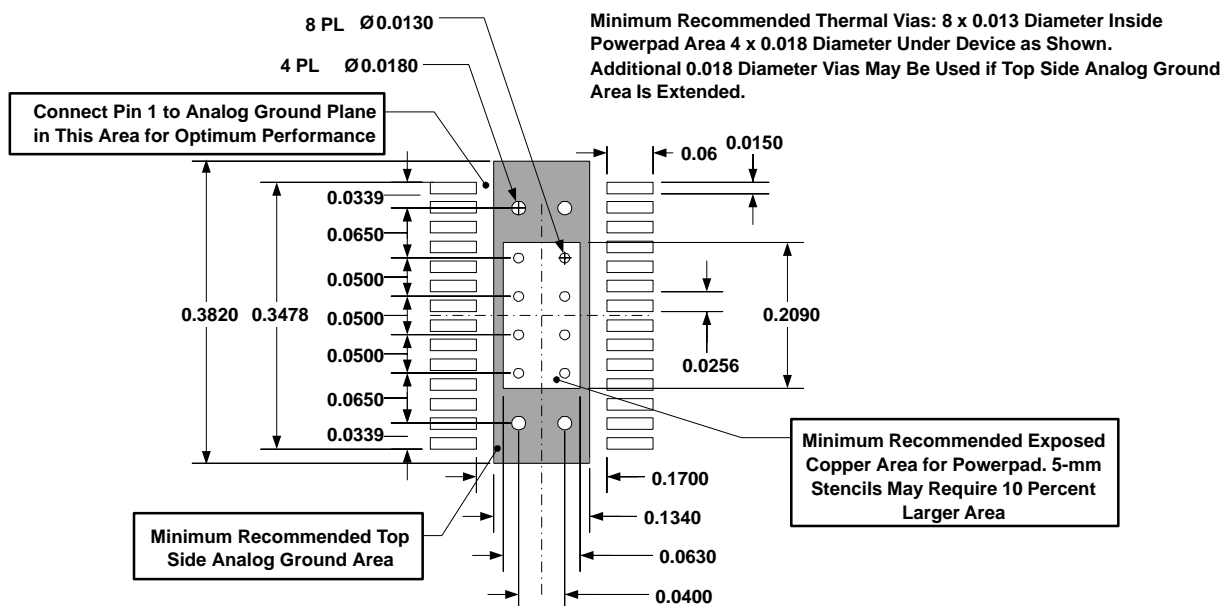


Figure 10. Recommended Land Pattern for 28-Pin PWP PowerPAD

PERFORMANCE GRAPHS

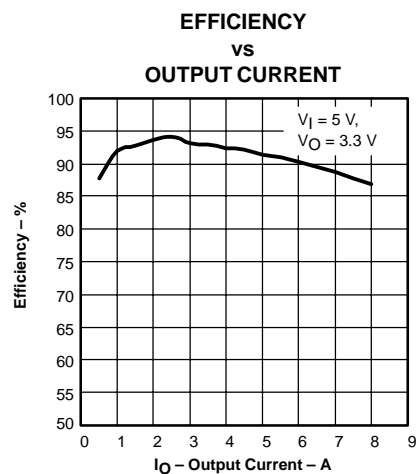


Figure 11

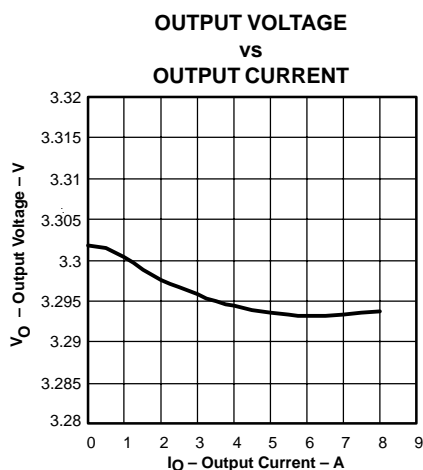


Figure 12

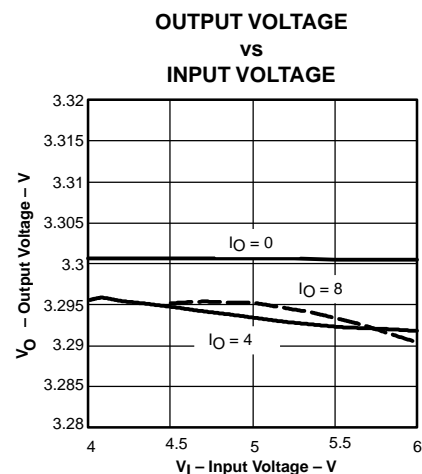


Figure 13

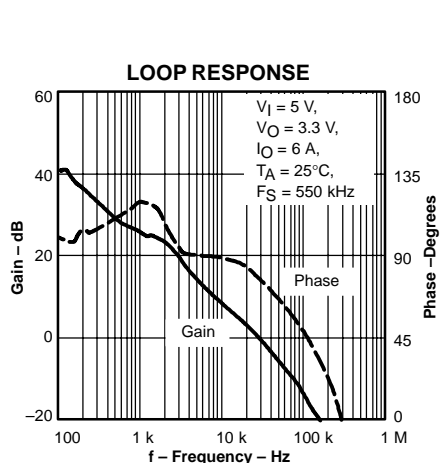


Figure 14

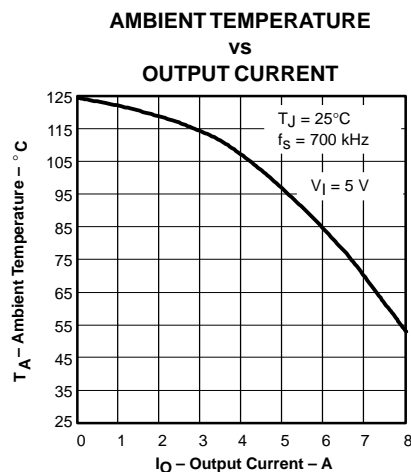


Figure 15

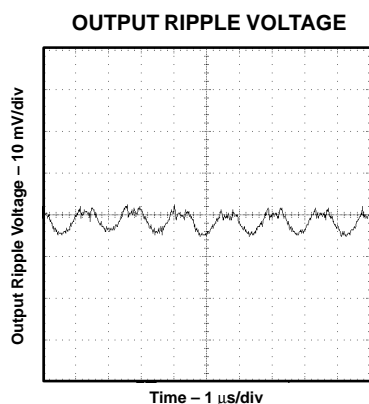


Figure 16

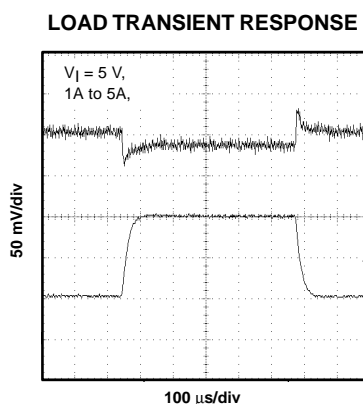


Figure 17

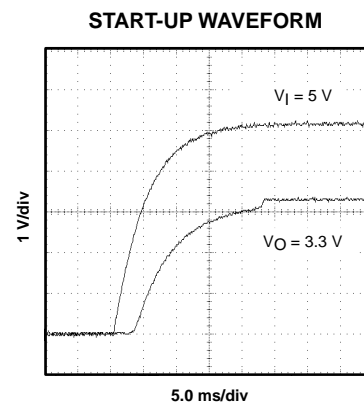


Figure 18

DETAILED DESCRIPTION

DISABLED SINKING DURING START-UP (DSDS)

The DSDS feature enables minimal voltage drooping of output precharge capacitors at start-up. The TPS54873 is designed to disable the low-side MOSFET to prevent sinking current from a precharge output capacitor during start-up. Once the high-side MOSFET has been turned on to the maximum duty cycle limit, the low-side MOSFET is allowed to switch. Once the maximum duty cycle condition is met, the converter functions as a sourcing converter until the SS/ENA is pulled low.

UNDERVOLTAGE LOCK OUT (UVLO)

The TPS54873 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 3.8 V. Once the UVLO start threshold

is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 3.5 V. Hysteresis in the UVLO comparator and a 2.5-μs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

SLOW-START/ENABLE (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-μs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

TPS54873

SLVS444 – OCTOBER 2002

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2 \text{ V}}{5 \text{ } \mu\text{A}} \quad (2)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7 \text{ V}}{5 \text{ } \mu\text{A}} \quad (3)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate. The low side MOSFET is off during the slow-start sequence.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

VOLTAGE REFERENCE

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54873, since it cancels offset errors in the scale and error amplifier circuits.

OSCILLATOR AND PWM RAMP

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the SYNC pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be

externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin and AGND and floating the SYNC pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100 \text{ k}\Omega}{R} \times 500 \text{ [kHz]} \quad (4)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 700 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose a resistor between the RT and AGND which sets the free running frequency to 80% of the synchronization signal. The following table summarizes the frequency selection configurations:

SWITCHING FREQUENCY	SYNC PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	$\geq 2.5 \text{ V}$	Float
Externally set 280 kHz to 700 kHz	Float	$R = 180 \text{ k}\Omega$ to $68 \text{ k}\Omega$
Externally synchronized frequency	Synchronization signal	$R = \text{RT value for } 80\% \text{ of external synchro-nization frequency}$

ERROR AMPLIFIER

The high performance, wide bandwidth, voltage error amplifier sets the TPS54873 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is reset, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the

high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54873 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5- Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold.

The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

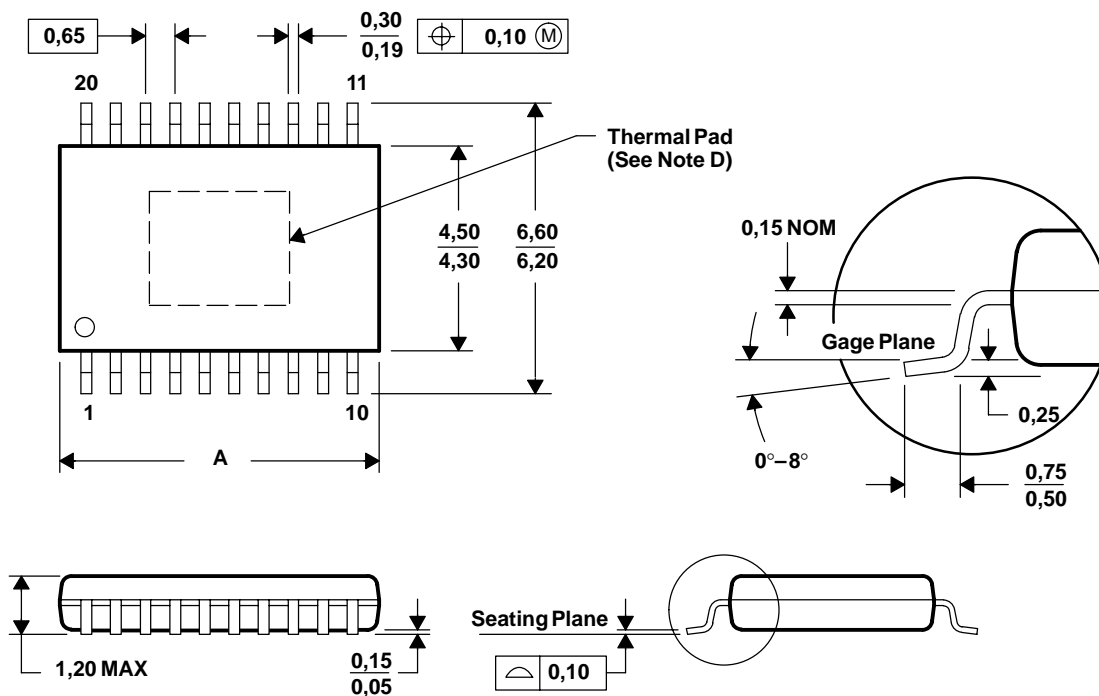
THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

POWER-GOOD (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low, or a thermal shutdown occurs. When $VIN \geq UVLO$ threshold, $SS/ENA \geq$ enable threshold, and $VSENSE > 90\%$ of V_{ref} , the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35 μ s falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

MECHANICAL DATA**PWP (R-PDSO-G**)****POWERPAD™ PLASTIC SMALL-OUTLINE****20 PINS SHOWN**

PINS **	14	16	20	24	28
DIM					
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F10/98

NOTES:A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusions.

D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.

E. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265