

9-A OUTPUT, 3-V TO 4-V INPUT TRACKING/TERMINATION SYNCHRONOUS PWM SWITCHER WITH INTEGRATED FETS (SWIFT™)

FEATURES

- Tracks Externally Applied Reference Voltage
- 15-mΩ MOSFET Switches for High Efficiency at 9-A Continuous Output Source or Sink Current
- 6% to 90% V_I Output Tracking Range
- Wide PWM Frequency: Fixed 350 kHz or Adjustable 280 kHz to 700 kHz
- Load Protected by Peak Current Limit and Thermal Shutdown
- Integrated Solution Reduces Board Area and Total Cost

APPLICATIONS

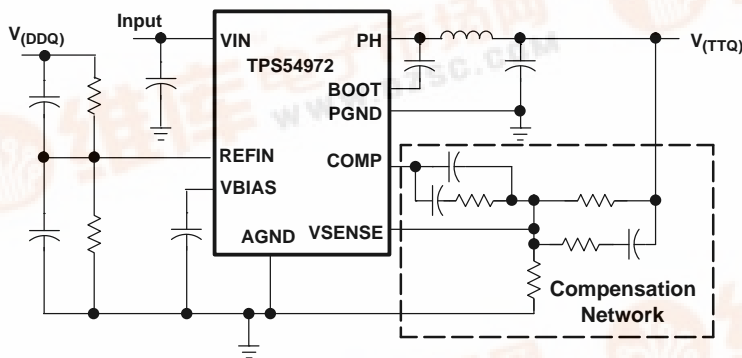
- DDR Memory Termination Voltage
- Active Termination of GTL and SSTL High-Speed Logic Families
- DAC Controlled High Current Output Stage
- Precision Point of Load Power Supply

DESCRIPTION

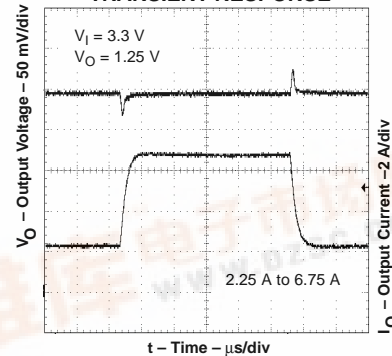
As a member of the SWIFT™ family of dc/dc regulators, the TPS54972 low-input voltage high-output current synchronous-buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 3.0 V; an internally set slow-start circuit to limit in-rush currents; and a status output to indicate valid operating conditions.

The TPS54972 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

SIMPLIFIED SCHEMATIC



TRANSIENT RESPONSE



TPS54972

SLVS437A — AUGUST 2002 – REVISED DECEMBER 2002



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	REFIN VOLTAGE	PACKAGE	PART NUMBER
-40°C to 85°C	0.2 V to 1.75 V	Plastic HTSSOP (PWP)(1)	TPS54972PWP

- (1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54972PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (2)

		TPS54972
Input voltage range, V_I	ENA	-0.3 V to 7 V
	VIN	-0.3 V to 4.5 V
	RT	-0.3 V to 6 V
	VSENSE, REFIN	-0.3 V to 4 V
	BOOT	-0.3 V to 17 V
Output voltage range, V_O	VBIAS, COMP, STATUS	-0.3 V to 7 V
	PH	-0.6 V to 6 V
Source current, I_O	PH	Internally Limited
	COMP, VBIAS	6 mA
Sink current, I_S	PH	16 A
	COMP	6 mA
	ENA, STATUS	10 mA
Voltage differential	AGND to PGND	± 0.3 V
Operating virtual junction temperature range, T_J		-40 to 125 °C
Storage temperature, T_{stg}		-65 to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300 °C

- (2) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I	3	4		V
Operating junction temperature, T_J	-40	125		°C

DISSIPATION RATINGS (3) (4)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T _A =25°C POWER RATING	T _A =70°C POWER RATING	T _A =85°C POWER RATING
28 Pin PWP with solder	14.4°C/W	6.94 W (5)	3.81 W	2.77 W
28 Pin PWP without solder	27.9°C/W	3.58 W	1.97 W	1.43 W

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 125°C, V_I = 3 V to 4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
VIN	Input voltage range		3.0		4.0	V
I _(Q)	Quiescent current	f _s =350 kHz, RT open, PH pin open		11	15.8	mA
		f _s =500 kHz, RT=100 kΩ, PH pin open		16	23.5	
		Shutdown, SS/ENA=0 V		1	1.4	
UNDER VOLTAGE LOCK OUT						
	Start threshold voltage, UVLO			2.95	3.0	V
	Stop threshold voltage, UVLO		2.7	2.8		V
	Hysteresis voltage, UVLO		0.14	0.16		V
	Rising and falling edge deglitch, UVLO (6)			2.5		μs
BIAS VOLTAGE						
	Output voltage, VBIAS	I _(VBIAS) =0	2.70	2.80	2.90	V
	Output current, VBIAS (7)				100	μA
REGULATION						
	Line regulation (6) (8)	I _L =4 A, f _s =350 kHz, T _J =85°C			0.04	%/V
	Load regulation (6) (8)	I _L =0 A to 8 A, f _s =350 kHz, T _J =85°C			0.03	%/A
OSCILLATOR						
	Internally set free running frequency	RT open	280	350	420	kHz
	Externally set free running frequency range	RT=180 kΩ (1% resistor to AGND)	252	280	308	
		RT=100 kΩ (1% resistor to AGND)	460	500	540	
		RT=68 kΩ (1% resistor to AGND)	663	700	762	
	Ramp valley (6)			0.75		V
	Ramp amplitude (peak-to-peak) (6)			1		V
	Minimum controllable on time (6)				200	ns
	Maximum duty cycle (6)		90%			
ERROR AMPLIFIER						
	Error amplifier open loop voltage gain	1 kΩ COMP to AGND (6)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND (6)	3	5		MHz
	Error amplifier common mode input voltage range	Powered by internal LDO (6)	0	VBIAS		V
	Input bias current, VSENSE	VSENSE=V _{ref}		60	250	nA

(3) For more information on the PWP package, refer to TI technical brief, literature number SLMA002.

(4) Test board conditions:

- 3" x 3", 4 layers, thickness: 0.062"
- 1.5 oz. copper traces located on the top of the PCB
- 1.5 oz. copper ground plane on the bottom of the PCB
- 12 thermal vias (see Recommended Land Pattern in applications section of this data sheet)

(5) Maximum power dissipation may be limited by overcurrent protection.

(6) Specified by design

(7) Static resistive loads only

(8) Specified by the circuit used in Figure 8

TPS54972

SLVS437A — AUGUST 2002 – REVISED DECEMBER 2002

ELECTRICAL CHARACTERISTICS (continued)

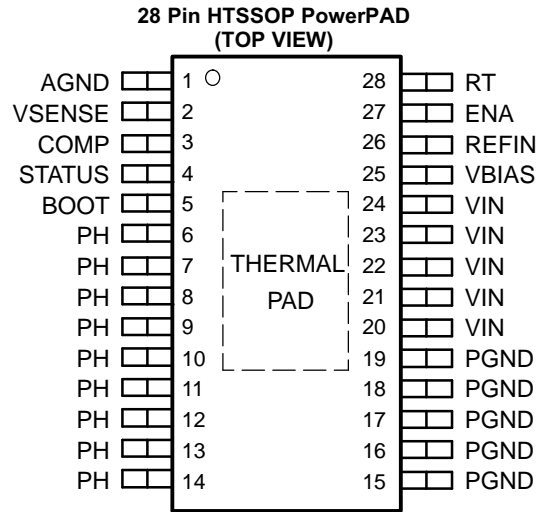
 $T_J = -40^{\circ}\text{C}$ to 125°C , $V_I = 3\text{ V}$ to 4 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage slew rate (symmetric), COMP		1.0	1.4		V/ μs
PWM COMPARATOR					
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive (6)		70	85	ns
SLOW-START/ENABLE					
Enable threshold voltage, ENA		0.82	1.20	1.40	V
Enable hysteresis voltage, ENA (6)			0.03		V
Falling edge deglitch, ENA (6)			2.5		μs
Internal slow-start time		2.6	3.35	4.1	ms
STATUS					
Output saturation voltage, PWRGD	$I_{\text{sink}}=2.5\text{ mA}$		0.18	0.30	V
Leakage current, PWRGD	$V_I=3.6\text{ V}$			1	μA
CURRENT LIMIT					
Current limit	$V_I=3.3\text{ V}$	11	15		A
Current limit leading edge blanking time			100		ns
Current limit total response time			200		ns
THERMAL SHUTDOWN					
Thermal shutdown trip point (9)		135	150	165	$^{\circ}\text{C}$
Thermal shutdown hysteresis (9)			10		$^{\circ}\text{C}$
OUTPUT POWER MOSFETS					
$r_{\text{DS(on)}}$ Power MOSFET switches	$V_I=3.0\text{ V}$ (10)		15	30	m Ω
	$V_I=3.6\text{ V}$ (10)		14	28	

(9) Specified by design

 (10) Matched MOSFETs low-side $r_{\text{DS(on)}}$ production tested, high-side $r_{\text{DS(on)}}$ production tested.

TPS54972 Externally Composed Pin-Out



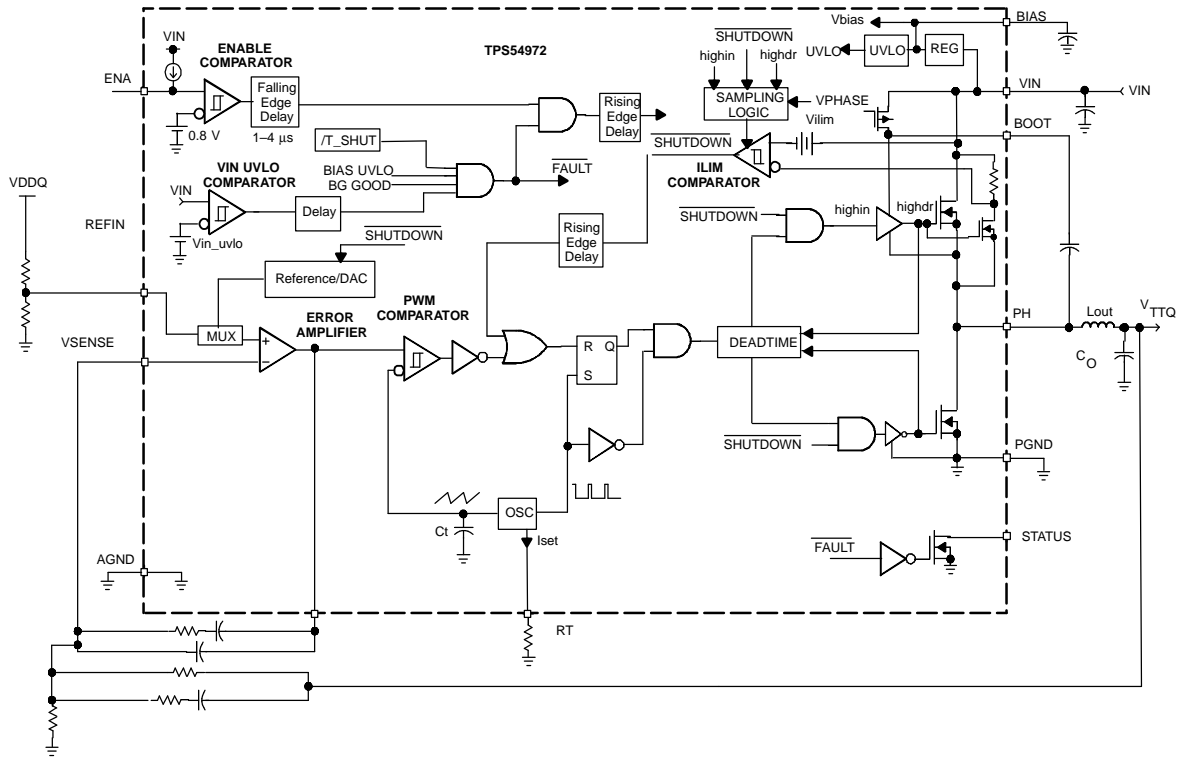
TERMINAL FUNCTIONS

TERMINAL NAME	NO.	DESCRIPTION
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor, and SYNC pin. Connect PowerPAD connection to AGND.
BOOT	5	Bootstrap output. 0.022- μ F to 0.1- μ F low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
ENA	27	Enable input. Logic high enables oscillator, PWM control, and MOSFET driver circuits. Logic low disables operation and places device in a low quiescent current state.
PGND	15-19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6-14	Phase input/output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s .
REFIN	26	External reference input. High impedance input to slow-start and error amplifier circuits.
STATUS	4	Open drain output. Asserted low when $V_{IN} < UVLO$, VBIAS and internal reference are not settled or the internal shutdown signal is active. Otherwise STATUS is high.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1- μ F to 1.0- μ F ceramic capacitor.
VIN	20-24	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high-quality, low-ESR 10- μ F ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

TPS54972

SLVS437A — AUGUST 2002 – REVISED DECEMBER 2002

INTERNAL BLOCK DIAGRAM



RELATED DC/DC PRODUCTS

- TPS54372
- TPS54672
- TPS54872

TYPICAL CHARACTERISTICS

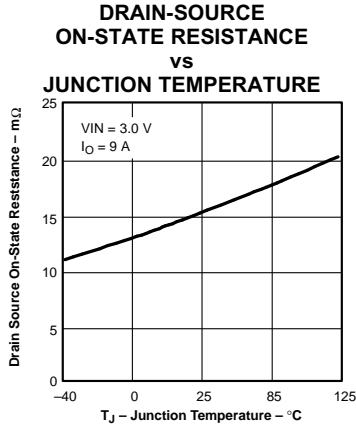


Figure 1

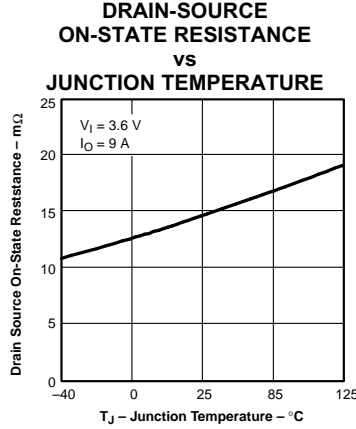


Figure 2

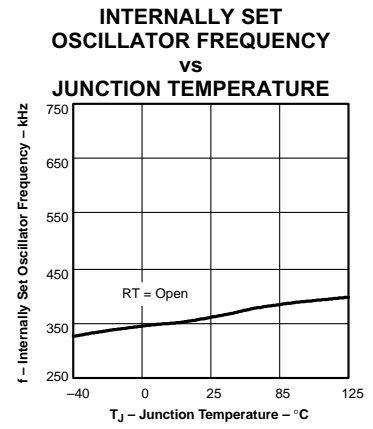


Figure 3

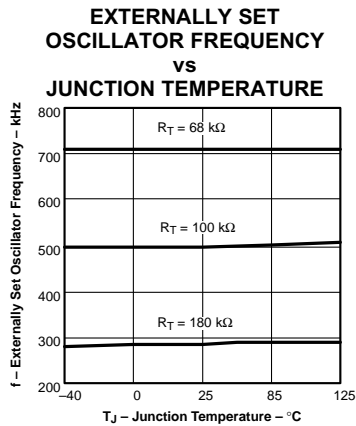


Figure 4

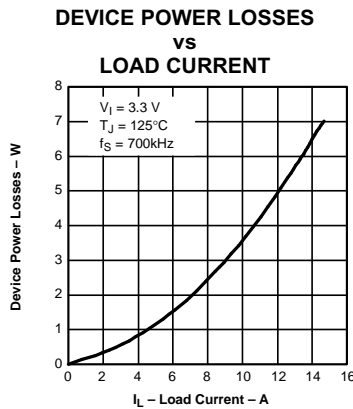


Figure 5

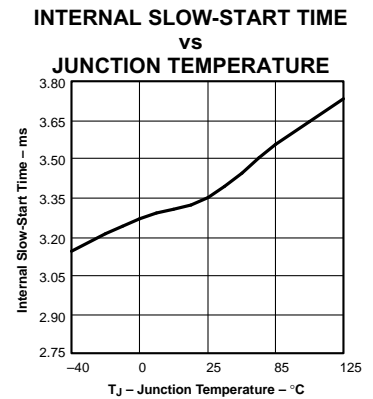


Figure 6

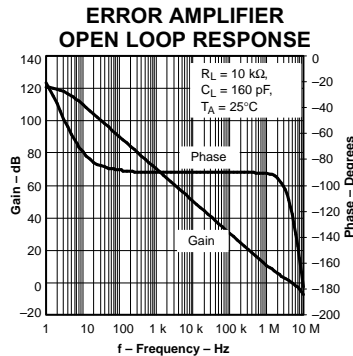


Figure 7

TPS54972

SLVS437A — AUGUST 2002 – REVISED DECEMBER 2002

APPLICATION INFORMATION

Figure 8 shows the schematic diagram for a typical TPS54972 application. The TPS54972 (U1) can provide up to 9 A of output current at a nominal output voltage of one half of $V_{(DDQ)}$ (typically 1.25 V). For proper operation, the PowerPAD underneath the integrated circuit TPS54972 is soldered directly to the printed-circuit board.

COMPONENT SELECTION

The values for the components used in this design example were selected for good transient response and small PCB area. Ceramic dielectric capacitors are utilized in the output filter circuit. A small size, small value output inductor is also used. Compensation network components are chosen to maximize closed loop bandwidth and provide good transient response characteristics. Additional design information is available at www.ti.com.

INPUT VOLTAGE

The input voltage is a nominal 3.3 VDC. The input filter (C4) is a 10- μ F ceramic capacitor (Taiyo Yuden). Capacitor C8, a 10- μ F ceramic capacitor (Taiyo Yuden) that provides high frequency decoupling of the TPS54972 from the input supply, must be located as close as possible to the device. Ripple current is carried in both C4 and C8, and the return path to PGND should avoid the current circulating in the output capacitors C7, C9, C11, and C12.

FEEDBACK CIRCUIT

The values for these components are selected to provide fast transient response times. Components R1, R2, R3, C1, C2, and C3 form the loop compensation network for the circuit. For this design, a type 3 topology is used. The transfer function of the feedback network is chosen to provide maximum closed loop gain available with open loop characteristics of the internal error amplifier. Closed loop cross-over frequency is typically between 70 kHz and 80 kHz for input from 3 V to 4 V.

OPERATING FREQUENCY

In the application circuit, RT is grounded through a 71.5 k Ω resistor to select the operating frequency of 700 kHz. To set a different frequency, place a 68-k Ω to 180-k Ω resistor between RT (pin 28) and analog ground or leave RT floating to select the default of 350 kHz. The resistance can be approximated using the following equation:

$$R = \frac{500 \text{ kHz}}{\text{Switching Frequency}} \times 100 [\text{k}\Omega] \quad (1)$$

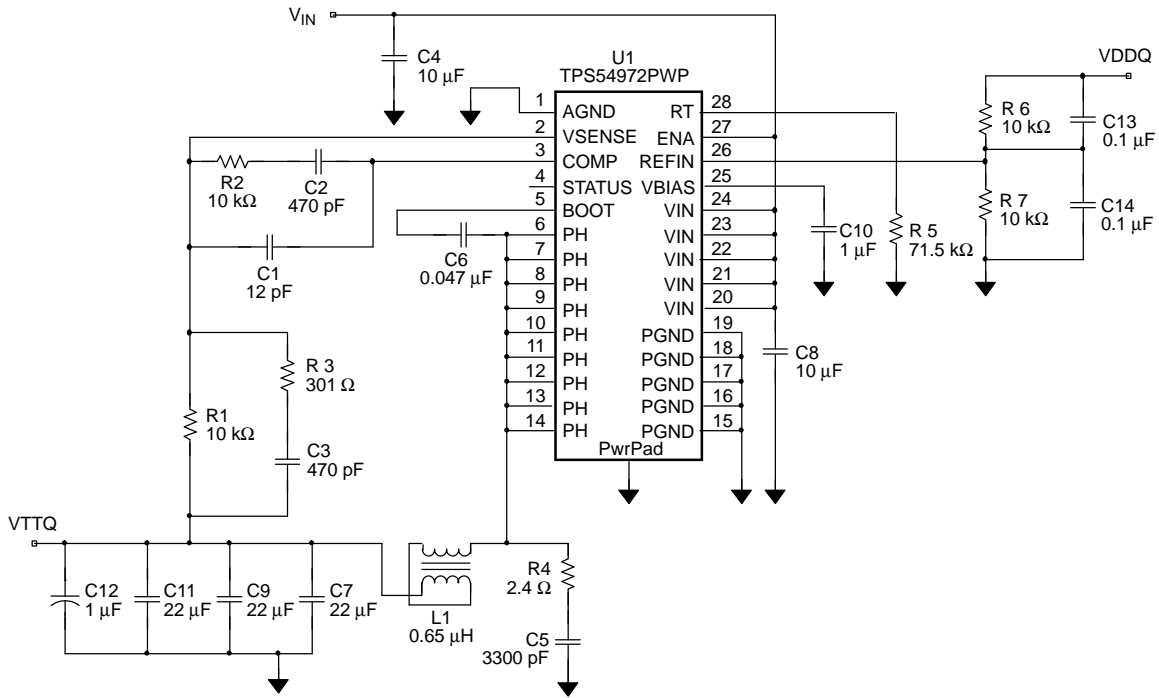


Figure 8. Application Circuit

OUTPUT FILTER

The output filter is composed of a 0.65- μ H inductor and three 22- μ F capacitors. The inductor is a low dc resistance (0.017 Ω) type, Pulse PA0277 0.65- μ H. The capacitors used are 22 μ F, 6.3-V ceramic types with X5R dielectric. An additional 1- μ F output capacitor (C12) is included to suppress high frequencies.

GROUNDING AND POWERPAD LAYOUT

The TPS54972 has two internal grounds (analog and power). Inside the TPS54972, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD must be tied directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54972, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground areas are recommended. The analog ground area should be tied to the power ground area directly at the IC to reduce noise between the two grounds. The only components that should tie directly to the power ground area are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54972. The power ground areas as well as the PowerPAD mounting area should be tied to any internal ground planes using multiple vias. The layout of the TPS54972 evaluation module is representative of a recommended layout for a 4-layer board with the two internal layers representing the system ground plane. Documentation for the TPS54972 evaluation module can be found on the Texas Instruments web site under the TPS54972 product folder.

TPS54972

SLVS437A — AUGUST 2002 — REVISED DECEMBER 2002

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 9 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Eight vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the ten recommended that enhance thermal performance should be included in areas not under the device package.

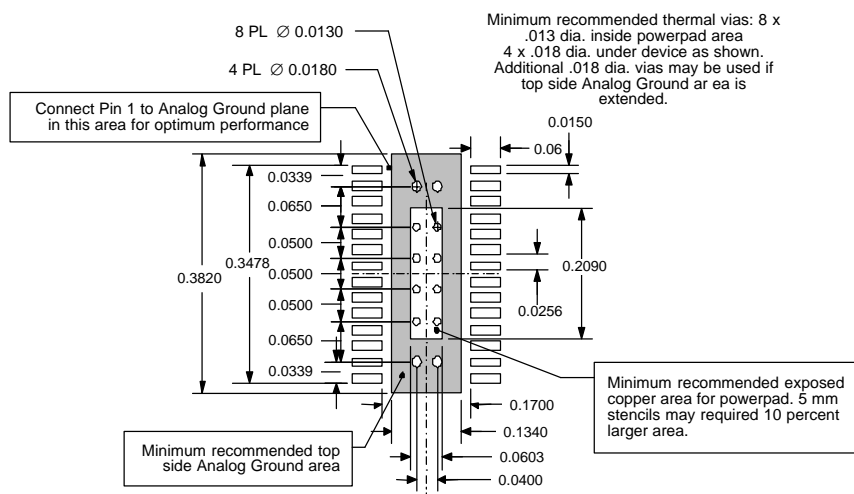


Figure 9. Recommended Land Pattern for 28-Pin PWP PowerPAD

PERFORMANCE GRAPHS

T_A = 25°C (unless otherwise noted)

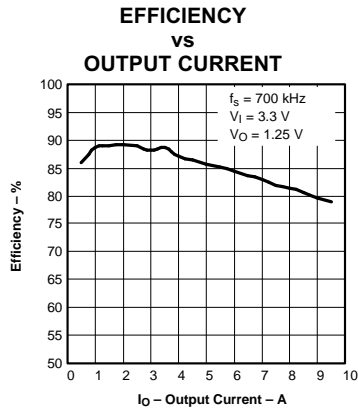


Figure 10

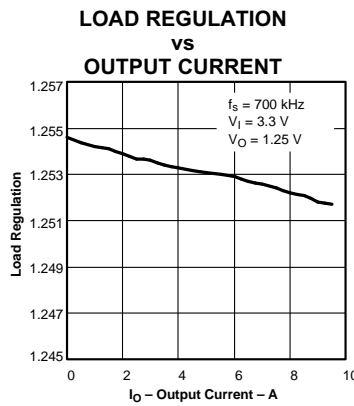


Figure 11

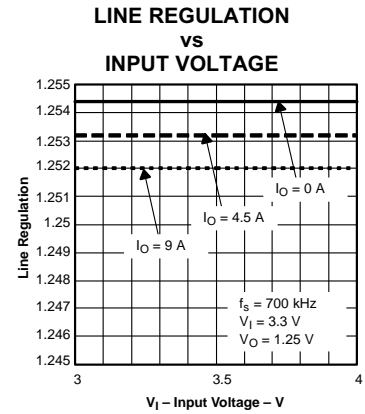


Figure 12

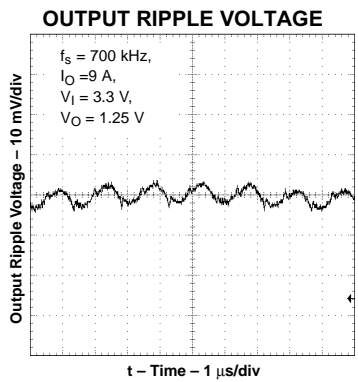


Figure 13

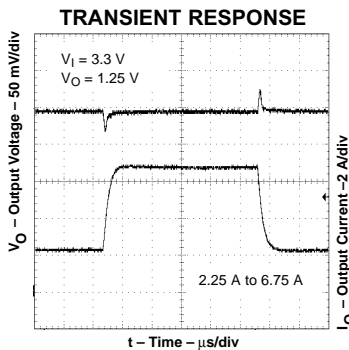


Figure 14

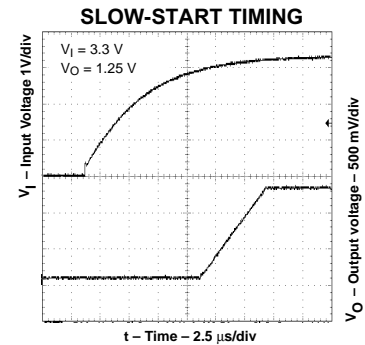


Figure 15

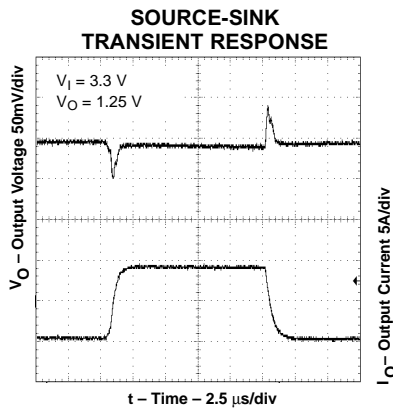
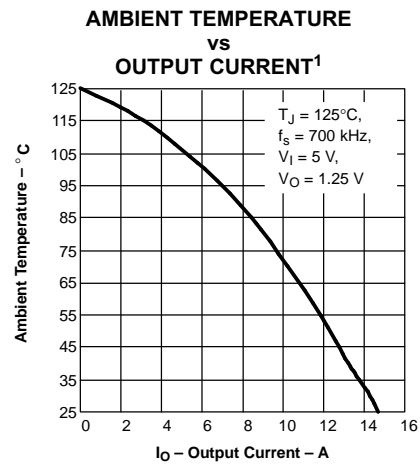


Figure 16



1. Safe operating area is applicable to the test board conditions listed in the dissipation rating table section of this data sheet.

Figure 17

TPS54972

SLVS437A — AUGUST 2002 – REVISED DECEMBER 2002

DETAILED DESCRIPTION

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS54972 incorporates an undervoltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.80 V. Hysteresis in the UVLO comparator, and a 2.5- μ s rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

ENABLE (ENA)

The enable pin, ENA, provides a digital control to enable or disable (shut down) the TPS54972. An input voltage of 1.4V or greater ensures the TPS54972 is enabled. An input of 0.9 V or less ensures the device operation is disabled. These are not standard logic thresholds, even though they are compatible with TTL outputs.

When ENA is low, the oscillator, slow-start, PWM control and MOSFET drivers are disabled and held in an initial state ready for device start-up. On an ENA transition from low to high, device start-up begins with the output starting from 0V.

SLOW-START

The slow-start circuit provides start-up slope control control of the output voltage to limit in-rush currents. The nominal internal slow-start rate is 0.25 V/ms with the minimum rate being 0.35 V/ms. When the voltage on REFIN rises faster than the internal slope or is present when device operation is enabled, the output rises at the internal rate. If the reference voltage on REFIN rises more slowly, then the output rises at approximately the same rate as REFIN.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND. External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

VOLTAGE REFERENCE

The REFIN pin provides an input for a user supplied tracking voltage. Typically this input is one half of $V_{(DDQ)}$. The input range for this external reference is 0.2 V to 1.75 V. Above this level, the internal bandgap reference overrides the externally supplied reference voltage.

OSCILLATOR AND PWM RAMP

The oscillator frequency can be set to an internally fixed value of 350 kHz by leaving the RT pin unconnected (floating). If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor to the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100 \text{ k}\Omega}{R} \times 500 \text{ [kHz]}$$

The following table summarizes the frequency selection configurations:

SWITCHING FREQUENCY	RT PIN
350 kHz, internally set	Float
Externally set 280 kHz to 700 kHz	R=68 k Ω to 180 k Ω

ERROR AMPLIFIER

The high performance, wide bandwidth, voltage error amplifier sets the TPS54972 apart from most dc/dc converters. The user has a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset, and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54972 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off, and the low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the gate drive voltage to the low-side FET is below 2 V, while the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V. The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle by cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100 ns leading edge blanking circuit prevents false tripping of the current limit when the high-side switch is turning on. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal limit trip point. This sequence repeats until the fault condition is removed.

TPS54972

SLVS437A — AUGUST 2002 – REVISED DECEMBER 2002

STATUS

The status pin is an open drain output that indicates when internal conditions are sufficient for proper operation. STATUS can be coupled back to a system controller or monitor circuit to indicate that the termination or tracking regulator is ready for start-up. STATUS is high impedance when the TPS54972 is operating or ready to be enabled.

STATUS is active low if any of the following occur:

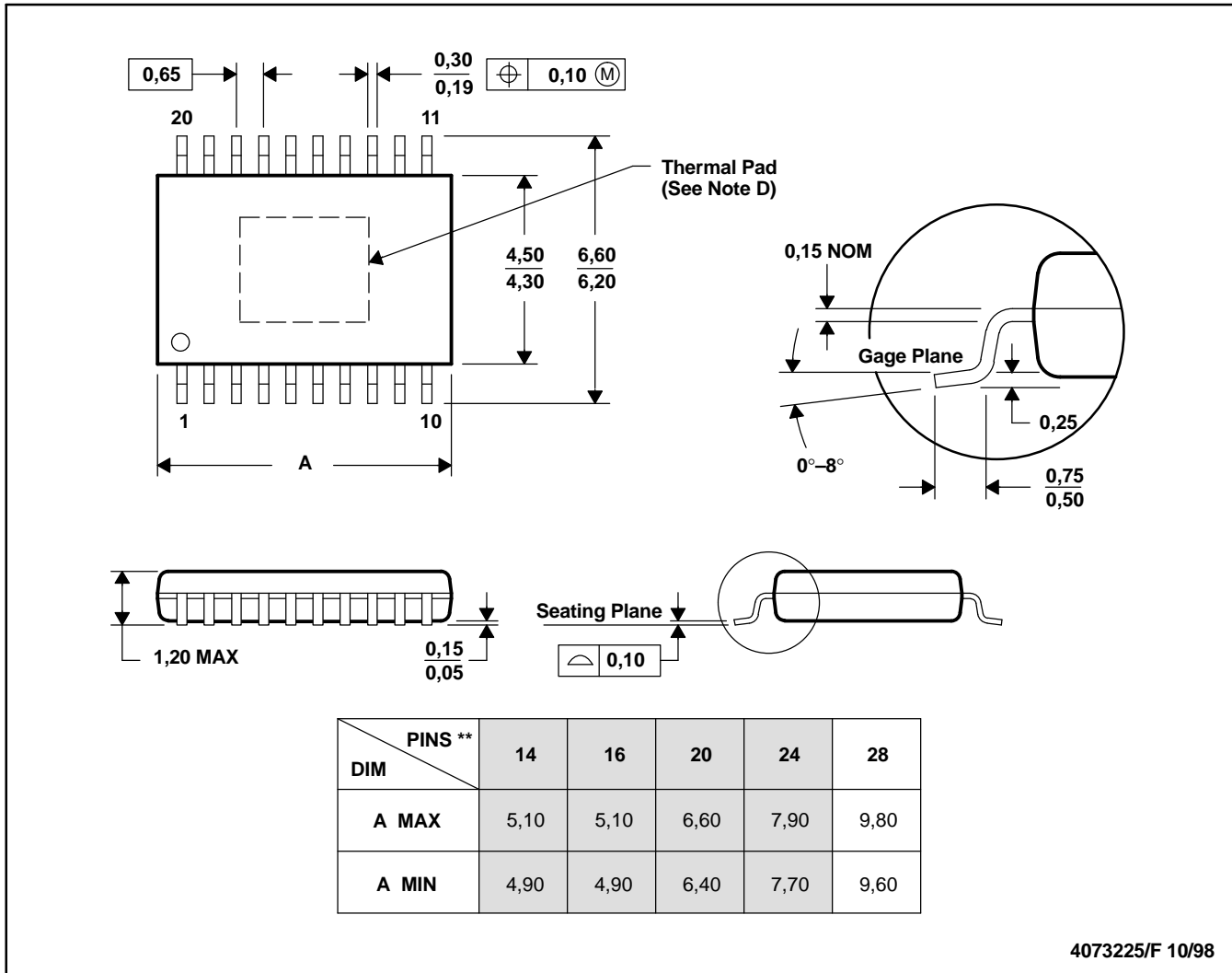
- VIN < UVLO threshold
- VBIAS or internal reference have not settled.
- Thermal shutdown is active.

MECHANICAL DATA

PWR (R-PDSO-G)**

PowerPAD™ PLASTIC SMALL-OUTLINE

20 PINS SHOWN



- (A) All linear dimensions are in millimeters.
- (B) This drawing is subject to change without notice.
- (C) Body dimensions do not include mold flash or protrusions.
- (D) The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
- (E) Falls within JEDEC MO-153

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