

- **Members of the Texas Instruments Widebus™ Family**
- **Output Ports Have Equivalent 25- $\Omega$  Series Resistors So No External Resistors Are Required**
- **State-of-the-Art EPIC-IIIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **High-Impedance State During Power Up and Power Down**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

#### description

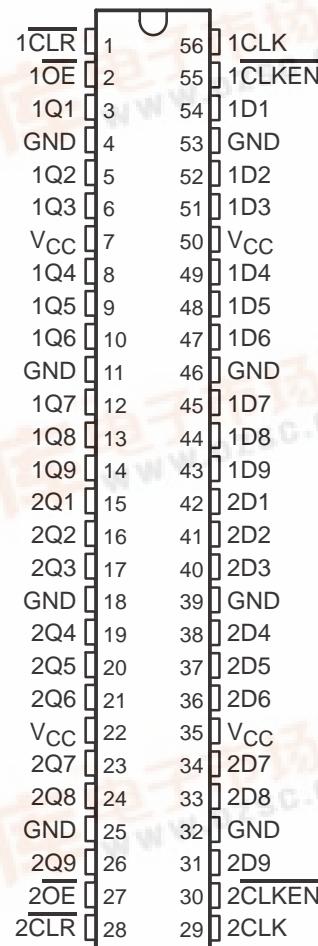
These 18-bit bus-interface flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT162823A can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ( $\overline{OE}$ ) input places the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.  $\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25- $\Omega$  series resistors to reduce overshoot and undershoot.

**SN54ABT162823A . . . WD PACKAGE**  
**SN74ABT162823A . . . DL PACKAGE**  
 (TOP VIEW)



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**SN54ABT162823A, SN74ABT162823A  
18-BIT BUS-INTERFACE FLIP-FLOPS  
WITH 3-STATE OUTPUTS**

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**description (continued)**

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT162823A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABT162823A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

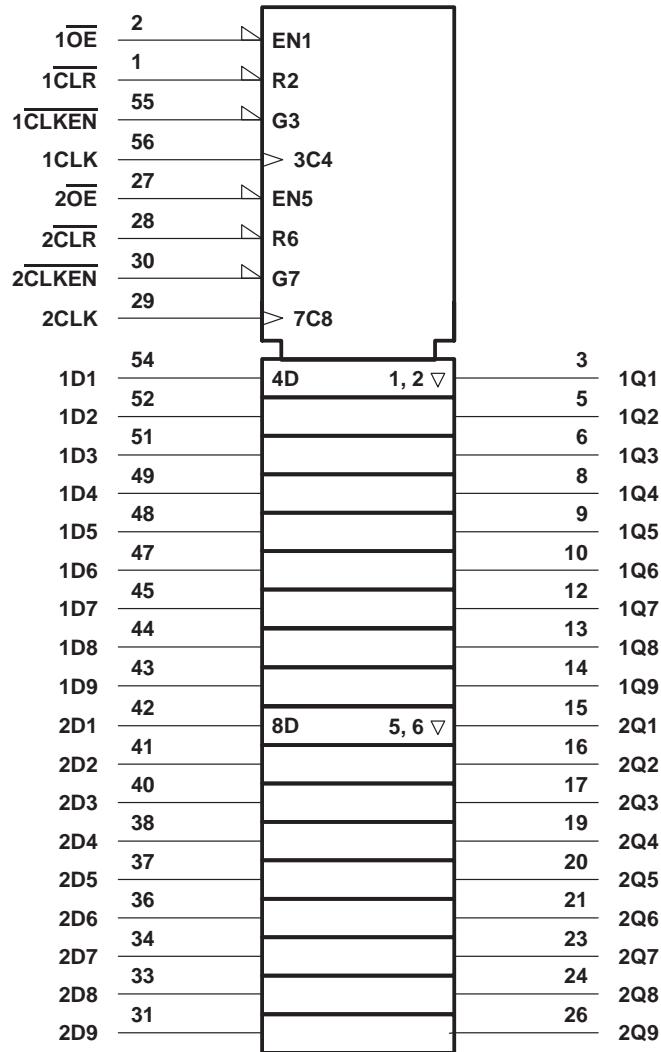
**FUNCTION TABLE  
(each 9-bit flip-flop)**

INPUTS					OUTPUT Q
$\overline{OE}$	CLR	CLKEN	CLK	D	
L	L	X	X	X	L
L	H	L	$\uparrow$	H	H
L	H	L	$\uparrow$	L	L
L	H	L	L	X	$Q_0$
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

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**logic symbol†**

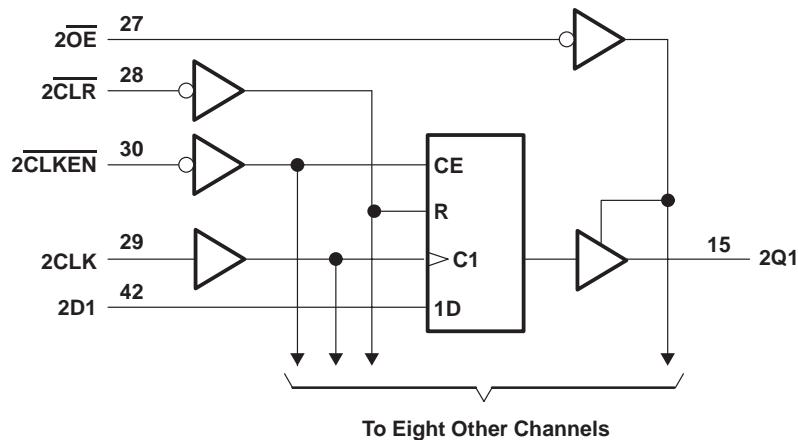
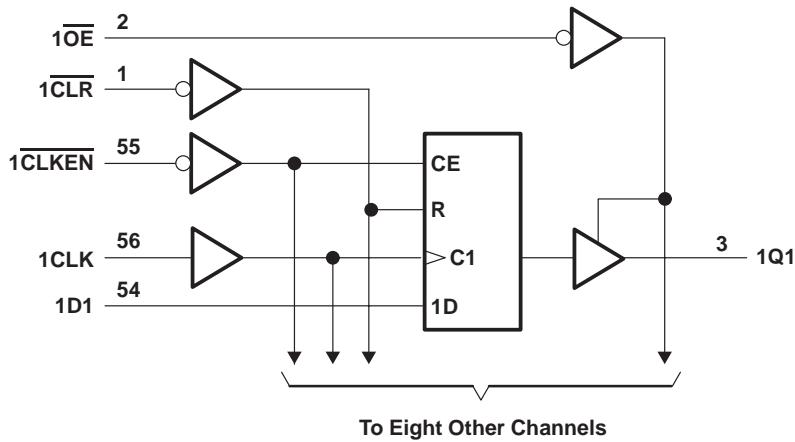


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ .....	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51, except through-hole packages, which use a trace length of zero.

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**recommended operating conditions (see Note 3)**

		SN54ABT162823A		SN74ABT162823A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-12		-12	mA
$I_{OL}$	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Input transition rise or fall rate		200		200	$\mu s/V$
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}C$

NOTE 3: Unused inputs must be held high or low to prevent them floating.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A = 25^{\circ}C$			SN54ABT162823A	SN74ABT162823A	UNIT
		MIN	TYPT†	MAX	MIN	MAX	
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA		-1.2		-1.2		-1.2
$V_{OH}$	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.5			2.5	2.5	V
	$V_{CC} = 5$ V, $I_{OH} = -1$ mA	3			3	3	
	$V_{CC} = 4.5$ V	2.4			2.4	2.4	
		$I_{OH} = -12$ mA	2*			2	
$V_{OL}$	$V_{CC} = 4.5$ V	$I_{OL} = 8$ mA	0.4	0.8	0.8	0.65	V
		$I_{OL} = 12$ mA				0.8	
$I_I$	$V_{CC} = 5.5$ V, $V_I = V_{CC}$ or GND		$\pm 1$		$\pm 1$	$\pm 1$	$\mu A$
$I_{OZPU}$	$V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$		$\pm 50$		$\pm 50$	$\pm 50$	$\mu A$
$I_{OZPD}$	$V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$		$\pm 50$		$\pm 50$	$\pm 50$	$\mu A$
$I_{OZH}^{\ddagger}$	$V_{CC} = 5.5$ V, $V_O = 2.7$ V		10		10	10	$\mu A$
$I_{OZL}^{\ddagger}$	$V_{CC} = 5.5$ V, $V_O = 0.5$ V		-10		-10	-10	$\mu A$
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O \leq 4.5$ V		$\pm 100$			$\pm 100$	$\mu A$
$I_{CEX}$	$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high		50	50	50	$\mu A$
$I_O^{\S}$	$V_{CC} = 5.5$ V, $V_O = 2.5$ V	-25	-55	-100	-25	-100	mA
$I_{CC}$	$V_{CC} = 5.5$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high		0.5	0.5	0.5	mA
		Outputs low		80	80	80	
		Outputs disabled		0.5	0.5	0.5	
$\Delta I_{CC}^{\ \}$	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND			1.5	1.5	1.5	mA
$C_I$	$V_I = 2.5$ V or 0.5 V		3.5				pF
$C_O$	$V_O = 2.5$ V or 0.5 V		9				pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at  $V_{CC} = 5$  V.

‡ The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL-voltage level rather than  $V_{CC}$  or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$		SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency		0	150	0	150	0	150	MHz
$t_w$	Pulse duration	CLR low	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
$t_{su}$	Setup time before CLK↑	CLR inactive	1.6		2		1.6		ns
		Data	2		2		2		
		CLKEN low	2.8		2.8		2.8		
$t_h$	Hold time after CLK↑	Data	1.2		1.2		1.2		ns
		CLKEN low	0.6		0.6		0.6		

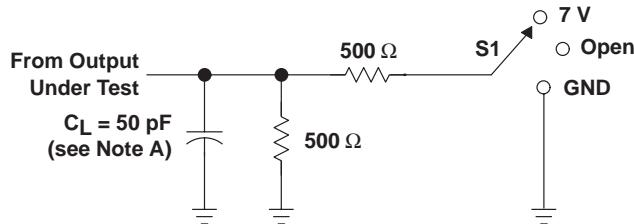
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$			SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			150			150		150		MHz
$t_{PLH}$	CLK	Q	2.3	4.6	6.2	2.3	8.4	2.3	7.5	ns
$t_{PHL}$			2.8	4.6	6.1	2.8	7.1	2.8	6.7	
$t_{PHL}$	CLR	Q	2.8	5	6.3	2.8	7.2	2.8	7	ns
$t_{PZH}$	OE	Q	1.7	3.8	5	1.7	5.8	1.7	5.9	ns
$t_{PZL}$			3	5	6.1	3	7.2	3	7	
$t_{PHZ}$	OE	Q	2.6	4.8	6.1	2.6	7.3	2.6	6.6	ns
$t_{PLZ}$			1.9	4.6	6.7	1.9	10.2	1.9	9	

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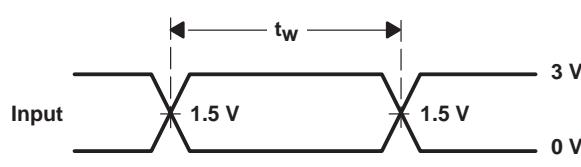
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PARAMETER MEASUREMENT INFORMATION

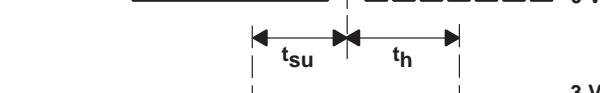


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

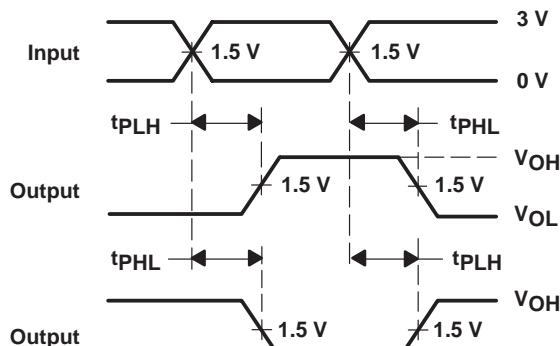
LOAD CIRCUIT



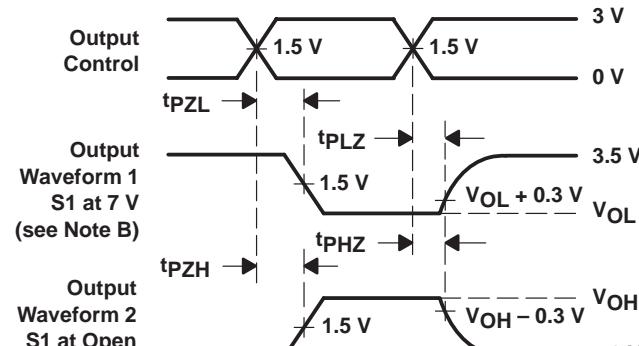
VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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