

# SN54ABT374, SN74ABT374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS111G – FEBRUARY 1991 – REVISED JANUARY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

## description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

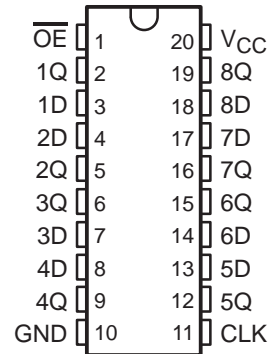
The eight flip-flops of the SN54ABT374 and SN74ABT374A are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

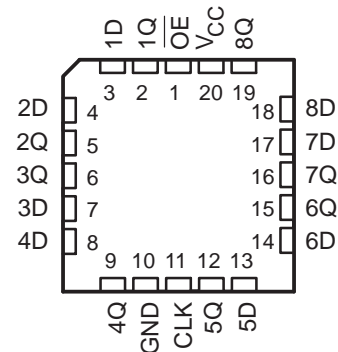
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT374 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT374A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT374 . . . J OR W PACKAGE  
SN74ABT374A . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ABT374 . . . FK PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

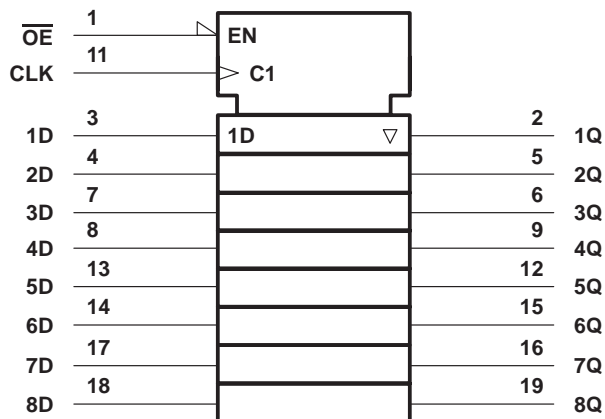
# SN54ABT374, SN74ABT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS111G – FEBRUARY 1991 – REVISED JANUARY 1997

FUNCTION TABLE  
(each flip-flop)

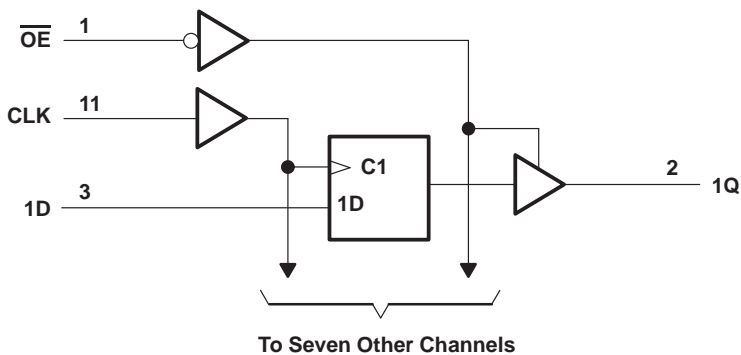
| INPUTS          |        |   | OUTPUT |
|-----------------|--------|---|--------|
| $\overline{OE}$ | CLK    | D | Q      |
| L               | ↑      | H | H      |
| L               | ↑      | L | L      |
| L               | H or L | X | $Q_0$  |
| H               | X      | X | Z      |

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# SN54ABT374, SN74ABT374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS111G – FEBRUARY 1991 – REVISED JANUARY 1997

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |                 |
|---|-----------------|
| Supply voltage range, $V_{CC}$ .....  | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1) .....                                   | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ ..... | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT374 .....              | 96 mA           |
| SN74ABT374A .....   | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....                              | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....         | 115°C/W         |
| DW package .....  | 97°C/W          |
| N package .....   | 67°C/W          |
| PW package .....  | 128°C/W         |
| Storage temperature range, $T_{stg}$ .....                                      | –65°C to 150°C  |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

|                     |                                    | SN54ABT374      |          | SN74ABT374A |          | UNIT |
|---------------------|------------------------------------|-----------------|----------|-------------|----------|------|
|                     |                                    | MIN             | MAX      | MIN         | MAX      |      |
| $V_{CC}$            | Supply voltage                     | 4.5             | 5.5      | 4.5         | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | 2               |          | 2           |          | V    |
| $V_{IL}$            | Low-level input voltage            |                 | 0.8      |             | 0.8      | V    |
| $V_I$               | Input voltage                      | 0               | $V_{CC}$ | 0           | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          |                 | –24      |             | –32      | mA   |
| $I_{OL}$            | Low-level output current           |                 | 48       |             | 64       | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled |          | 5           | 5        | ns/V |
| $T_A$               | Operating free-air temperature     | –55             | 125      | –40         | 85       | °C   |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



# SN54ABT374, SN74ABT374A

## OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

SCBS111G – FEBRUARY 1991 – REVISED JANUARY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                   | TEST CONDITIONS  | $T_A = 25^\circ\text{C}$ |      |                | SN54ABT374 |                | SN74ABT374A |                | UNIT          |               |    |
|-----------------------------|--|--------------------------|------|----------------|------------|----------------|-------------|----------------|---------------|---------------|----|
|                             |  | MIN                      | TYP† | MAX            | MIN        | MAX            | MIN         | MAX            |               |               |    |
| $V_{IK}$                    | $V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$  |                          |      | -1.2           |            | -1.2           |             | -1.2           | V             |               |    |
| $V_{OH}$                    | $V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$  |                          |      | 2.5            |            | 2.5            |             | 2.5            | V             |               |    |
|                             | $V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$  |                          |      | 3              |            | 3              |             | 3              |               |               |    |
|                             | $V_{CC} = 4.5\text{ V}$  | $I_{OH} = -24\text{ mA}$ |      |                | 2          |                |             | 2              |               |               |    |
| $V_{OL}$                    | $V_{CC} = 4.5\text{ V}$  | $I_{OL} = 48\text{ mA}$  |      |                |            | 0.55           |             |                | V             |               |    |
|                             |  | $I_{OL} = 64\text{ mA}$  |      |                |            | 0.55*          |             | 0.55           |               |               |    |
| $V_{hys}$                   |  |                          |      | 100            |            |                |             |                | mV            |               |    |
| $I_I$                       | $V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$ or GND  |                          |      | $\pm 1$        |            | $\pm 1$        |             | $\pm 1$        | $\mu\text{A}$ |               |    |
| $I_{OZH}$                   | $V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$   |                          |      | $10^\ddagger$  |            | $10^\ddagger$  |             | $10^\ddagger$  | $\mu\text{A}$ |               |    |
| $I_{OZL}$                   | $V_{CC} = 5.5\text{ V}$ , $V_O = 0.5\text{ V}$   |                          |      | $-10^\ddagger$ |            | $-10^\ddagger$ |             | $-10^\ddagger$ | $\mu\text{A}$ |               |    |
| $I_{off}$                   | $V_{CC} = 0$ , $V_I$ or $V_O \leq 4.5\text{ V}$  |                          |      | $\pm 100$      |            |                |             | $\pm 100$      | $\mu\text{A}$ |               |    |
| $I_{CEX}$                   | $V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$   | Outputs high             |      |                |            | 50             |             | 50             | $\mu\text{A}$ |               |    |
| $I_{O}^{\S}$                | $V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$   |                          |      | -50            | -100       | -180           | -50         | -180           | -50           | -180          | mA |
| $I_{CC}$                    | $V_{CC} = 5.5\text{ V}$ , $I_O = 0$ ,<br>$V_I = V_{CC}$ or GND                             | Outputs high             |      |                |            | 250            |             | 250            | 250           | $\mu\text{A}$ |    |
|                             |  | Outputs low              |      |                |            | 30             |             | 30             | 30            | mA            |    |
|                             |  | Outputs disabled         |      |                |            | 250            |             | 250            | 250           | $\mu\text{A}$ |    |
| $\Delta I_{CC}^{\parallel}$ | $V_{CC} = 5.5\text{ V}$ , One input at $3.4\text{ V}$ ,<br>Other inputs at $V_{CC}$ or GND |                          |      |                |            | 1.5            |             | 1.5            | 1.5           | mA            |    |
| $C_i$                       | $V_I = 2.5\text{ V}$ or $0.5\text{ V}$   |                          |      |                |            | 3.5            |             |                |               | pF            |    |
| $C_o$                       | $V_O = 2.5\text{ V}$ or $0.5\text{ V}$   |                          |      |                |            | 6.5            |             |                |               | pF            |    |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ This data sheet limit may vary among suppliers.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|             |                        | SN54ABT374  |     |     |     | UNIT |
|-------------|------------------------|---|-----|-----|-----|------|
|             |                        | $V_{CC} = 5\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |     | MIN | MAX |      |
|             |                        | MIN   | MAX |     |     |      |
| $f_{clock}$ | Clock frequency        | 0   | 150 | 0   | 150 | MHz  |
| $t_w$       | Pulse duration         | CLK high or low                                     |     | 3.3 | 3.3 | ns   |
| $t_{su}$    | Setup time before CLK↑ | Data high   |     | 2   | 2.5 | ns   |
|             |                        | Data low  |     | 2   | 2.5 |      |
| $t_h$       | Hold time after CLK↑   | Data high or low                                    |     | 2   | 2.5 | ns   |



# SN54ABT374, SN74ABT374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS111G – FEBRUARY 1991 – REVISED JANUARY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|                    |                        |                  | SN74ABT374A                                     |     |      |     | UNIT |     |
|--------------------|------------------------|------------------|---|-----|------|-----|------|-----|
|                    |                        |                  | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |      | MIN |      | MAX |
|                    |                        |                  | MIN   | MAX |      |     |      |     |
| f <sub>clock</sub> | Clock frequency        |                  | 0   | 150 | 0    | 150 | MHz  |     |
| t <sub>w</sub>     | Pulse duration         | CLK high or low  | 3.3   |     | 3.3  |     | ns   |     |
| t <sub>su</sub>    | Setup time before CLK↑ | Data high        | 1   |     | 1    |     | ns   |     |
|                    |                        | Data low         | 1.9   |     | 1.9  |     |      |     |
| t <sub>h</sub>     | Hold time after CLK↑   | Data high or low | 2.1†  |     | 2.1† |     | ns   |     |

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN54ABT374                                      |     |     |     | UNIT |     |
|------------------|-----------------|----------------|---|-----|-----|-----|------|-----|
|                  |                 |                | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | MIN |      | MAX |
|                  |                 |                | MIN   | TYP | MAX |     |      |     |
| f <sub>max</sub> |                 |                | 150   | 200 |     | 150 | MHz  |     |
| t <sub>PLH</sub> | CLK             | Q              | 2.2   | 4.2 | 5.7 | 1.8 | 6.6  | ns  |
| t <sub>PHL</sub> |                 |                | 3.1   | 5.1 | 6.6 | 2.6 | 7.6  |     |
| t <sub>PZH</sub> | $\overline{OE}$ | Q              | 1.2   | 3.2 | 4.7 | 0.8 | 5.7  | ns  |
| t <sub>PZL</sub> |                 |                | 2.3   | 4.7 | 6.2 | 1.5 | 7.2  |     |
| t <sub>PHZ</sub> | $\overline{OE}$ | Q              | 2.3   | 4.5 | 6.1 | 1.3 | 7.2  | ns  |
| t <sub>PLZ</sub> |                 |                | 1.9   | 4.5 | 6   | 1   | 7    |     |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN74ABT374A                                     |     |     |     | UNIT |     |
|------------------|-----------------|----------------|---|-----|-----|-----|------|-----|
|                  |                 |                | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | MIN |      | MAX |
|                  |                 |                | MIN   | TYP | MAX |     |      |     |
| f <sub>max</sub> |                 |                | 150   | 200 |     | 150 | MHz  |     |
| t <sub>PLH</sub> | CLK             | Q              | 2.2   | 4.2 | 5.7 | 2.2 | 6.2  | ns  |
| t <sub>PHL</sub> |                 |                | 3.1   | 5.1 | 6.6 | 3.1 | 7.1  |     |
| t <sub>PZH</sub> | $\overline{OE}$ | Q              | 1.2   | 3.2 | 4.7 | 1.2 | 5.2  | ns  |
| t <sub>PZL</sub> |                 |                | 2.7   | 4.7 | 6.2 | 2.7 | 6.7  |     |
| t <sub>PHZ</sub> | OE              | Q              | 2.5   | 4.5 | 6   | 2.5 | 6.7† | ns  |
| t <sub>PLZ</sub> |                 |                | 2   | 4.5 | 6   | 2   | 6.5  |     |

† This data sheet limit may vary among suppliers.

# SN54ABT374, SN74ABT374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS111G – FEBRUARY 1991 – REVISED JANUARY 1997

## PARAMETER MEASUREMENT INFORMATION

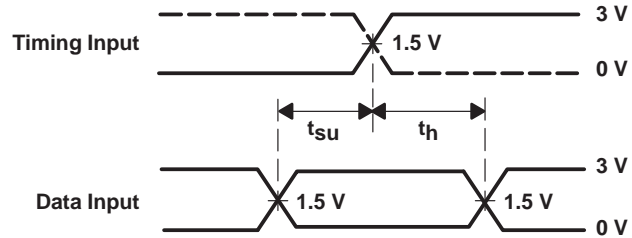


LOAD CIRCUIT

| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



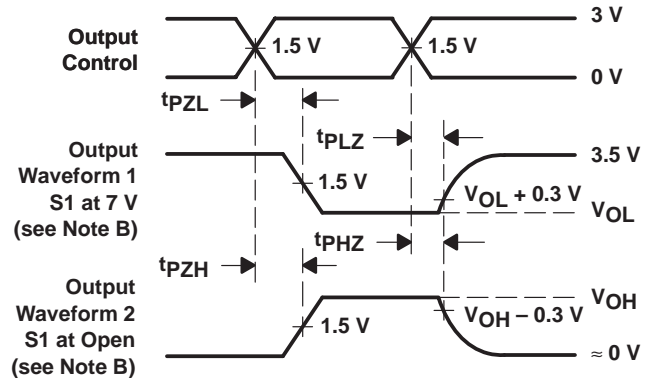
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © Each Manufacturing Company.

All Datasheets cannot be modified without permission.

This datasheet has been download from :

[www.AllDataSheet.com](http://www.AllDataSheet.com)

100% Free DataSheet Search Site.

Free Download.

No Register.

Fast Search System.

[www.AllDataSheet.com](http://www.AllDataSheet.com)